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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mnt0mlhr

Description Input Multiplexing sheet(s) attached with Reference Manual.

	Parameter	S32K11x		S32K14x			
		K116	K118	K142	K144	K146	K148
System	Core	Arm® Cortex™-M0+		Arm® Cortex™-M4F			
	Frequency	48 MHz		80 MHz (RUN mode) or 112 MHz (HSRUN mode) ¹			
	IEEE-754 FPU	○		●			
	Cryptographic Services Engine (CSEc) ¹	●		●			
	CRC module	1x		1x			
	ISO 26262	capable up to ASIL-B		capable up to ASIL-B			
	Peripheral speed	up to 48 MHz		up to 112 MHz (HSRUN)			
	Crossbar	●		●			
	DMA	●		●			
	External Watchdog Monitor (EWM)	○		●			
	Memory Protection Unit (MPU)	●		●			
	FIRC CMU	●		○			
	Watchdog	1x		1x			
	Low power modes	●		●			
	HSRUN mode ¹	○		●			
	Number of I/Os	up to 43	up to 58	up to 89	up to 128	up to 156	
	Single supply voltage	2.7 - 5.5 V		2.7 - 5.5 V			
	Ambient Operation Temperature (T _A)	-40°C to +105°C / +125°C		-40°C to +105°C / +125°C			
Memory	Flash	128 KB	256 KB	256 KB	512 KB	1 MB	2 MB ²
	Error Correcting Code (ECC)	●		●			
	System RAM (including FlexRAM and MTB)	17 KB	25 KB	32 KB	64 KB	128 KB	256 KB
	FlexRAM (also available as system RAM)	2 KB		4 KB			
	Cache	○		4 KB			
	EEPROM emulated by FlexRAM ¹	2 KB (up to 32 KB D-Flash)		4 KB (up to 64 KB D-Flash)			See footnote 3
	External memory interface	○		○			QuadSPI incl. HyperBus™
Timer	Low Power Interrupt Timer (LPIT)	1x		1x			
	FlexTimer (16-bit counter) 8 channels	2x (16)		4x (32)		6x (48)	8x (64)
	Low Power Timer (LPTMR)	1x		1x			
	Real Time Counter (RTC)	1x		1x			
	Programmable Delay Block (PDB)	1x		2x			
Analog	Trigger mux (TRGMUX)	1x (43)	1x (45)	1x (64)		1x (73)	1x (81)
	12-bit SAR ADC (1 Msps each)	1x (13)	1x (16)	2x (16)		2x (24)	2x (32)
	Comparator with 8-bit DAC	1x		1x			
Communication	10/100 Mbps IEEE-1588 Ethernet MAC	○		○			1x
	Serial Audio Interface (AC97, TDM, I2S)	○		○			2x
	Low Power UART/LIN (LPUART) (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A, and SAE J2602)	2x		2x	3x		
	Low Power SPI (LPSPPI)	1x	2x	2x	3x		
	Low Power I2C (LPI2C)	1x		1x			2x
	FlexCAN (CAN-FD ISO/CD 11898-1)	1x (1x with FD)		2x (1x with FD)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		1x			
IDEs	Debug & trace	SWD, MTB (1 KB), JTAG ⁴		SWD, JTAG (ITM, SWV, SWO)			SWD, JTAG (ITM, SWV, SWO), ETM
	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems		NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems			
Other	Packages ⁵	32-pin QFN 48-pin LQFP	48-pin LQFP 64-pin LQFP	64-pin LQFP 100-pin LQFP	64-pin LQFP 100-pin LQFP 100-pin MAPBGA	64-pin LQFP 100-pin MAPBGA 100-pin LQFP 144-pin LQFP	100-pin MAPBGA 144-pin LQFP 176-pin LQFP

LEGEND:

○ Not implemented

● Available on the device

1 No write or erase access to Flash module, including Security (CSEc) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.

2 Available when EEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.

3 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.

4 Only for Boundary Scan Register

5 See Dimensions section for package drawings

Figure 3. S32K1xx product series comparison

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. ³	Typ.	Max.	Unit
C_{REF} ^{4, 5}	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} ^{5, 6, 7}	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 μ F, 0.1 μ F and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
 - The protection/decoupling capacitors must be on the path of the trace connected to that component.
 - No trace exceeding 1 mm from the protection to the trace or to the ground.
 - The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
 - The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.

Table 5. V_{DD} supply LVR, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- RUN Mode:
 - Clock source: FIRC
 - SYS_CLK/CORE_CLK = 48 MHz
 - BUS_CLK = 48 MHz
 - FLASH_CLK = 24 MHz
- HSRUN Mode:
 - Clock source: SPL
 - SYS_CLK/CORE_CLK = 112 MHz
 - BUS_CLK = 56 MHz
 - FLASH_CLK = 28 MHz
- VLPR Mode:
 - Clock source: SIRC
 - SYS_CLK/CORE_CLK = 4 MHz
 - BUS_CLK = 4 MHz
 - FLASH_CLK = 1 MHz
- STOP1/STOP2 Mode:
 - Clock source: FIRC
 - SYS_CLK/CORE_CLK = 48 MHz
 - BUS_CLK = 48 MHz
 - FLASH_CLK = 24 MHz
- VLPS Mode: All clock sources disabled ¹

Table 6. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	μ s

Table continues on the next page...

1.

- For S32K11x – FIRC/SOSC
- For S32K14x – FIRC/SOSC/SPLL

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	μs
	STOP1 → RUN	0.07	0.075	0.08	μs
	STOP2 → RUN	0.07	0.075	0.08	μs
	VLPR → RUN	19	—	26	μs
	VLPR → VLPS	5.1	5.7	6.5	μs
	VLPS → VLPR	18.8	23	27.75	μs
	RUN → Compute operation	0.72	0.75	0.77	μs
	HSRUN → Compute operation	0.3	0.31	0.35	μs
	RUN → STOP1	0.35	0.38	0.4	μs
	RUN → STOP2	0.2	0.23	0.25	μs
	RUN → VLPS	0.3	0.35	0.4	μs
	RUN → VLPR	3.5	3.8	5	μs
	VLPS → Asynchronous DMA Wakeup	105	110	125	μs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	Pin reset → Code execution	—	214	—	μs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes_Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table [Table 7](#). For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

Table 8. VLPS additional use-case power consumption at typical conditions

Use-case	Description	Temp.	Device						Unit
			S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
VLPS and RTC	Clock source: LPO or RTC_CLKIN	25	TBD	TBD	30	30	30	40	μA
		85	TBD	TBD	110	170	180	240	μA
		105	TBD	TBD	230	330	350	490	μA
		125	TBD	TBD	570	680	810	1250	μA
VLPS and LPUART TX/RX	- Clock source: SIRC - Transmitting or receiving continuously using DMA - Baudrate: 19.2 kbps	25	TBD	TBD	230	230	250	250	μA
		85	TBD	TBD	320	400	410	490	μA
		105	TBD	TBD	490	550	600	850	μA
		125	TBD	TBD	890	1070	1250	1960	μA
VLPS and LPUART wake-up	- Clock source: SIRC - Wake-up address feature enabled - Baudrate: 19.2 kbps	25	TBD	TBD	100	100	110	110	μA
		85	TBD	TBD	170	240	280	350	μA
		105	TBD	TBD	260	400	480	600	μA
		125	TBD	TBD	530	580	1000	1280	μA
VLPS and LPI2C master	- Clock Source: SIRC - Transmit/receive using DMA - Baudrate: 100 kHz	25	TBD	TBD	670	690	820	900	μA
		85	TBD	TBD	880	960	1220	1370	μA
		105	TBD	TBD	1080	1250	1660	2060	μA
		125	TBD	TBD	1970	1980	2860	3690	μA
VLPS and LPI2C slave wake-up	- Clock source: SIRC - Wake-up address feature enabled - Baudrate: 100 kHz	25	TBD	TBD	250	250	270	280	μA
		85	TBD	TBD	340	340	410	510	μA
		105	TBD	TBD	430	430	610	810	μA
		125	TBD	TBD	740	760	1170	1540	μA
VLPS and LPSPi master	- Clock source: SIRC - Transmit/receive using DMA - Baudrate: 500 kHz	25	TBD	TBD	2.99	3.19	3.75	4.11	mA
		85	TBD	TBD	3.26	3.7	4.35	4.93	mA
		105	TBD	TBD	3.5	4.2	4.93	5.74	mA
		125	TBD	TBD	3.93	4.63	5.97	7.38	mA
VLPS and LPIT	- Clock source: SIRC 1 channel enable - Mode: 32-bit periodic counter	25	TBD	TBD	100	100	120	130	μA
		85	TBD	TBD	190	250	260	320	μA
		105	TBD	TBD	310	410	440	570	μA
		125	TBD	TBD	640	750	910	1280	μA

The following table shows the power consumption targets for S32K148 in various mode of operations measure at 3.3 V.

Table 9. Power consumption at 3.3 V

Chip/Device	Ambient Temperature (°C)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) ¹	
			Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI	Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI
S32K148	25	Typ	67.3	79.1	89.8	105.5
	85	Typ	67.4	79.2	95.6	105.9
		Max	82.5	88.2	109.7	117.4
	105	Typ	68.0	79.8	96.6	106.7
		Max	80.3	89.1	109.0	119.0
	125	Max	83.5	94.7	NA	

1. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.

4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	– 4000	4000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I _{LAT}	Latch-up current at ambient temperature of 125 °C	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input $V = V_{SS}$
7. Measured at input $V = V_{DD}$

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max.	Min.	Max.	
tRF _{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
tRF _{GPIO-HD}	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
tRF _{GPIO-FAST}	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max .	Min.	Max.	
tRF _{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
tRF _{GPIO-HD}	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

Table 16. Device clock specifications 1 (continued)

Symbol	Description	Min.	Max.	Unit
f _{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) ³				
f _{SYS}	System and core clock	—	80	MHz
f _{BUS}	Bus clock	—	40 ⁴	MHz
f _{FLASH}	Flash clock	—	26.67	MHz
VLPR mode ⁵				
f _{SYS}	System and core clock	—	4	MHz
f _{BUS}	Bus clock	—	4	MHz
f _{FLASH}	Flash clock	—	1	MHz
f _{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section [Feature comparison](#) for the availability of modes and other specifications.
2. Only available on some devices. See section [Feature comparison](#).
3. With SPLP as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description ¹		S32K116		S32K118		Unit		Notes
			Typ	Max	Typ	Max			
t _{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	ms		2
t _{pgmsec1k}	Program Section execution time (1 KB flash)	—	5	—	5	—	ms		
t _{rd1all}	Read 1s All Block execution time	—	—	1.7	—	2.8	ms		
t _{rdonce}	Read Once execution time	—	—	30	—	30	μs		
t _{pgmonce}	Program Once execution time	—	90	—	90	—	μs		
t _{ersall}	Erase All Blocks execution time	—	150	1500	230	2500	ms		2
t _{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	μs		
t _{ersallu}	Erase All Blocks Unsecure execution time	—	150	1500	230	2500	ms		2
t _{pgmpart}	Program Partition for EEPROM execution time	32 KB EEPROM backup	71	—	71	—	ms		3
		64 KB EEPROM backup	—	—	—	—			
t _{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	ms		3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2			
		48 KB EEPROM backup	—	—	—	—			
		64 KB EEPROM backup	—	—	—	—			
t _{eevr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	μs		3-4
		48 KB EEPROM backup	—	—	—	—			
		64 KB EEPROM backup	—	—	—	—			
t _{eevr16b}	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	μs		3-4
		48 KB EEPROM backup	—	—	—	—			
		64 KB EEPROM backup	—	—	—	—			
t _{eevr32bers}	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	μs		

Table continues on the next page...

Table 26. QuadSPI electrical specifications (continued)

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN ¹						HSRUN ¹						RUN/HSRUN ²			
QuadSPI Mode			SDR						SDR						SDR		DDR ³	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCK Duty Cycle	t _{SDC}	ns	t ₁ - 1.5	t ₂ + 1.5	t ₃ - 1.5	t ₄ + 1.5	t ₅ - 1.5	t ₆ + 1.5	t ₇ - 1.5	t ₈ + 1.5	t ₉ - 0.750	t ₁₀ + 0.750	t ₁₁ - 1.5	t ₁₂ + 1.5	t ₁₃ - 2.5	t ₁₄ + 2.5	t ₁₅ - 2.5	t ₁₆ + 2.5
Data Input Setup Time	t _{IS}	ns	15	-	2.5	-	10	-	14	-	1.6	-	9	-	25	-	2	-
Data Input Hold Time	t _{IH}	ns	0	-	1	-	1	-	0	-	1	-	1	-	0	-	20	-
Data Output Valid Time	t _{OV}	ns	-	4.5	-	4.5	-	4.5	-	4	-	4	-	4	-	10	-	10
Data Output In-Valid Time	t _{IV}	ns	-	5	-	5	-	5	-	5	-	3 ⁵	-	5	-	5	-	5
CS to SCK Time ⁶	t _{CSSCK}	ns	5	-	5	-	5	-	5	-	5	-	5	-	10	-	10	-
SCK to CS Time ⁷	t _{SCKCS}	ns	5	-	5	-	5	-	5	-	5	-	5	-	5	-	5	-
Output Load		pf	25		25		25		25		25		25		25		25	

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz, Output invalid time is 5 ns.
6. Program register value QuadSPI_FLSHCR[TCSS] = 4'h2
7. Program register value QuadSPI_FLSHCR[TCSH] = 4'h1

Table 32. LPSPI electrical specifications¹ (continued)

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
4	t _{Lag} ⁹	Enable lag time (After SPSCCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS+1)*t _{periph} - 25	-	(SCKPCS+1)*t _{periph} - 25	-	(SCKPCS+1)*t _{periph} - 25	-	(SCKPCS+1)*t _{periph} - 25	(SCKPCS+1)*t _{periph} - 50	-	(SCKPCS+1)*t _{periph} - 50	-		
			Master Loopback ⁵													
			Master Loopback(slow) ⁶													
5	t _{WSPSCCK} ¹⁰	Clock(SPSCCK) high or low time (SPSCCK duty cycle)	Slave	t _{SPSCCK} /2-3	t _{SPSCCK} /2+3	t _{SPSCCK} /2-3	t _{SPSCCK} /2+3	t _{SPSCCK} /2-3	t _{SPSCCK} /2+3	t _{SPSCCK} /2-3	t _{SPSCCK} /2+3	t _{SPSCCK} /2-5	t _{SPSCCK} /2+5	t _{SPSCCK} /2-5	t _{SPSCCK} /2+5	ns
			Master													
			Master Loopback ⁵													
			Master Loopback(slow) ⁶													
6	t _{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37 ¹¹ 32 ¹²	-	72	-	78	-	
			Master Loopback ⁵	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow) ⁶	8	-	10	-	7	-	9	-	20	-	20	-	
7	t _{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback ⁵	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow) ⁶	3	-	3	-	3	-	3	-	12	-	12	-	

Table continues on the next page...

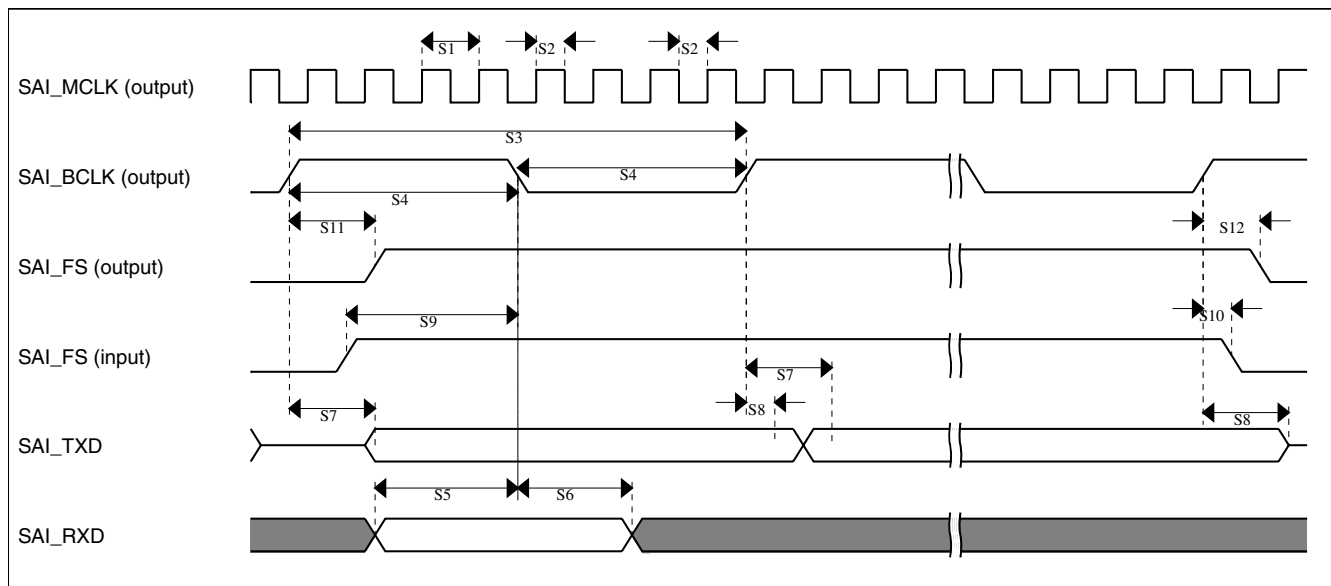


Figure 22. SAI Timing — Master modes

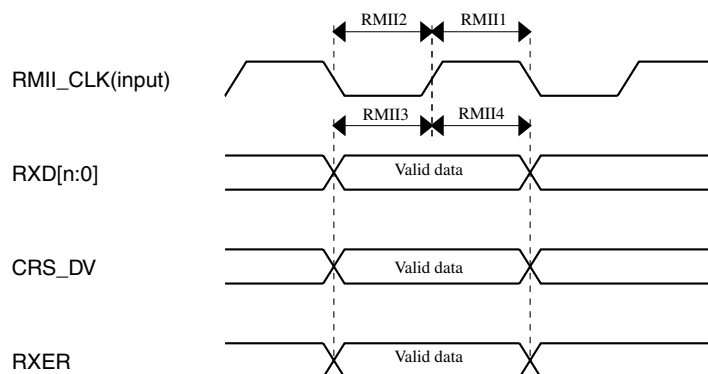
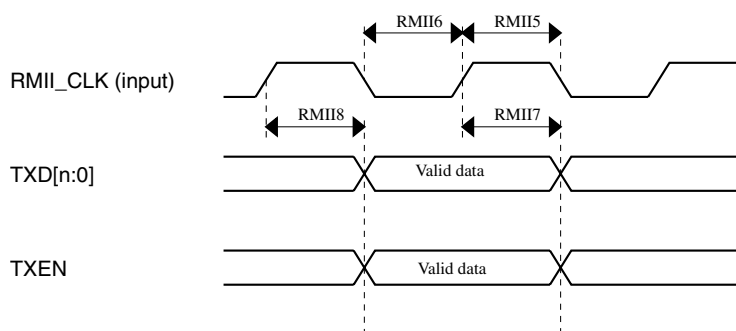
Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14 ¹	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

**Table 36. RMI signal switching specifications
(continued)**

Symbol	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	2	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

**Figure 26. RMI receive diagram****Figure 27. RMI transmit diagram**

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- MDIO pin must have external Pull-up.

Table 37. MDIO timing specifications

Symbol	Description	Min.	Max.	Unit
—	MDC Clock Frequency	—	2.5	MHz

Table continues on the next page...

Table 40. JTAG electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
J1	TCLK frequency of operation													MHz
	Boundary Scan	-	20	-	20	-	20	-	20	-	10	-	10	
	JTAG	-	20	-	20	-	20	-	20	-	10	-	10	
J2	TCLK cycle period	1/J1	-	1/J1	-	1/J1	-	1/J1	-	1/J1	-	1/J1	-	ns
J3	TCLK clock pulse width													ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG													
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	5	-	5	-	15	-	15	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	5	-	5	-	8	-	8	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	3	-	3	-	15	-	15	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	2	-	2	-	8	-	8	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Single layer board (1s)	$R_{\theta JA}$	32	93	NA	NA	NA	NA	NA	°C/W
			48	79	71	NA	NA	NA	NA	
			64	NA	62	61	61	59	NA	
			100	NA	NA	53	52	51	NA	
			144	NA	NA	NA	NA	51	44	
			176	NA	NA	NA	NA	NA	42	
Thermal resistance, Junction to Ambient (Natural Convection) ¹	Two layer board (1s1p)	$R_{\theta JA}$	32	50	NA	NA	NA	NA	NA	
			48	58	50	NA	NA	NA	NA	
			64	NA	46	45	45	44	NA	
			100	NA	NA	42	42	40	NA	
			144	NA	NA	NA	NA	44	37	
			176	NA	NA	NA	NA	NA	36	
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Four layer board (2s2p)	$R_{\theta JA}$	32	32	NA	NA	NA	NA	NA	
			48	55	47	NA	NA	NA	NA	
			64	NA	44	43	43	41	NA	
			100	NA	NA	40	40	39	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	35	
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 3}	Single layer board (1s)	$R_{\theta JMA}$	32	77	NA	NA	NA	NA	NA	
			48	66	58	NA	NA	NA	NA	
			64	NA	50	49	49	48	NA	
			100	NA	NA	43	42	41	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	34	
Thermal resistance, Junction to Ambient (@200 ft/min) ¹	Two layer board (1s1p)	$R_{\theta JMA}$	32	43	NA	NA	NA	NA	NA	
			48	51	43	NA	NA	NA	NA	
			64	NA	39	38	38	37	NA	
			100	NA	NA	35	35	34	NA	

Table continues on the next page...

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (@ 200 ft/min) ^{1, 3}	Four layer board (2s2p)	R _{θJMA}	144	NA	NA	NA	NA	37	31	
			176	NA	NA	NA	NA	NA	30	
			32	26	NA	NA	NA	NA	NA	
			48	48	41	NA	NA	NA	NA	
			64	NA	37	36	36	35	NA	
			100	NA	NA	34	34	33	NA	
			144	NA	NA	NA	NA	36	30	
			176	NA	NA	NA	NA	NA	29	
Thermal resistance, Junction to Board ⁴	—	R _{θJB}	32	11	NA	NA	NA	NA	NA	
			48	33	24	NA	NA	NA	NA	
			64	NA	26	25	25	23	NA	
			100	NA	NA	25	25	24	NA	
			144	NA	NA	NA	NA	30	24	
			176	NA	NA	NA	NA	NA	24	
Thermal resistance, Junction to Case ⁵	—	R _{θJC}	32	NA	NA	NA	NA	NA	NA	
			48	23	19	NA	NA	NA	NA	
			64	NA	14	13	12	11	NA	
			100	NA	NA	13	12	11	NA	
			144	NA	NA	NA	NA	12	9	
			176	NA	NA	NA	NA	NA	9	
Thermal resistance, Junction to Case (Bottom) ⁶	—	R _{θJCBottom}	32	1	NA					
			48	NA						
			64							
			100							
			144							
			176							

Table continues on the next page...

Table 42. Thermal characteristics for the 100 MAPBGA package

Rating	Conditions	Symbol	Values			Unit
			S32K146	S32K144	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2}	Single layer board (1s)	R _{θJA}	57.2	61.0	52.5	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) ^{1, 2, 3}	Four layer board (2s2p)	R _{θJA}	32.1	35.6	27.5	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 2, 3}	Single layer board (1s)	R _{θJMA}	44.1	46.6	39.0	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 3}	Two layer board (2s2p)	R _{θJMA}	27.2	30.9	22.8	°C/W
Thermal resistance, Junction to Board ⁴	—	R _{θJB}	15.3	18.9	11.2	°C/W
Thermal resistance, Junction to Case ⁵	—	R _{θJC}	10.2	14.2	7.5	°C/W
Thermal resistance, Junction to Package Top outside center ⁶	—	Ψ _{JT}	0.2	0.4	0.2	°C/W
Thermal resistance, Junction to Package Bottom outside center ⁷	—	Ψ _{JB}	12.2	15.9	18.3	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package ($^{\circ}\text{C}$)
- Ψ_{JT} = thermal characterization parameter ($^{\circ}\text{C}/\text{W}$)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to <http://www.nxp.com> and perform a keyword search for the drawing's document number:

Package option	Document Number
32-pin QFN	SOT617-3 ¹
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W
100-pin MAPBGA	98ASA00802D
144-pin LQFP	98ASS23177W
176-pin LQFP	98ASS23479W

1. 5x5 mm package

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release
2	03 March 2017	- Updated description of QSPI and Clock interfaces in Key Features section - Updated figure: High-level architecture diagram for the S32K1xx family - Updated figure: S32K1xx product series comparison - Added note in section Selecting orderable part number - Updated figure: Ordering information - In table: Absolute maximum ratings : - Added footnote to I_{INJPAD_DC} - Updated min and max value of I_{INJPAD_DC} - Updated description, max and min values for I_{INJSUM} - Updated $V_{IN_TRANSIENT}$ - In table: Voltage and current operating requirements : - Renamed V_{SUP_OFF} - Updated max value of V_{DD_OFF} - Removed V_{INA} and V_{IN} - Added V_{REFH} and V_{REFL} - Updated footnote "Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V ..." - Removed I_{NJSUM_AF} - Updated footnotes in table Table 4 - Updated section Power mode transition operating behaviors - In table: Power consumption - Added footnote "With PMC_REGSC[CLKBIASDIS] ..." - Updated conditions for VLPR - Removed I_{dd}/MHz for S32K144 - Updated numbers for S32K142 and S32K148 - Removed use case footnotes - In section Modes configuration : - Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes_Master_configuration_sheet' - In table: DC electrical specifications at 3.3 V Range : - Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage - Added footnote to High drive port pins - In table: DC electrical specifications at 5.0 V Range :

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated 3.3 V numbers and added footnote against f_{op}, t_{SU}, and t_V in HSRUN Mode - Added footnote to 't_{WSPCK}' - Updated Thermal characteristics for S32K11x
6	31 Jan 2018	- Changed the representation of ARM trademark throughout. - Removed S32K142 from 'Caution' - In 'Key features', added the following note under 'Power management', 'Memory and memory interfaces', and 'Reliability, safety and security': - No write or erase access to ... - In High-level architecture diagram for the S32K14x family, added the following footnote: - No write or erase access to ... - In High-level architecture diagram for the S32K11x family : - Minor editorial update: Fixed the placement of SRAM, under 'Flash memory controller' block - Updated figure: S32K1xx product series comparison : - Updated footnote 1, and added against 'HSRUN' in addition to 'HW security module (CSEc)' and 'EEPROM emulated by FlexRAM'. - Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148. - Updated channel count for S32K116 in row '12-bit SAR ADC (1 MSPS each)'. - Updated Ordering information - Updated Flash timing specifications — commands for S32K148, S32K142, S32K146, S32K116, and S32K118.
7	19 April 2018	- Changed Caution to Notes - Updated the wordings of Notes and removed S32K146 - Added 'Following two are the available ...' - In 'Key features' : - Editorial updates - Updated the note under Power management, Memory and memory interfaces, and Safety and security. - Updated FlexIO under Communications interfaces - Added ENET and SAI under Communications interfaces - Updated Cryptographic Services Engine (CSEc) under 'Safety and security' - In High-level architecture diagram for the S32K14x family : - Minor editorial updates - Updated note 3 - In High-level architecture diagram for the S32K11x family : - Minor editorial updates - In figure: S32K1xx product series comparison : - Editorial updates - Updated Frequency for S32K14x - Updated footnote 4 - Added footnote 5 - In Ordering information : - Renamed section, updated the starting paragraph - Updated the figure - In Voltage and current operating requirements, updated the note - In Power consumption : - Updated specs for S32K146 - Removed section 'Modes configuration', and moved its content under the first paragraph. - In 12-bit ADC operating conditions :

Table continues on the next page...