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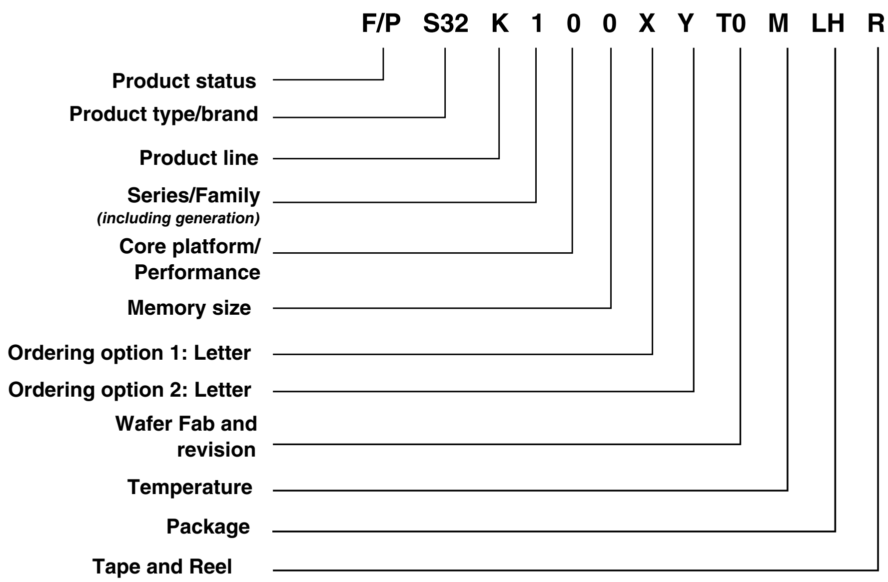
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mnt0mlht

3.2 Ordering information



Product status
P: Prototype
F: Qualified

Product type/brand
S32: Automotive 32-bit MCU

Product line
K: Arm Cortex MCUs

Series/Family
1: 1st product series
2: 2nd product series

Core platform/Performance
1: Arm Cortex M0+
4: Arm Cortex M4F

Memory size

	2	4	6	8
S32K11x			128K	256K
S32K14x	256K	512K	1M	2M

Ordering option
X: Speed
B: 48 MHz without DMA (S32K11x only)
L: 48 MHz with DMA (S32K11x only)
H: 80 MHz
U[1]: 112 MHz (Not valid with M temperature/125C)

Y: Optional feature
R: Base feature set
F: CAN FD, FlexIO
A[1]: CAN FD, FlexIO, Security
E: Ethernet, Serial Audio Interface (S32K148 only)
J[1]: Ethernet, Serial Audio Interface, CAN FD, FlexIO, Security (S32K148 only)

Wafer, Fab and revision
Fx: ATMC[2]
Tx: GF
XX: Flex #[2]

x0: 1st revision

Temperature
V: -40C to 105C
M: -40C to 125C
W: -40C to 150C[2]

Package

Pins	LQFP	QFN	BGA
32	-	FM	-
48	LF	-	-
64	LH	-	-
100	LL	-	MH
144	LQ	-	-
176	LU	-	-

Tape and Reel
T: Trays/Tubes
R: Tape and Reel

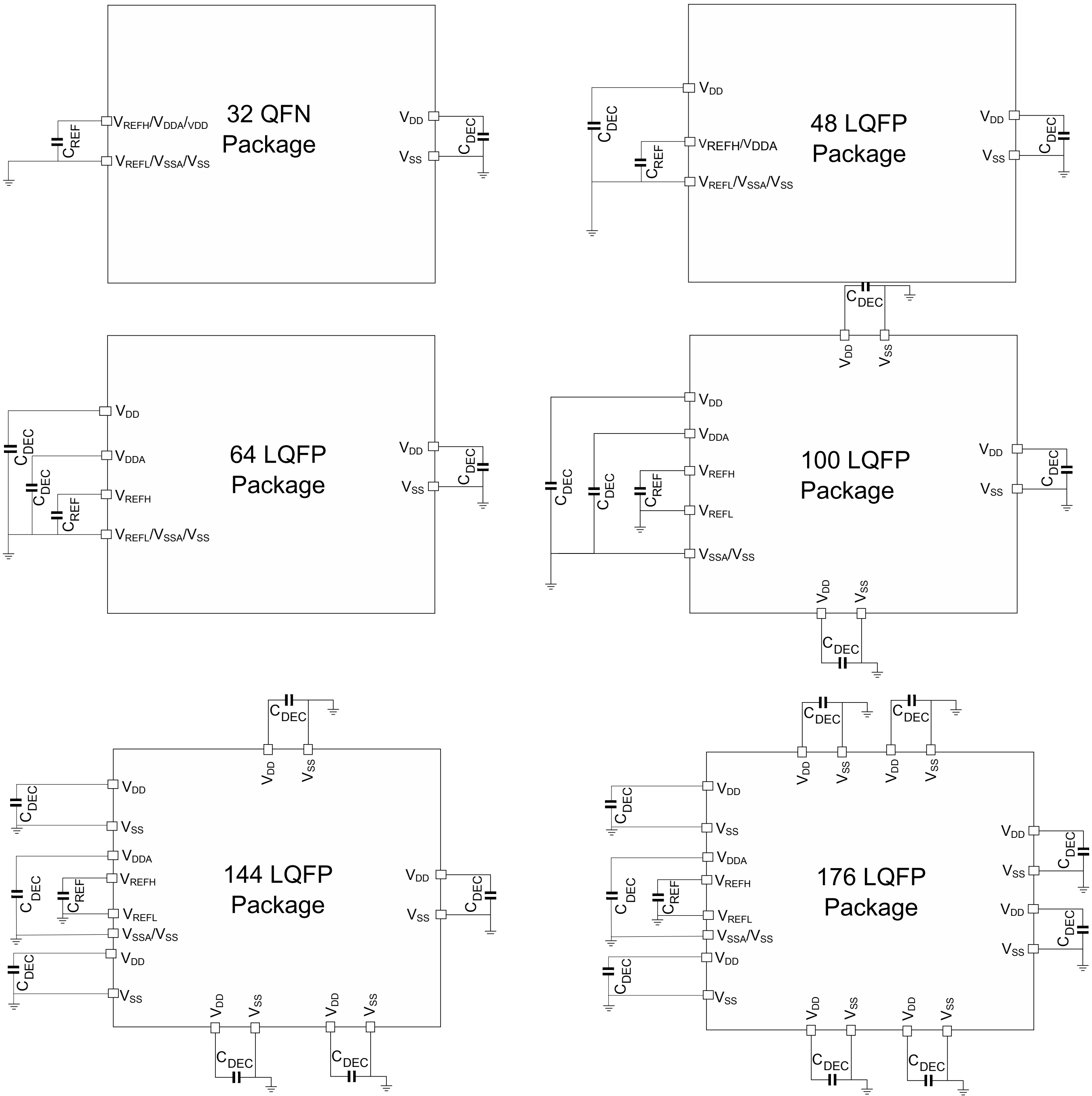
1. CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
2. Not supported yet
3. Part numbers no longer offered as standard include:
Ordering Option X (M:64MHz); Ordering Option Y (N: limited RAM. 16KB for K142, 48KB for K144, 96KB for K146, 192KB for K148 S: Security); Temperature (C: -40C to 85C)

NOTE

Not all part number combinations are available. See S32K1xx_Orderable_Part_Number_List.xlsx attached with the Datasheet for list of standard orderable parts.

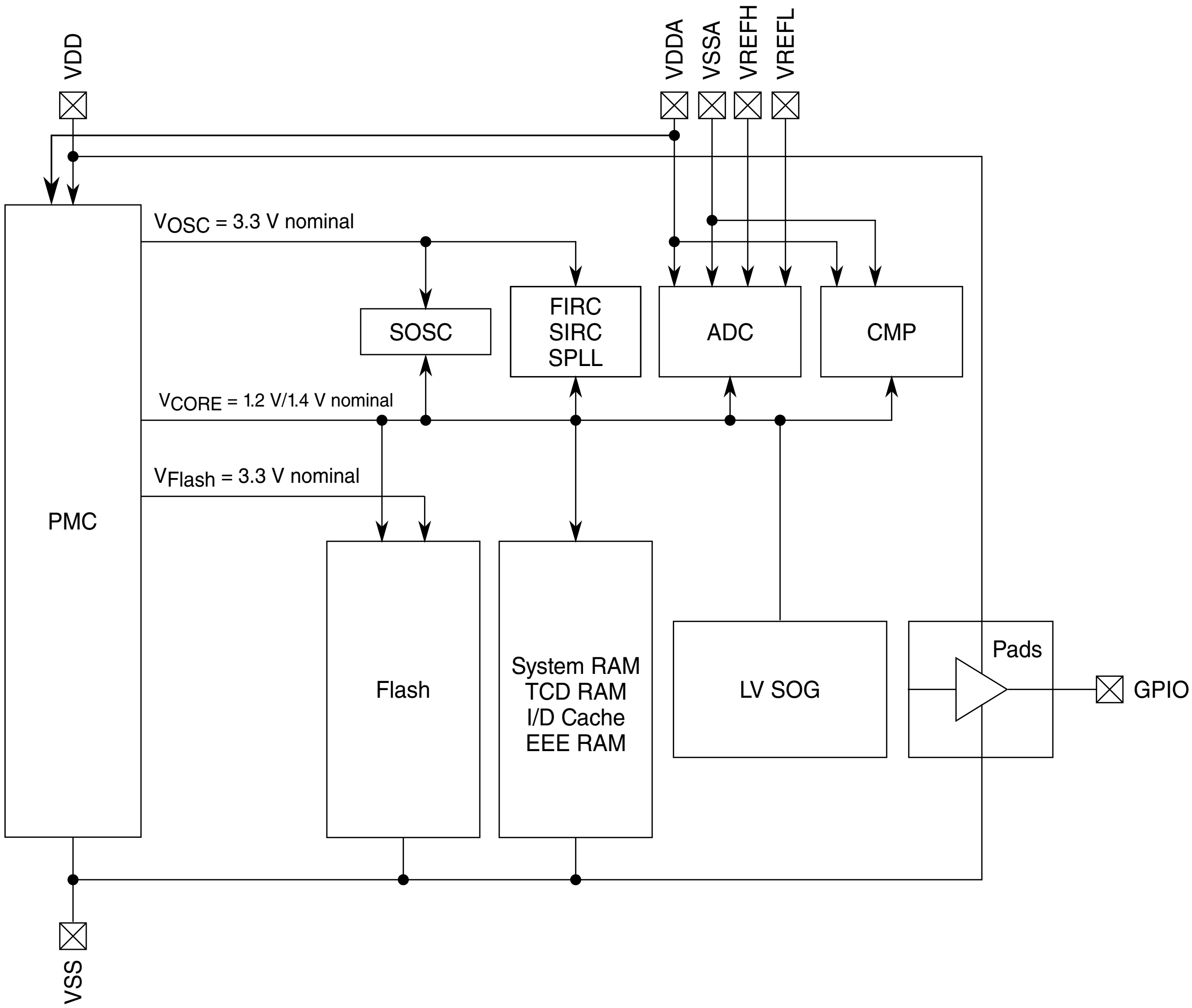
Figure 4. Ordering information

4.4 Power and ground pins



NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB

Figure 5. Pinout decoupling



*Note: VSSA and VSS are shorted at package level

Figure 6. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 5. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	1
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1

Table continues on the next page...

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	μs
	STOP1 → RUN	0.07	0.075	0.08	μs
	STOP2 → RUN	0.07	0.075	0.08	μs
	VLPR → RUN	19	—	26	μs
	VLPR → VLPS	5.1	5.7	6.5	μs
	VLPS → VLPR	18.8	23	27.75	μs
	RUN → Compute operation	0.72	0.75	0.77	μs
	HSRUN → Compute operation	0.3	0.31	0.35	μs
	RUN → STOP1	0.35	0.38	0.4	μs
	RUN → STOP2	0.2	0.23	0.25	μs
	RUN → VLPS	0.3	0.35	0.4	μs
	RUN → VLPR	3.5	3.8	5	μs
	VLPS → Asynchronous DMA Wakeup	105	110	125	μs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	Pin reset → Code execution	—	214	—	μs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes _Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table Table 7. For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input V = V_{SS}
7. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
$tRF_{GPIO-FAST}$	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

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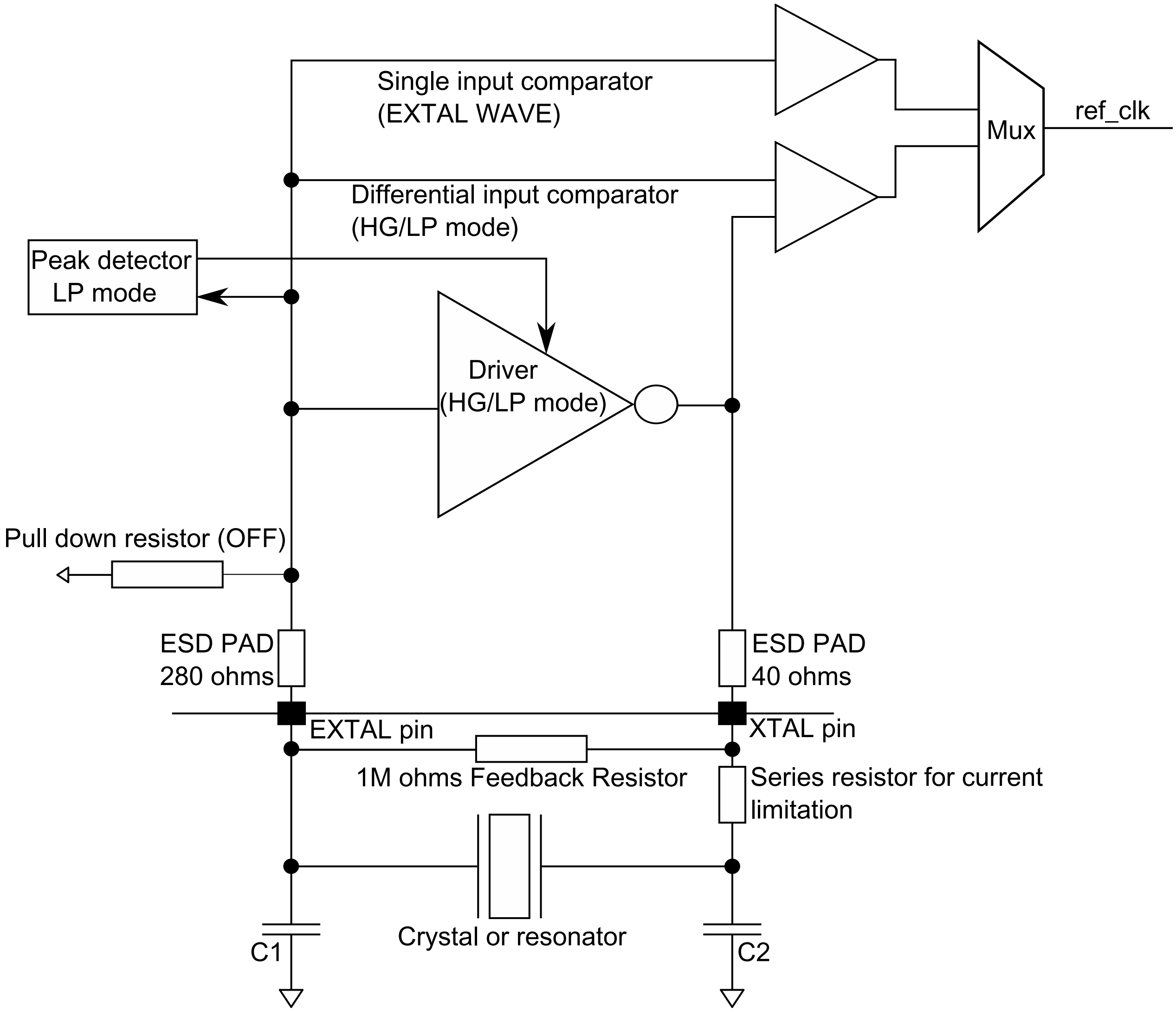

Figure 8. Oscillator connections scheme

Table 17. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz	2.2	—	13.7	mA/V	
	SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	1.15	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	[3]
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	[3,4]
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	[3,4]
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	μs	
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	μs	[3,4]
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	μs	[4,5,6]
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description[1]		S32K116		S32K118			
			Typ	Max	Typ	Max	Unit	Notes
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1 KB flash)	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	1.7	—	2.8	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	μs	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	μs	
t_{ersall}	Erase All Blocks execution time	—	150	1500	230	2500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	μs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	150	1500	230	2500	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	71	—	71	—	ms	3
		64 KB EEPROM backup	—	—	—	—		
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2		
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	μs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	μs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	μs	

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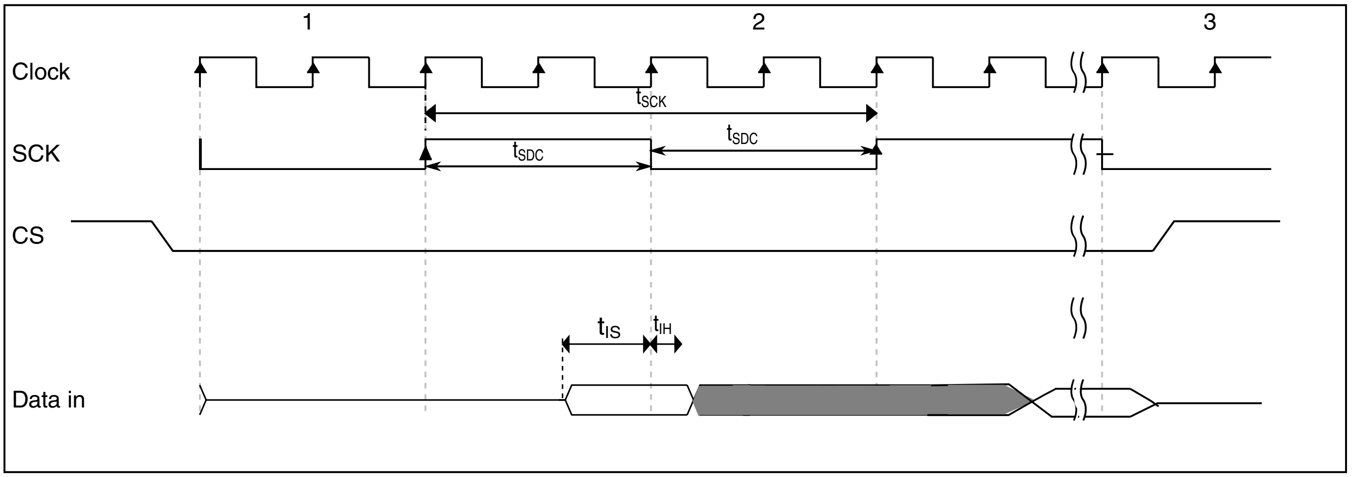


Figure 9. QuadSPI input timing (SDR mode) diagram

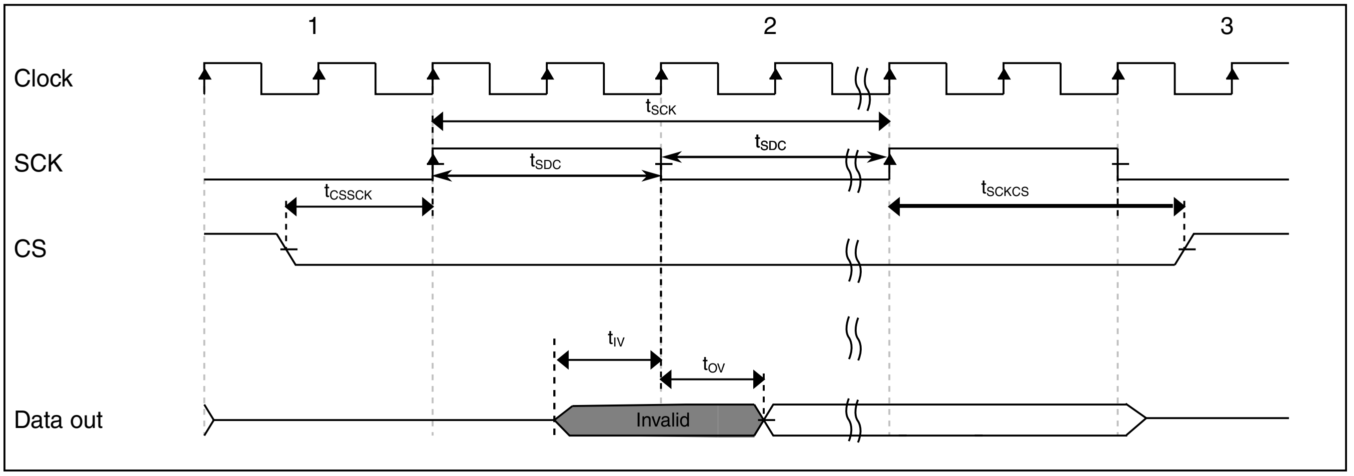
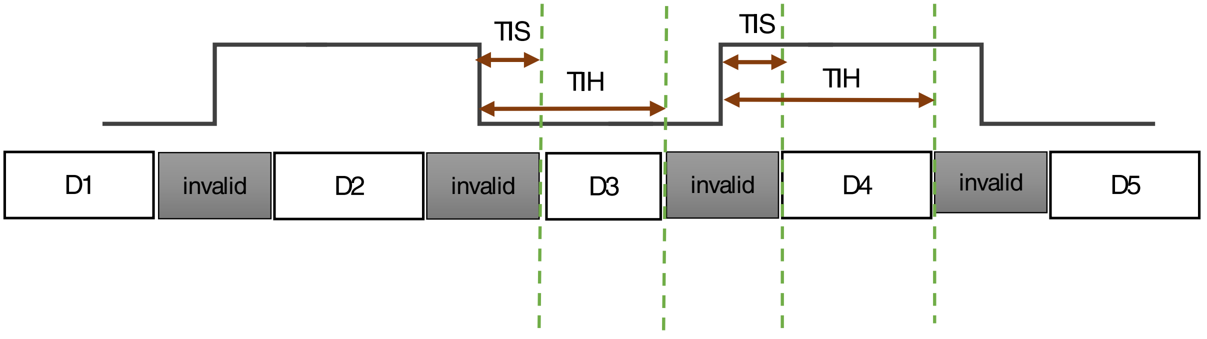


Figure 10. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time
TIH – Hold Time

Figure 11. QuadSPI input timing (HyperRAM mode) diagram

6.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See AN5426 for details

Table 28. 12-bit ADC characteristics (2.7 V to 3 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC		—	0.6	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±2.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume V_{DDA} = 3 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 32. LPSPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	f_{periph}, [3, 4]	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	4	-	4	MHz
			Master	-	40	-	40	-	56	-	56	-	4	-	4	
			Master Loopback[5]	-	40	-	48	-	48	-	48	-	4	-	4	
			Master Loopback(slow)[6]	-	48	-	48	-	48	-	48	-	4	-	4	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14 [7]	-	2	-	2	MHz
			Master	-	10	-	10	-	14	-	14 [7]	-	2	-	2	
			Master Loopback[5]	-	20	-	12	-	24	-	12	-	2	-	2	
			Master Loopback(slow)[6]	-	12	-	12	-	12	-	12	-	2	-	2	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	500	-	500	-	ns
			Master	100	-	100	-	72	-	72	-	500	-	500	-	
			Master Loopback[5]	50	-	83	-	42	-	83	-	500	-	500	-	
			Master Loopback(slow)[6]	83	-	83	-	83	-	83	-	500	-	500	-	
3	t_{Lead}[8]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	$(PCSSCK+1)*t_{periph}-25$	-	$(PCSSCK+1)*t_{periph}-25$	-	$(PCSSCK+1)*t_{periph}-25$	-	$(PCSSCK+1)*t_{periph}-25$	-	$(PCSSCK+1)*t_{periph}-50$	-	$(PCSSCK+1)*t_{periph}-50$	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													

Table continues on the next page...

Table 32. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
			Master Loopback(slow) [6]	-		-		-		-		-		-		

1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. f_{periph} = LPSPI peripheral clock
4. $t_{periph} = 1/f_{periph}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
7. This is the maximum operating frequency (f_{op}) for LPSPI0 with medium PAD type only. Otherwise, the maximum operating frequency (f_{op}) is 12 Mhz.
8. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
9. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.
10. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
11. Maximum operating frequency (f_{op}) is 12 MHz irrespective of PAD type and LPSPI instance.
12. Applicable for LPSPI0 only with medium PAD type, with maximum operating frequency (f_{op}) as 14 MHz.

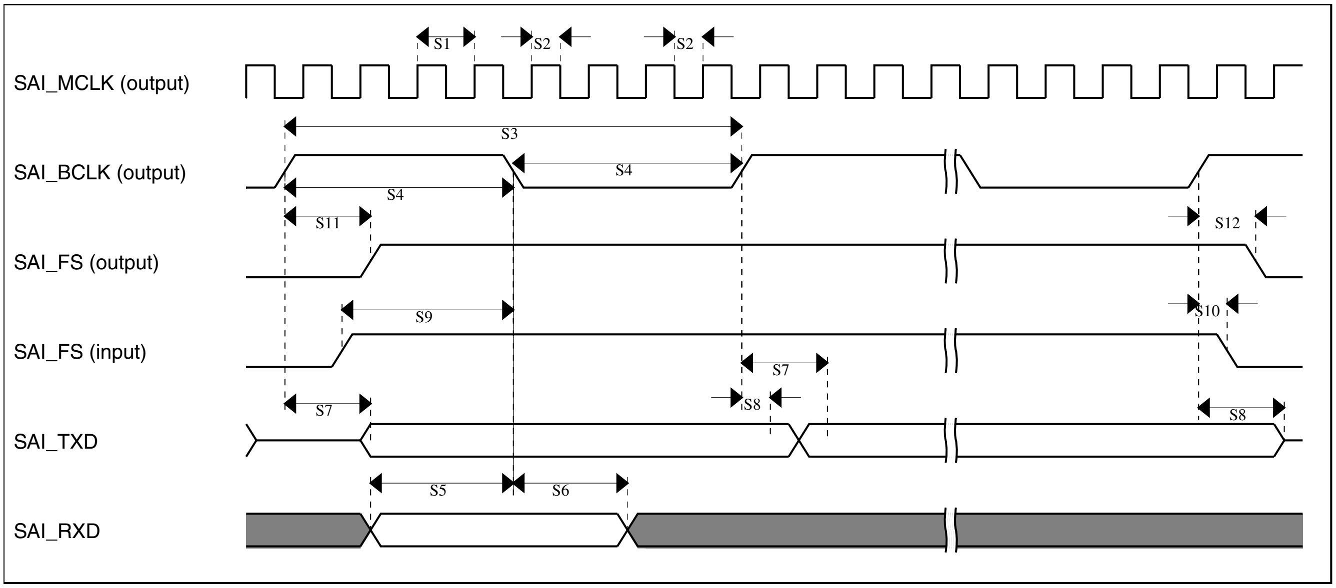


Figure 22. SAI Timing — Master modes

Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14[1]	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

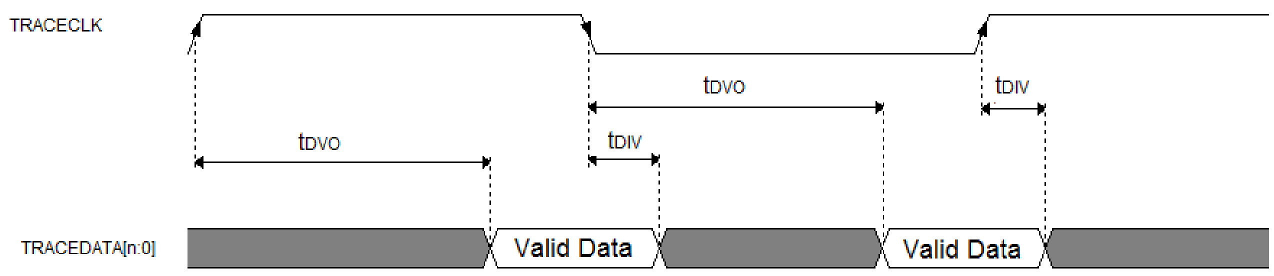


Figure 31. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

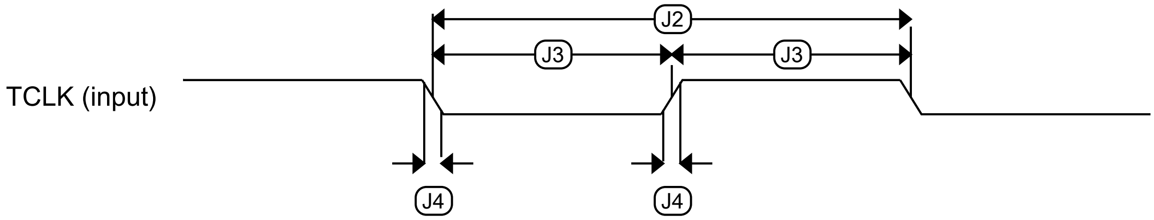


Figure 32. Test clock input timing

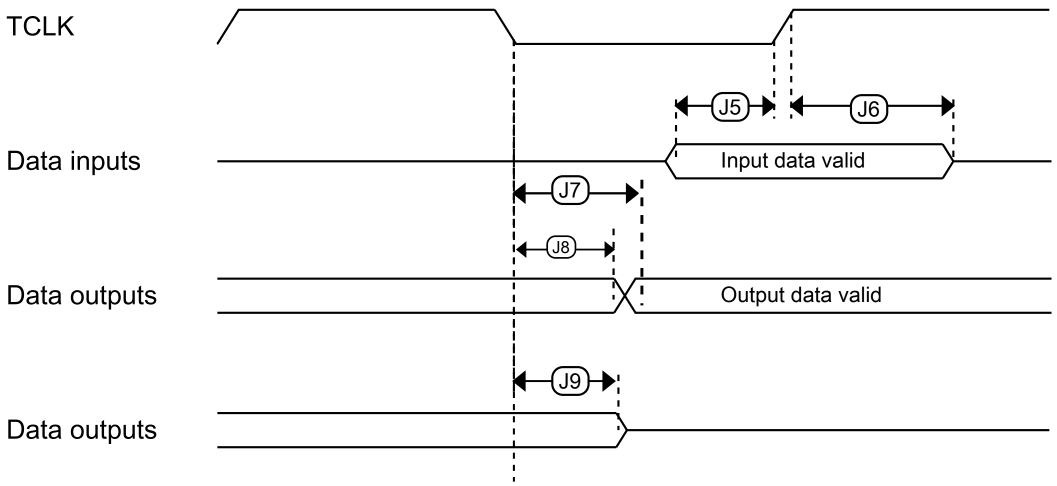


Figure 33. Boundary scan (JTAG) timing

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	32	93	NA	NA	NA	NA	NA	°C/W
			48	79	71	NA	NA	NA	NA	
			64	NA	62	61	61	59	NA	
			100	NA	NA	53	52	51	NA	
			144	NA	NA	NA	NA	51	44	
			176	NA	NA	NA	NA	NA	42	
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Two layer board (1s1p)	$R_{\theta JA}$	32	50	NA	NA	NA	NA	NA	
			48	58	50	NA	NA	NA	NA	
			64	NA	46	45	45	44	NA	
			100	NA	NA	42	42	40	NA	
			144	NA	NA	NA	NA	44	37	
			176	NA	NA	NA	NA	NA	36	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	32	32	NA	NA	NA	NA	NA	
			48	55	47	NA	NA	NA	NA	
			64	NA	44	43	43	41	NA	
			100	NA	NA	40	40	39	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	35	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	32	77	NA	NA	NA	NA	NA	
			48	66	58	NA	NA	NA	NA	
			64	NA	50	49	49	48	NA	
			100	NA	NA	43	42	41	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	34	
Thermal resistance, Junction to Ambient (@200 ft/min)[1]	Two layer board (1s1p)	$R_{\theta JMA}$	32	43	NA	NA	NA	NA	NA	
			48	51	43	NA	NA	NA	NA	
			64	NA	39	38	38	37	NA	
			100	NA	NA	35	35	34	NA	

Table continues on the next page...

Table 42. Thermal characteristics for the 100 MAPBGA package

Rating	Conditions	Symbol	Values			Unit
			S32K146	S32K144	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) [1, 2]	Single layer board (1s)	$R_{\theta JA}$	57.2	61.0	52.5	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) [1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	32.1	35.6	27.5	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) [1, 2, 3]	Single layer board (1s)	$R_{\theta JMA}$	44.1	46.6	39.0	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Two layer board (2s2p)	$R_{\theta JMA}$	27.2	30.9	22.8	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	15.3	18.9	11.2	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	10.2	14.2	7.5	°C/W
Thermal resistance, Junction to Package Top outside center[6]	—	Ψ_{JT}	0.2	0.4	0.2	°C/W
Thermal resistance, Junction to Package Bottom outside center[7]	—	Ψ_{JB}	12.2	15.9	18.3	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number
32-pin QFN	SOT617-3 [1]
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W
100-pin MAPBGA	98ASA00802D
144-pin LQFP	98ASS23177W
176-pin LQFP	98ASS23479W

1. 5x5 mm package

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