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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mnt0mlt

Table of Contents

1	Block diagram.....	4	6.2.5	SPLL electrical specifications	32
2	Feature comparison.....	5	6.3	Memory and memory interfaces.....	32
3	Ordering information.....	7	6.3.1	Flash memory module (FTFC) electrical specifications.....	32
3.1	Selecting orderable part number	7	6.3.1.1	Flash timing specifications — commands.....	32
3.2	Ordering information	8	6.3.1.2	Reliability specifications.....	37
4	General.....	9	6.3.2	QuadSPI AC specifications.....	38
4.1	Absolute maximum ratings.....	9	6.4	Analog modules.....	42
4.2	Voltage and current operating requirements.....	10	6.4.1	ADC electrical specifications.....	42
4.3	Thermal operating characteristics.....	11	6.4.1.1	12-bit ADC operating conditions.....	42
4.4	Power and ground pins.....	12	6.4.1.2	12-bit ADC electrical characteristics.....	44
4.5	LVR, LVD and POR operating requirements.....	14	6.4.2	CMP with 8-bit DAC electrical specifications.....	46
4.6	Power mode transition operating behaviors.....	15	6.5	Communication modules.....	50
4.7	Power consumption.....	16	6.5.1	LPUART electrical specifications.....	50
4.8	ESD handling ratings.....	21	6.5.2	LPSPi electrical specifications.....	50
4.9	EMC radiated emissions operating behaviors.....	21	6.5.3	LPI2C electrical specifications.....	56
5	I/O parameters.....	22	6.5.4	FlexCAN electrical specifications.....	57
5.1	AC electrical characteristics.....	22	6.5.5	SAI electrical specifications.....	57
5.2	General AC specifications.....	22	6.5.6	Ethernet AC specifications.....	59
5.3	DC electrical specifications at 3.3 V Range.....	23	6.5.7	Clockout frequency.....	62
5.4	DC electrical specifications at 5.0 V Range.....	24	6.6	Debug modules.....	62
5.5	AC electrical specifications at 3.3 V range	25	6.6.1	SWD electrical specofications	62
5.6	AC electrical specifications at 5 V range	25	6.6.2	Trace electrical specifications.....	64
5.7	Standard input pin capacitance.....	26	6.6.3	JTAG electrical specifications.....	65
5.8	Device clock specifications.....	26	7	Thermal attributes.....	68
6	Peripheral operating requirements and behaviors.....	27	7.1	Description.....	68
6.1	System modules.....	27	7.2	Thermal characteristics.....	68
6.2	Clock interface modules.....	27	7.3	General notes for specifications at maximum junction temperature.....	73
6.2.1	External System Oscillator electrical specifications....	27	8	Dimensions.....	74
6.2.2	External System Oscillator frequency specifications .	29	8.1	Obtaining package dimensions	74
6.2.3	System Clock Generation (SCG) specifications.....	31	9	Pinouts.....	75
6.2.3.1	Fast internal RC Oscillator (FIRC) electrical specifications.....	31	9.1	Package pinouts and signal descriptions.....	75
6.2.3.2	Slow internal RC oscillator (SIRC) electrical specifications	31	10	Revision History.....	75
6.2.4	Low Power Oscillator (LPO) electrical specifications	32			

Description Input Multiplexing sheet(s) attached with Reference Manual.

	Parameter	S32K11x		S32K14x			
		K116	K118	K142	K144	K146	K148
System	Core	Arm® Cortex™-M0+		Arm® Cortex™-M4F			
	Frequency	48 MHz		80 MHz (RUN mode) or 112 MHz (HSRUN mode) ¹			
	IEEE-754 FPU	○		●			
	Cryptographic Services Engine (CSEc) ¹	●		●			
	CRC module	1x		1x			
	ISO 26262	capable up to ASIL-B		capable up to ASIL-B			
	Peripheral speed	up to 48 MHz		up to 112 MHz (HSRUN)			
	Crossbar	●		●			
	DMA	●		●			
	External Watchdog Monitor (EWM)	○		●			
	Memory Protection Unit (MPU)	●		●			
	FIRC CMU	●		○			
	Watchdog	1x		1x			
	Low power modes	●		●			
	HSRUN mode ¹	○		●			
	Number of I/Os	up to 43	up to 58	up to 89	up to 128	up to 156	
	Single supply voltage	2.7 - 5.5 V		2.7 - 5.5 V			
	Ambient Operation Temperature (T _A)	-40°C to +105°C / +125°C		-40°C to +105°C / +125°C			
Memory	Flash	128 KB	256 KB	256 KB	512 KB	1 MB	2 MB ²
	Error Correcting Code (ECC)	●		●			
	System RAM (including FlexRAM and MTB)	17 KB	25 KB	32 KB	64 KB	128 KB	256 KB
	FlexRAM (also available as system RAM)	2 KB		4 KB			
	Cache	○		4 KB			
	EEPROM emulated by FlexRAM ¹	2 KB (up to 32 KB D-Flash)		4 KB (up to 64 KB D-Flash)			See footnote 3
	External memory interface	○		○			QuadSPI incl. HyperBus™
Timer	Low Power Interrupt Timer (LPIT)	1x		1x			
	FlexTimer (16-bit counter) 8 channels	2x (16)		4x (32)	6x (48)	8x (64)	
	Low Power Timer (LPTMR)	1x		1x			
	Real Time Counter (RTC)	1x		1x			
	Programmable Delay Block (PDB)	1x		2x			
Analog	Trigger mux (TRGMUX)	1x (43)	1x (45)	1x (64)	1x (73)	1x (81)	
	12-bit SAR ADC (1 Msps each)	1x (13)	1x (16)	2x (16)	2x (24)	2x (32)	
	Comparator with 8-bit DAC	1x		1x			
Communication	10/100 Mbps IEEE-1588 Ethernet MAC	○		○			1x
	Serial Audio Interface (AC97, TDM, I2S)	○		○			2x
	Low Power UART/LIN (LPUART) (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A, and SAE J2602)	2x		2x	3x		
	Low Power SPI (LPSPPI)	1x	2x	2x	3x		
	Low Power I2C (LPI2C)	1x		1x			2x
	FlexCAN (CAN-FD ISO/CD 11898-1)	1x (1x with FD)		2x (1x with FD)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		1x			
IDEs	Debug & trace	SWD, MTB (1 KB), JTAG ⁴		SWD, JTAG (ITM, SWV, SWO)			SWD, JTAG (ITM, SWV, SWO), ETM
	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems		NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems			
Other	Packages ⁵	32-pin QFN 48-pin LQFP	48-pin LQFP 64-pin LQFP	64-pin LQFP 100-pin LQFP	64-pin LQFP 100-pin LQFP 100-pin MAPBGA	64-pin LQFP 100-pin MAPBGA 100-pin LQFP 144-pin LQFP	100-pin MAPBGA 144-pin LQFP 176-pin LQFP

LEGEND:

○ Not implemented

● Available on the device

1 No write or erase access to Flash module, including Security (CSEc) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.

2 Available when EEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.

3 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.

4 Only for Boundary Scan Register

5 See Dimensions section for package drawings

Figure 3. S32K1xx product series comparison

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	μs
	STOP1 → RUN	0.07	0.075	0.08	μs
	STOP2 → RUN	0.07	0.075	0.08	μs
	VLPR → RUN	19	—	26	μs
	VLPR → VLPS	5.1	5.7	6.5	μs
	VLPS → VLPR	18.8	23	27.75	μs
	RUN → Compute operation	0.72	0.75	0.77	μs
	HSRUN → Compute operation	0.3	0.31	0.35	μs
	RUN → STOP1	0.35	0.38	0.4	μs
	RUN → STOP2	0.2	0.23	0.25	μs
	RUN → VLPS	0.3	0.35	0.4	μs
	RUN → VLPR	3.5	3.8	5	μs
	VLPS → Asynchronous DMA Wakeup	105	110	125	μs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	Pin reset → Code execution	—	214	—	μs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes_Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table [Table 7](#). For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

Table 7. Power consumption (Typicals unless stated otherwise) 1 (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (μA) ²		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) ³		IDD/MHz (μA/MHz) ⁴
			Peripherals disabled ⁵	Peripherals enabled	Peripherals disabled ⁶	Peripherals enabled use case 1 ⁶	Peripherals enabled use case 2 ⁷			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
		Max	1637	1694	3.1	3.21	NA	12.7	13.7	25	32.9	30.7	38.8	36	43.8	NA		450
S32K144	25	Typ	29.8	42	1.48	1.50	2.91	7	7.7	19.7	26.9	25.1	33.3	30.2	39.6	43.3	55.6	378
	85	Typ	150	159	1.72	1.85	3.08	7.2	8.1	20.4	27.1	26.1	33.5	30.5	40	43.9	56.1	381
		Max	359	384	2.60	2.65	NA	9.2	9.9	23.2	29.6	29.3	36.2	34.8	42.1	46.3	59.7	435
	105	Typ	256	273	1.80	2.10	3.23	7.8	8.5	20.6	27.4	26.6	33.8	31.2	40.5	44.8	57.1	390
		Max	850	900	2.65	2.70	NA	10.3	11.1	23.9	30.6	30.3	37.3	35.6	43.5	47.9	61.3	445
	125	Typ	NA	NA	NA	NA	3.65	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	1960	1998	3.18	3.25	NA	12.9	13.8	26.9	33.6	35	40.3	38.7	46.8	NA		484
S32K146	25	Typ	37	47	1.57	1.61	3.3	8	9.2	23.4	31.4	30.5	40.2	36.2	47.6	52	68.3	452
	85	Typ	207	209	1.79	1.83	3.54	8.9	10.1	24.4	32.4	31.5	41.3	37.2	48.7	53.3	69.8	465
		Max	974	981	3.32	3.38	NA	12.7	13.9	29.3	37.9	36.7	47	42.4	54.4	60.3	78	530
	105	Typ	419	422	1.99	2.04	3.78	9.8	11	25.3	33.4	32.5	42.2	38.1	49.6	54.4	70.8	477
		Max	2004	2017	4.06	4.13	NA	17.1	18.3	34.1	42.6	41.3	51.4	46.9	58.8	65.7	82.8	587
	125	Typ	NA	NA	NA	NA	4.44	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3358	3380	5.28	5.38	NA	22.6	23.7	40.2	48.8	47.3	57.4	52.8	64.8	NA		660
S32K148 ⁸	25	Typ	38	54	2.17	2.20	3.45	8.5	9.6	27.6	34.9	35.5	45.3	42.1	57.7	60.3	83.3	526
	85	Typ	336	357	2.30	2.35	3.74	10.1	11.1	29.1	37.0	36.8	46.6	43.4	59.9	62.9	88.7	543

Table continues on the next page...

The following table shows the power consumption targets for S32K148 in various mode of operations measure at 3.3 V.

Table 9. Power consumption at 3.3 V

Chip/Device	Ambient Temperature (°C)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) ¹	
			Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI	Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI
S32K148	25	Typ	67.3	79.1	89.8	105.5
	85	Typ	67.4	79.2	95.6	105.9
		Max	82.5	88.2	109.7	117.4
	105	Typ	68.0	79.8	96.6	106.7
		Max	80.3	89.1	109.0	119.0
	125	Max	83.5	94.7	NA	

1. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.

4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	– 4000	4000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I _{LAT}	Latch-up current at ambient temperature of 125 °C	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

Table 14. AC electrical specifications at 5 V Range (continued)

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max.	Min.	Max.	
	1	17.3	54.8	17.6	59.7	200
		1.1	4.6	1.1	5.0	25
		2.0	5.7	2.0	5.8	50
		5.4	16.0	5.0	16.0	200
tRF _{GPIO-FAST}	0	0.42	2.2	0.37	2.2	25
		2.0	5.0	1.9	5.2	50
		9.3	18.8	8.5	19.3	200
	1	0.37	0.9	0.35	0.9	25
		1.2	2.7	1.2	2.9	50
		6.0	11.8	6.0	12.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 15. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C _{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to [External System Oscillator electrical specifications](#) for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 16. Device clock specifications 1

Symbol	Description	Min.	Max.	Unit
High Speed run mode ²				
f _{SYS}	System and core clock	—	112	MHz
f _{BUS}	Bus clock	—	56	MHz
f _{FLASH}	Flash clock	—	28	MHz
Normal run mode (S32K11x series)				
f _{SYS}	System and core clock	—	48	MHz
f _{BUS}	Bus clock	—	48	MHz

Table continues on the next page...

Table 18. External System Oscillator frequency specifications

Symbol	Description	Min.		Typ.		Max.		Unit	Notes
		S32K14x	S32K11x	S32K14x	S32K11x	S32K14x	S32K11x		
f _{osc_hi}	Oscillator crystal or resonator frequency	4		—		40		MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—		—		50	48	MHz	1
t _{dc_extal}	Input clock duty cycle (external clock mode)	48		50		52		%	1
t _{cst}	Crystal Start-up Time								
	8 MHz low-gain mode (HGO=0)	—		1.5		—		ms	2
	8 MHz high-gain mode (HGO=1)	—		2.5		—			
	40 MHz low-gain mode (HGO=0)	—		2		—			
	40 MHz high-gain mode (HGO=1)	—		2		—			

1. Frequencies below 40 MHz can be used for degraded duty cycle upto 40-60%
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.4 Low Power Oscillator (LPO) electrical specifications

Table 21. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F _{LPO}	Internal low power oscillator frequency	113	128	139	kHz
T _{startup}	Startup Time	—	—	20	μs

6.2.5 SPLL electrical specifications

Table 22. SPLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F _{SPLL_REF} ¹	PLL Reference Frequency Range	8	—	16	MHz
F _{SPLL_Input} ²	PLL Input Frequency	8	—	40	MHz
F _{VCO_CLK}	VCO output frequency	180	—	320	MHz
F _{SPLL_CLK}	PLL output frequency	90	—	160	MHz
J _{CYC_SPLL}	PLL Period Jitter (RMS) ³				
	at F _{VCO_CLK} 180 MHz	—	120	—	ps
	at F _{VCO_CLK} 320 MHz	—	75	—	ps
J _{ACC_SPLL}	PLL accumulated jitter over 1μs (RMS) ³				
	at F _{VCO_CLK} 180 MHz	—	1350	—	ps
	at F _{VCO_CLK} 320 MHz	—	600	—	ps
D _{UNL}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%
T _{SPLL_LOCK}	Lock detector detection time ⁴	—	—	150 × 10 ⁻⁶ + 1075(1/F _{SPLL_REF})	s

1. F_{SPLL_REF} is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLLCFG register of Reference Manual.
2. F_{SPLL_Input} is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

6.3 Memory and memory interfaces

6.3.1 Flash memory module (FTFC) electrical specifications

This section describes the electrical characteristics of the flash memory module.

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit	Notes
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
t _{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t _{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
t _{eewr16b}	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
t _{eewr32bers}	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	μs	
t _{eewr32b}	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	μs	3,4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
t _{quickwr}	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	μs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

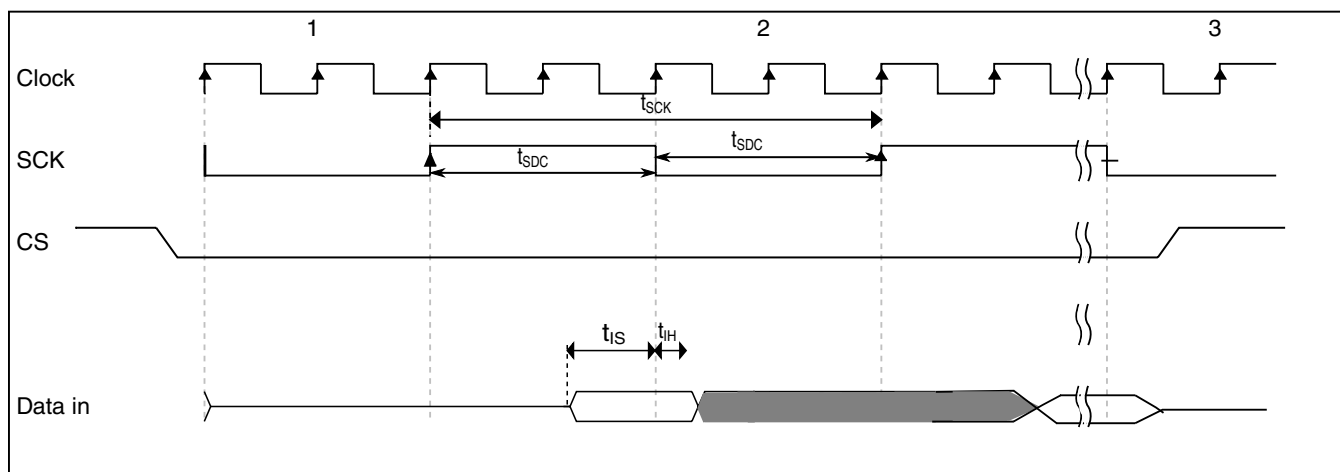


Figure 9. QuadSPI input timing (SDR mode) diagram

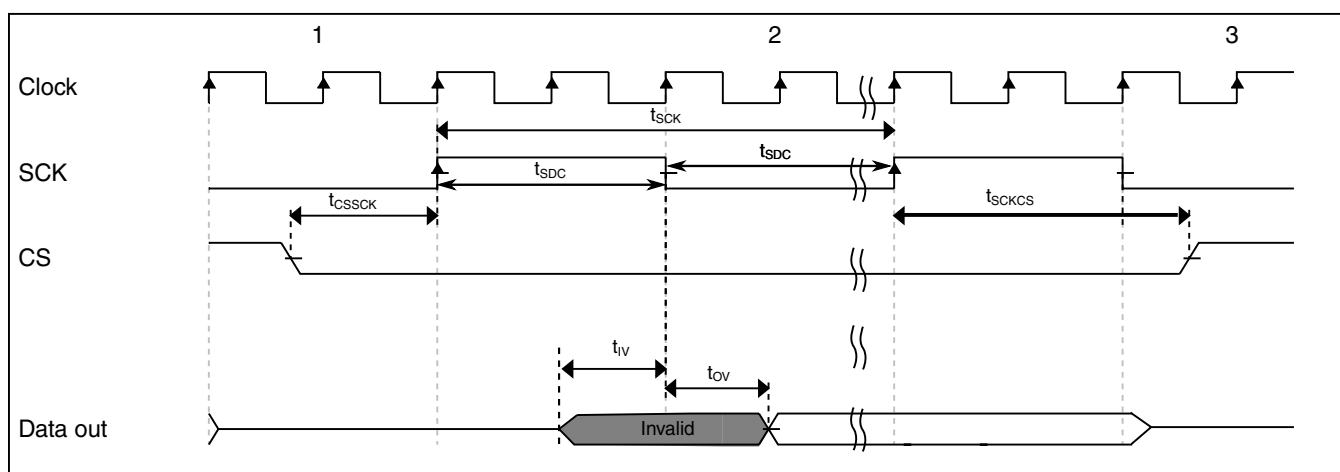
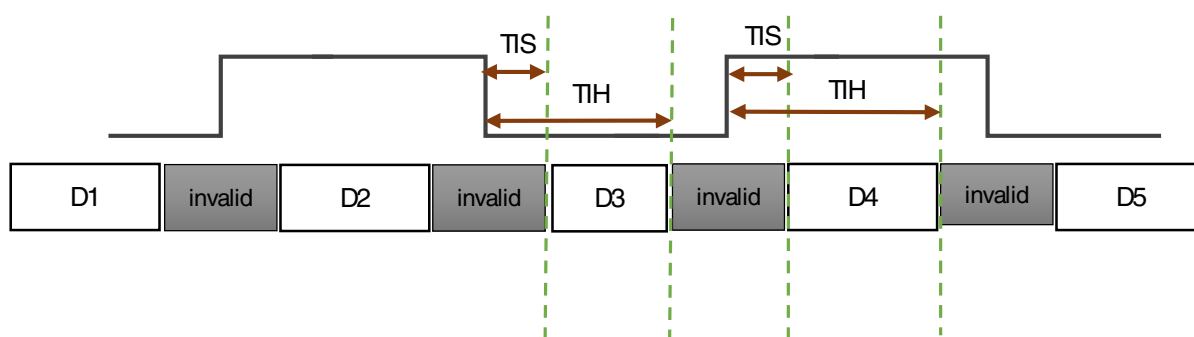


Figure 10. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time

TIH – Hold Time

Figure 11. QuadSPI input timing (HyperRAM mode) diagram

6.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See [AN5426](#) for details

Table 28. 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
V_{DDA}	Supply voltage		2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC		—	0.6	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the <i>Reference Manual</i>	ns	
TUE ⁴	Total unadjusted error		—	±4	±8	LSB ⁵	6, 7, 8, 9
DNL	Differential non-linearity		—	±1.0	—	LSB ⁵	6, 7, 8, 9
INL	Integral non-linearity		—	±2.0	—	LSB ⁵	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}=V_{DD}$, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume $V_{DDA} = 3\text{ V}$, Temp = 25 °C, $f_{ADCK} = 40\text{ MHz}$, $R_{AS}=20\ \Omega$, and $C_{AS}=10\text{ nF}$.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

Table 29. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the <i>Reference Manual</i>	ns	
TUE ⁴	Total unadjusted error		—	±4	±8	LSB ⁵	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB ⁵	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB ⁵	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}=V_{DD}$, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 40$ MHz, $R_{AS}=20$ Ω, and $C_{AS}=10$ nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

6.4.2 CMP with 8-bit DAC electrical specifications

Table 31. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DDHS}	Supply current, High-speed mode ¹				μA
	-40 - 125 °C	—	230	300	
I _{DDL}	Supply current, Low-speed mode ¹				μA
	-40 - 105 °C	—	6	11	
	-40 - 125 °C		6	13	
V _{AIN}	Analog input voltage	0	0 - V _{DDA}	V _{DDA}	V
V _{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
V _{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
t _{DHSB}	Propagation delay, High-speed mode ²				ns
	-40 - 105 °C	—	35	200	
	-40 - 125 °C		35	300	
t _{DL}	Propagation delay, Low-speed mode ²				μs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
t _{DH}	Propagation delay, High-speed mode ³				ns
	-40 - 105 °C	—	70	400	
	-40 - 125 °C	—	70	500	
t _{DL}	Propagation delay, Low-speed mode ³				μs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
t _{IDH}	Initialization delay, High-speed mode ⁴				μs
	-40 - 125 °C	—	1.5	3	
t _{IDL}	Initialization delay, Low-speed mode ⁴				μs
	-40 - 125 °C	—	10	30	
V _{HYST0}	Analog comparator hysteresis, Hyst0				mV
	-40 - 125 °C	—	0	—	
V _{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 °C	—	19	66	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 °C	—	15	40	
V _{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 °C	—	34	133	

Table continues on the next page...

Table 31. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	—	23	80	
V _{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	—	46	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	—	32	120	
I _{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	μA
	5V Reference Voltage	—	10	16	μA
INL ⁵	8-bit DAC integral non-linearity	−0.75	—	0.75	LSB ⁶
DNL	8-bit DAC differential non-linearity	−0.5	—	0.5	LSB ⁶
t _{DDAC}	Initialization and switching settling time	—	—	30	μs

1. Difference at input > 200mV
2. Applied $\pm (100 \text{ mV} + V_{\text{HYST0}/1/2/3+ \text{ max. of } V_{\text{AIO}})$ around switch point.
3. Applied $\pm (30 \text{ mV} + 2 \times V_{\text{HYST0}/1/2/3+ \text{ max. of } V_{\text{AIO}})$ around switch point.
4. Applied $\pm (100 \text{ mV} + V_{\text{HYST0}/1/2/3})$.
5. Calculation method used: Linear Regression Least Square Method
6. $1 \text{ LSB} = V_{\text{reference}}/256$

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

Table 32. LPSPI electrical specifications¹ (continued)

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
8	t _a	Slave access time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
9	t _{dis}	Slave MISO (SOUT) disable time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
10	t _v	Data valid (after SPSCCK edge)	Slave	-	30	-	39	-	26	-	36 ¹¹ 31 ¹²	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback ⁵	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow) ⁶	-	8	-	10	-	7	-	9	-	44	-	44	
11	t _{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback ⁵	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	
			Master Loopback(slow) ⁶	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	t _{RI/FI}	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		
			Master Loopback ⁵	-		-		-		-		-		-		
			Master Loopback(slow) ⁶	-		-		-		-		-		-		
13	t _{RO/FO}	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		
			Master Loopback ⁵	-		-		-		-		-		-		

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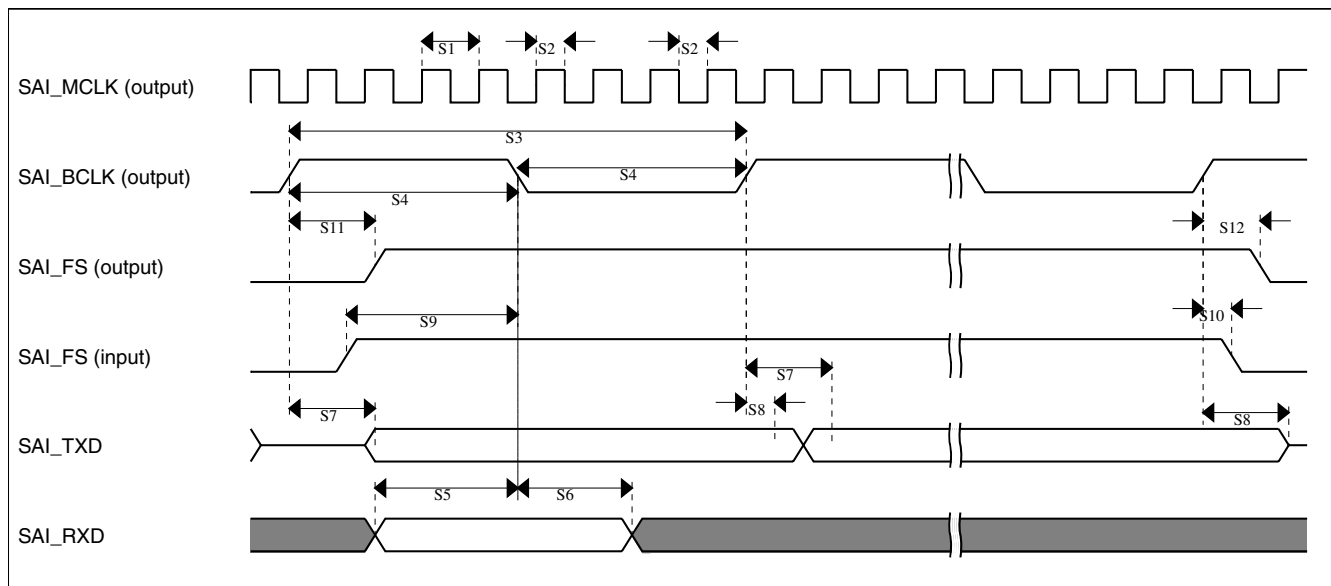


Figure 22. SAI Timing — Master modes

Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14 ¹	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Package Top ⁷	Natural Convection	ψ_{JT}	32	1	NA	NA	NA	NA	NA	
			48	4	2	NA	NA	NA	NA	
			64	NA	2	2	2	2	NA	
			100	NA	NA	2	2	2	NA	
			144	NA	NA	NA	NA	2	1	
			176	NA	NA	NA	NA	NA	1	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J , can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated values for V_{REFH} and V_{REFL} to add reference to the section "voltage and current operating requirements" for Min and Max values - Updated footnote to Typ. - Removed footnote from RAS Analog source resistance - Updated figure: ADC input impedance equivalency diagram - In table: 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Removed rows for V_{TEMP_S} and V_{TEMP25} - Updated footnote to Typ. - In table: 12-bit ADC characteristics (3 V to 5.5 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Removed rows for V_{TEMP_S} and V_{TEMP25} - Removed number for TUE - Updated footnote to Typ. - In table: Comparator with 8-bit DAC electrical specifications - Updated Typ. of I_{DDL5} Supply current, Low-speed mode - Updated Typ. of t_{DLSB} Propagation delay, Low-speed mode - Updated Typ. of t_{DHSS} Propagation delay, High-speed mode - Updated t_{DLSS} Propagation delay - Added row for t_{DDAC} Initialization and switching settling time - Updated footnote - Updated section LPSPi electrical specifications - Added section: SAI electrical specifications - Updated section: Ethernet AC specifications - Added section: Clockout frequency - Added section: Trace electrical specifications - Updated table: Table 41 : Updated numbers for S32K142 and S32K148 - Updated table: Table 42 : Updated numbers for S32K148 - Updated Document number for 32-pin QFN in topic Obtaining package dimensions
3	14 March 2017	- In Table 2 - Updated min. value of V_{DD_OFF} - Added parameter I_{INJSUM_AF} - Updated Power mode transition operating behaviors - Updated Power consumption - Updated footnote to T_{SPLL_LOCK} in SPLL electrical specifications - In 12-bit ADC electrical characteristics - Updated table: 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Added typ. value to I_{DDA_ADC}, TUE, DNL, and INL - Added min. value to SMPLTS - Removed footnote 'All the parameters in this table ... ' - Updated table: 12-bit ADC characteristics (3 V to 5.5 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Added typ. value to I_{DDA_ADC} - Removed footnote 'All the parameters in this table ... ' - In Flash timing specifications — commands updated Max. value of t_{Vfykey} to 33 μs
4	02 June 2017	- In section: Block diagram, added block diagram for S32K11x series. - Updated figure: S32K1xx product series comparison. - In section: Selecting orderable part number , added reference to attachment S32K_Part_Numbers.xlsx. - In section: Ordering information - Updated figure: Ordering information. - In Table 1,

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Table 43. Revision History

Rev. No.	Date	Substantial Changes
		- Added footnote 'For S32K11x – FIRC/SOSC/FIRC/LPO; For S32K14x – FIRC/SOSC/FIRC/LPO/SPLL' to 'VLPS Mode: All clock sources disabled' - Updated numbers for: - VLPR → VLPS - VLPS → VLPR 'RUN → Compute operation' - RUN → VLPS - RUN → VLPR - In Power consumption : - Updated specs for S32K142, S32K144, and S32K148 - Updated footnote 'Typical current numbers are indicative ...' - Updated footnote 'The S32K148 data ...' - Removed footnote 'Above S32K148 data is preliminary targets only' - Added new table 'Power consumption at 3.3 V' - In General AC specifications : - Updated max value and footnote of WFRST - Updated symbol for not filtered pulse to 'WNFRST', updated min value, removed max. value, and added footnote - Fixed naming conventions to align with DS in DC electrical specifications at 3.3 V Range and DC electrical specifications at 5.0 V Range - Updated specs for AC electrical specifications at 3.3 V range and AC electrical specifications at 5 V range - In Device clock specifications : - Updated f_{BUS} to 48 for 11x - Added footnote to f_{BUS} for 14x - In External System Oscillator frequency specifications : - Added specs for S32K11x - Updated 't_{dc_extal}' for S32K14x - Added footnote 'Frequencies below ...' to 'f_{ec_extal}' and 't_{dc_extal}' - Splitted Flash timing specifications — commands for S32K14x and S32K11x - Updated Flash timing specifications — commands for S32K14x - In Reliability specifications : - Added footnote 'Data retention period ...' for 'tnvmretp1k' and 'tnvmreteet' - Minor update in footnote for 'nnvmwree16' 'nnvmwree256' - In QuadSPI AC specifications : - Updated 'MCR[SCLKCFG[5]]' value to 0 - Updated 'Data Input Setup Time' HSRUN Internal DQS PAD Loopback value to 1.6 - Updated 'Data Input Setup Time' DDR External DQS min. value to 2 - Updated 'Data Input Hold Time' DDR External DQS min. value to 20 - Updated figure 'QuadSPI output timing (SDR mode) diagram' and 'QuadSPI input timing (HyperRAM mode) diagram' - In 12-bit ADC electrical characteristics : - Added note 'On reduced pin packages where ...' - Removed max. value of 'I_{DDA_ADC}' - Added note 'Due to triple ...' - In 12-bit ADC operating conditions, removed parameter 'ΔV_{DDA}' - In CMP with 8-bit DAC electrical specifications : - Updated Typ. and Max. values of 'I_{DDL5}' - Updated Typ. value of 't_{DHSB}' - Updated Typ. value of 'V_{HYST1}', 'V_{HYST2}', and 'V_{HYST3}' - In LPSPFI electrical specifications : - Updated 'f_{periph}' and 'f_{op}', and 't_{SPSCK}'

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