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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mnt0vlhr

- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
  - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
  - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
  - 128-bit Unique Identification (ID) number
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - System Memory Protection Unit (System MPU)
  - Cyclic Redundancy Check (CRC) module
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
- Timing and control
  - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- Package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

Description Input Multiplexing sheet(s) attached with Reference Manual.

		S32K11x		S32K14x			
	Parameter	K116	K118	K142	K144	K146	K148
	Core	Arm® Cortex™-M0+		Arm® Cortex™-M4F			
	Frequency	48 MHz		80 MHz (RUN mode) or 112 MHz (HSRUN mode)[1]			
System	IEEE-754 FPU	○		●			
System	Cryptographic Services Engine (CSEc)[1]	●		●			
System	CRC module	1x		1x			
System	ISO 26262	capable up to ASIL-B		capable up to ASIL-B			
System	Peripheral speed	up to 48 MHz		up to 112 MHz (HSRUN)			
System	Crossbar	●		●			
System	DMA	●		●			
System	External Watchdog Monitor (EWM)	○		●			
System	Memory Protection Unit (MPU)	●		●			
System	FIRC CMU	●		○			
System	Watchdog	1x		1x			
System	Low power modes	●		●			
System	HSRUN mode[1]	○		●			
System	Number of I/Os	up to 43	up to 58	up to 89		up to 128	up to 156
System	Single supply voltage	2.7 - 5.5 V		2.7 - 5.5 V			
System	Ambient Operation Temperature (T_A)	-40ºC to +105ºC / +125ºC		-40ºC to +105ºC / +125ºC			
Memory	Flash	128 KB	256 KB	256 KB	512 KB	1 MB	2 MB[2]
Memory	Error Correcting Code (ECC)	●		●			
Memory	System RAM (including FlexRAM and MTB)	17 KB	25 KB	32 KB	64 KB	128 KB	256 KB
Memory	FlexRAM (also available as system RAM)	2 KB		4 KB			
Memory	Cache	○		4 KB			
Memory	EEPROM emulated by FlexRAM[1]	2 KB (up to 32 KB D-Flash)		4 KB (up to 64 KB D-Flash)			See footnote 3
Memory	External memory interface	○		○			QuadSPI incl. HyperBus™
Timer	Low Power Interrupt Timer (LPIT)	1x		1x			
Timer	FlexTimer (16-bit counter) 8 channels	2x (16)		4x (32)		6x (48)	8x (64)
Timer	Low Power Timer (LPTMR)	1x		1x			
Timer	Real Time Counter (RTC)	1x		1x			
Timer	Programmable Delay Block (PDB)	1x		2x			
Analog	Trigger mux (TRGMUX)	1x (43)	1x (45)	1x (64)		1x (73)	1x (81)
Analog	12-bit SAR ADC (1 Msps each)	1x (13)	1x (16)	2x (16)		2x (24)	2x (32)
Analog	Comparator with 8-bit DAC	1x		1x			
Communication	10/100 Mbps IEEE-1588 Ethernet MAC	○		○			1x
Communication	Serial Audio Interface (AC97, TDM, I2S)	○		○			2x
Communication	Low Power UART/LIN (LPUART) (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A, and SAE J2602)	2x		2x	3x		
Communication	Low Power SPI (LPSPI)	1x	2x	2x	3x		
Communication	Low Power I2C (LPI2C)	1x		1x			2x
Communication	FlexCAN (CAN-FD ISO/CD 11898-1)	1x (1x with FD)		2x (1x with FD)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
Communication	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		1x			
IDEs	Debug & trace	SWD, MTB (1 KB), JTAG[4]		SWD, JTAG (ITM, SWV, SWO)			SWD, JTAG (ITM, SWV, SWO), ETM
IDEs	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems		NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems			
Other	Packages[5]	32-pin QFN 48-pin LQFP	48-pin LQFP 64-pin LQFP	64-pin LQFP 100-pin LQFP	64-pin LQFP 100-pin LQFP 100-pin MAPBGA	64-pin LQFP 100-pin MAPBGA 100-pin LQFP 144-pin LQFP	100-pin MAPBGA 144-pin LQFP 176-pin LQFP

LEGEND:
- ○ Not implemented
- ● Available on the device

1 No write or erase access to Flash module, including Security (CSEc) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.
2 Available when EEEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
3 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.
4 Only for Boundary Scan Register
5 See Dimensions section for package drawings

Figure 3. S32K1xx product series comparison

5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
6. Open drain outputs must be pulled to V_{DD}.
7. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.

4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP, 100 LQFP, and 100 MAP-BGA packages.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	85[1]	℃
$T_{J\ C\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	105[1]	℃
$T_{A\ V\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	105[1]	℃
$T_{J\ V\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	125[1]	℃
$T_{A\ M\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	125[2]	℃
$T_{J\ M\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	135[2]	℃

1. Values mentioned are measured at ≤ 112 MHz in HSRUN mode.
2. Values mentioned are measured at ≤ 80 MHz in RUN mode.

Table 5. V_{DD} supply LVR, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- RUN Mode:
  - Clock source: FIRC
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
  - FLASH_CLK = 24 MHz
- HSRUN Mode:
  - Clock source: SPLL
  - SYS_CLK/CORE_CLK = 112 MHz
  - BUS_CLK = 56 MHz
  - FLASH_CLK = 28 MHz
- VLPR Mode:
  - Clock source: SIRC
  - SYS_CLK/CORE_CLK = 4 MHz
  - BUS_CLK = 4 MHz
  - FLASH_CLK = 1 MHz
- STOP1/STOP2 Mode:
  - Clock source: FIRC
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
  - FLASH_CLK = 24 MHz
- VLPS Mode: All clock sources disabled [1]

Table 6. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	µs

Table continues on the next page...

1. • For S32K11x – FIRC/SOSC
   • For S32K14x – FIRC/SOSC/SPLL

Table 7. Power consumption (Typicals unless stated otherwise) 1 (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (µA) [2]		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [3]		IDD/MHz (µA/MHz) [4]
			Peripherals disabled [5]	Peripherals enabled	Peripherals disabled [6]	Peripherals enabled use case 1[6]	Peripherals enabled use case 2[7]			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
		Max	1660	1736	3.48	3.55	NA	14.5	15.6	34.8	43.6	41.9	53.9	48.7	65.1	70.4	96.1	609
	105	Typ	560	577	2.49	2.54	4.03	10.9	11.9	29.8	37.8	37.6	47.5	45.2	61.5	63.8	89.1	565
		Max	2945	2970	4.40	4.47	NA	18.0	19.0	38.4	46.8	44.9	55.3	51.6	66.8	73.6	97.4	645
	125	Typ	NA	NA	NA	NA	4.85	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3990	4166	6.00	6.08	NA	23.4	24.5	44.3	52.5	50.9	61.3	57.5	71.6	NA		719

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and On-chip pulldown is enabled for all unused input pins.
2. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
3. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
4. Values mentioned for S32K14x devices are measured at RUN@80 MHz with peripherals disabled and values mentioned for S32K11x devices are measured at RUN@48 MHz with peripherals disabled.
5. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
6. Data collected using RAM
7. Numbers on limited samples size and data collected with Flash
8. The S32K148 data points assume that ENET/QuadSPI/SAI etc. are inactive.

6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
7. When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
8. Measured at input V = V_{SS}
9. Measured at input V = V_{DD}

5.4 DC electrical specifications at 5.0 V Range

Table 12. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh}= (V_{DD} - 0.8 V)	5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	5	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = V_{DD} - 0.8 V	20	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	20	—	—	mA	3
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	14.0	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	14.5	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	21	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	20.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					5
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	6
R_{PD}	Internal pulldown resistors	20		50	kΩ	7

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
4. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

6.2.3 System Clock Generation (SCG) specifications

6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 19. Fast internal RC Oscillator electrical specifications

Symbol	Parameter[1]	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	$\%F_{FIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		3.4	5	µs[2]
T_{JIT}, [3]	Cycle-to-Cycle jitter	—	300	500	ps
T_{JIT}[3]	Long term jitter over 1000 cycles	—	0.04	0.1	$\%F_{FIRC}$

1. With FIRC regulator enable
2. Startup time is defined as the time between clock enablement and clock availability for system use.
3. FIRC as system clock

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 20. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	—	±3	$\%F_{SIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	—	±3.3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	9	12.5	µs[1]

1. Startup time is defined as the time between clock enablement and clock availability for system use.

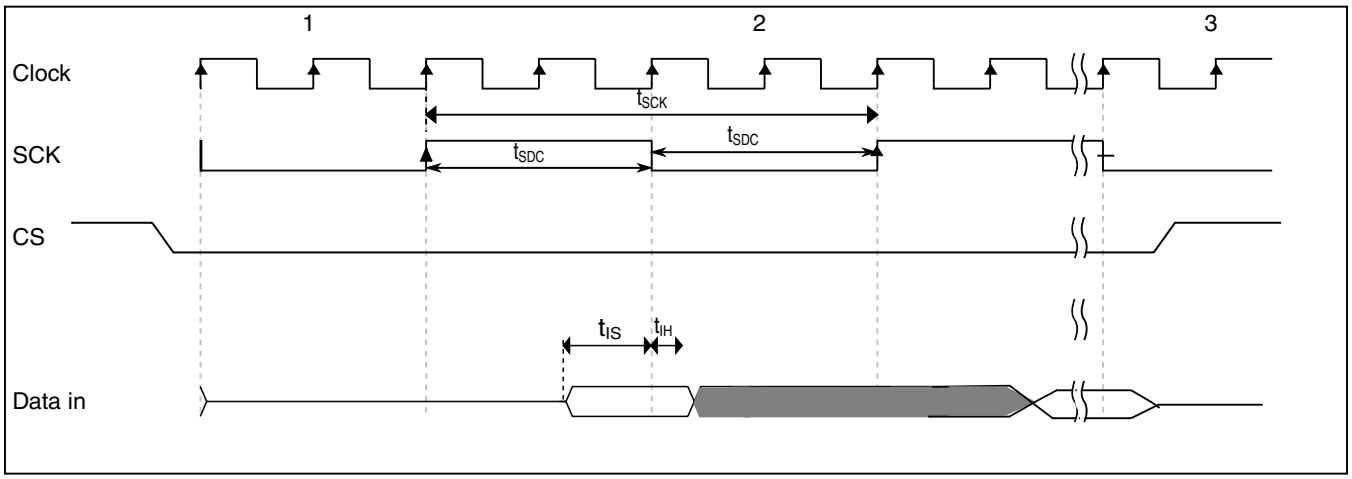


Figure 9. QuadSPI input timing (SDR mode) diagram

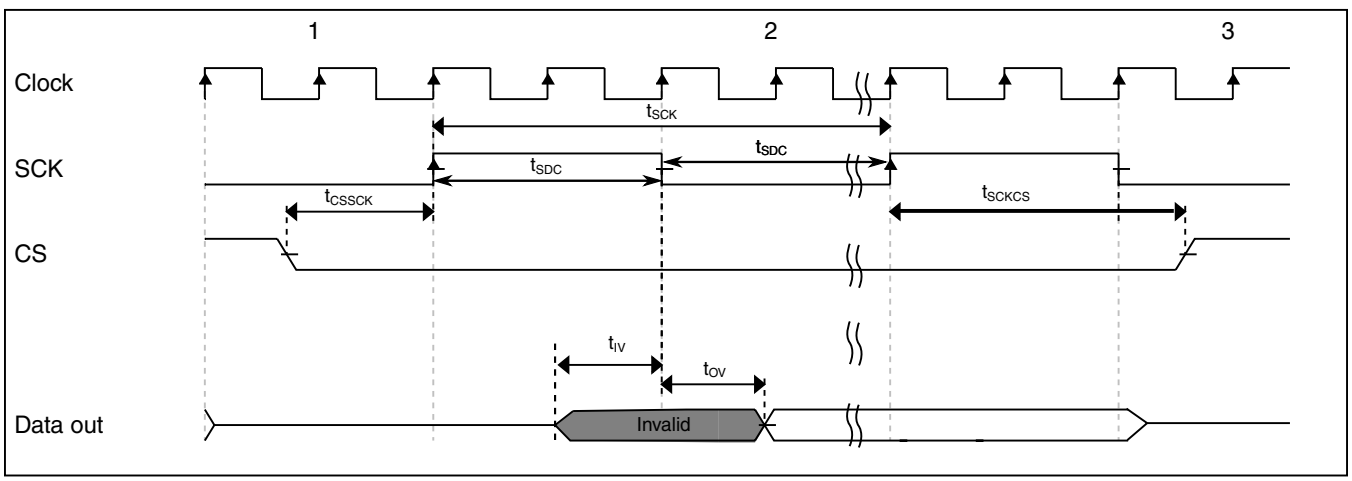
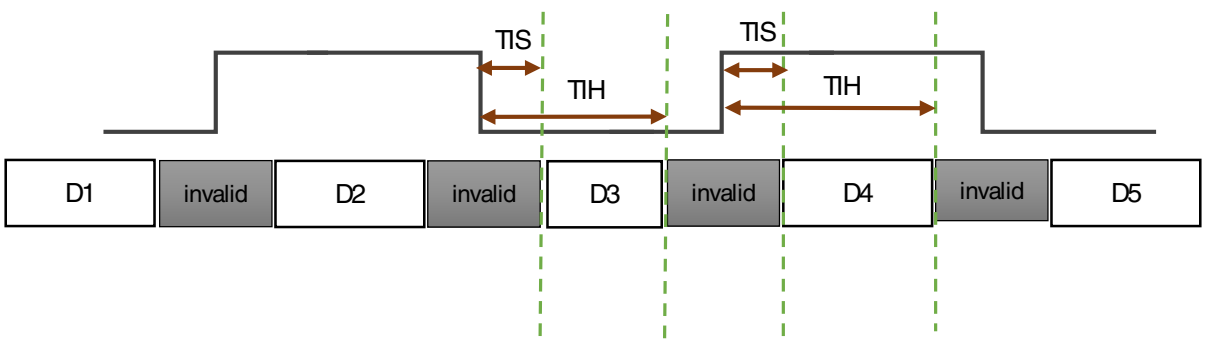


Figure 10. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time
TIH – Hold Time

Figure 11. QuadSPI input timing (HyperRAM mode) diagram

Table 27. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
f_{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	MHz	3, 4
f_{CONV}	ADC conversion frequency	No ADC hardware averaging.[5] Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	6, 7
		ADC hardware averaging set to 32. [5] Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	6, 7

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual* .
4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. Numbers based on the minimum sampling time of 275 ns.
7. For guidelines and examples of conversion rate calculation, see the *Reference Manual* section 'Calibration function'

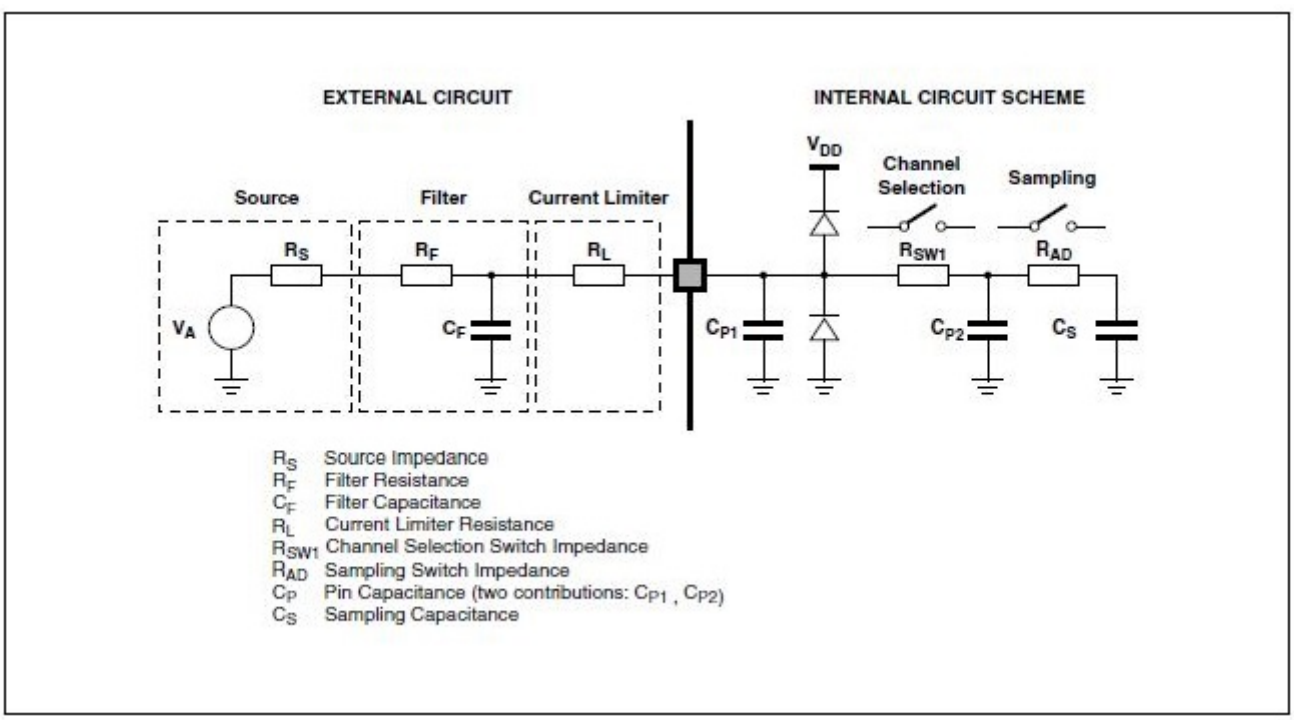


Figure 13. ADC input impedance equivalency diagram

6.4.2 CMP with 8-bit DAC electrical specifications

Table 31. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode[1]				µA
	-40 - 125 °C	—	230	300	
I_{DDLS}	Supply current, Low-speed mode[1]				µA
	-40 - 105 °C	—	6	11	
	-40 - 125 °C		6	13	
V_{AIN}	Analog input voltage	0	0 - V_{DDA}	V_{DDA}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[2]				ns
	-40 - 105 °C	—	35	200	
	-40 - 125 °C		35	300	
t_{DLSB}	Propagation delay, Low-speed mode[2]				µs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
t_{DHSS}	Propagation delay, High-speed mode[3]				ns
	-40 - 105 °C	—	70	400	
	-40 - 125 °C	—	70	500	
t_{DLSS}	Propagation delay, Low-speed mode[3]				µs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode[4]				µs
	-40 - 125 °C	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[4]				µs
	-40 - 125 °C	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0				mV
	-40 - 125 °C	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 °C	—	19	66	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 °C	—	15	40	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 °C	—	34	133	

Table continues on the next page...

Table 31. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	—	23	80	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	—	46	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	—	32	120	
I_{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL[5]	8-bit DAC integral non-linearity	–0.75	—	0.75	LSB[6]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB[6]
t_{DDAC}	Initialization and switching settling time	—	—	30	µs

1. Difference at input > 200mV
2. Applied ± (100 mV + $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
3. Applied ± (30 mV + 2 × $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
4. Applied ± (100 mV + $V_{HYST0/1/2/3}$).
5. Calculation method used: Linear Regression Least Square Method
6. 1 LSB = $V_{reference}$/256

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

6.5.4 FlexCAN electical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

6.5.5 SAI electrical specifications

The following table describes the SAI electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 33. Master mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	—	ns
S4	SAI_BCLK pulse width high/low	45%	55%	BCLK period
S5	SAI_RXD input setup before SAI_BCLK	28	—	ns
S6	SAI_RXD input hold after SAI_BCLK	0	—	ns
S7	SAI_BCLK to SAI_TXD output valid	—	8	ns
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	ns
S9	SAI_FS input setup before SAI_BCLK	28	—	ns
S10	SAI_FS input hold after SAI_BCLK	0	—	ns
S11	SAI_BCLK to SAI_FS output valid	—	8	ns
S12	SAI_BCLK to SAI_FS output invalid	-2	—	ns

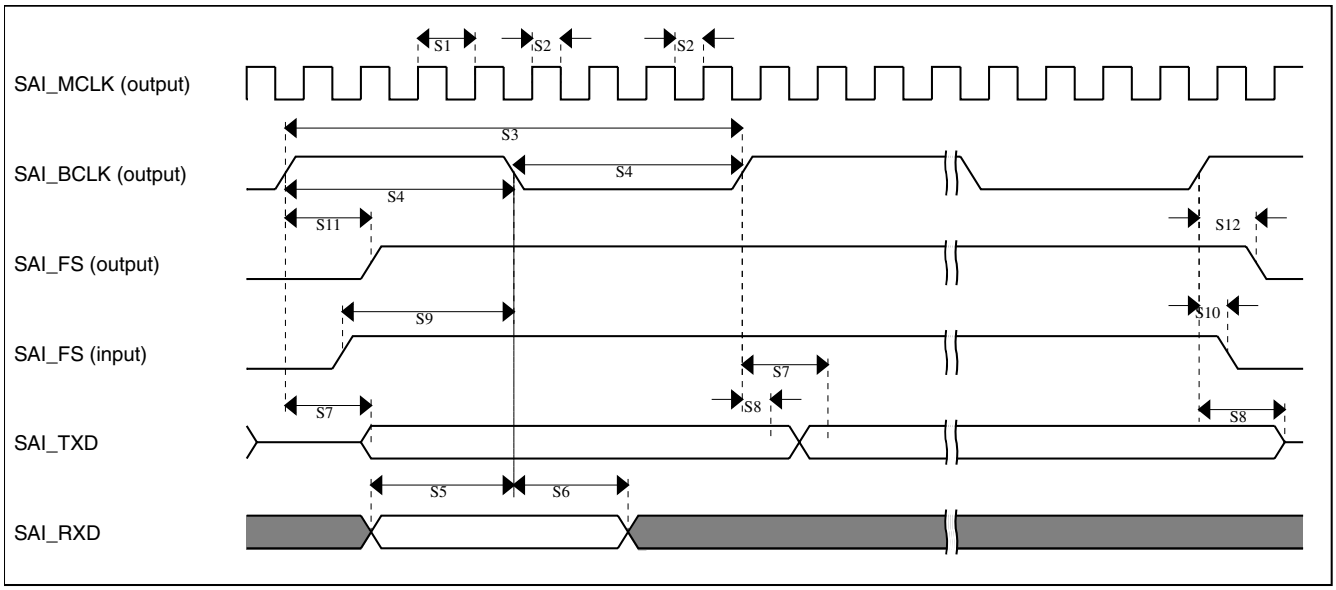


Figure 22. SAI Timing — Master modes

Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14[1]	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

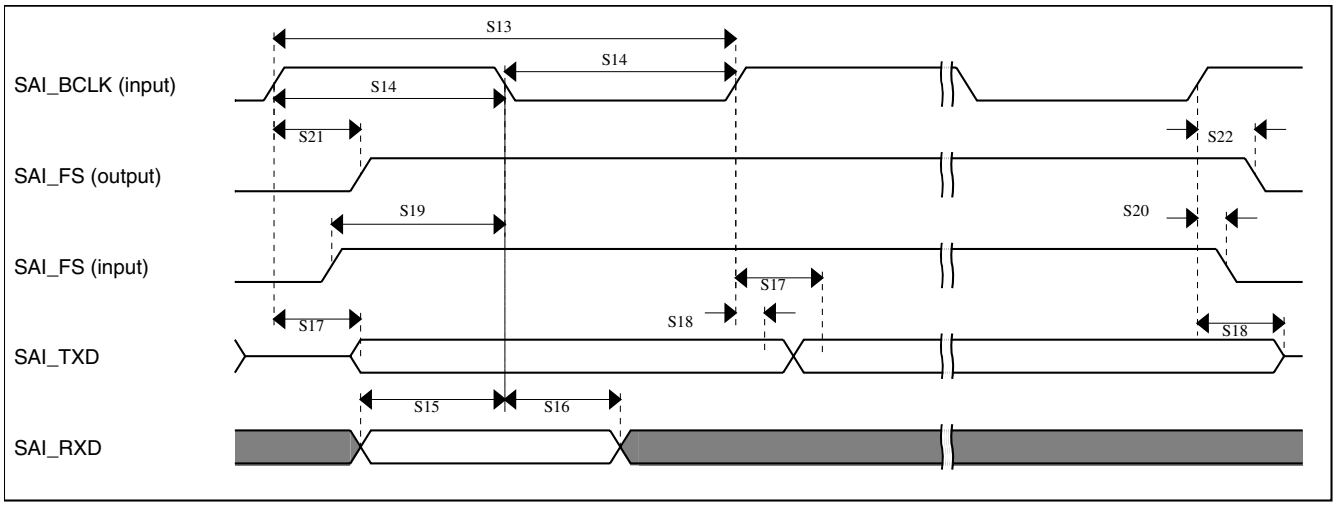


Figure 23. SAI Timing — Slave modes

6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 35. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

Table 37. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

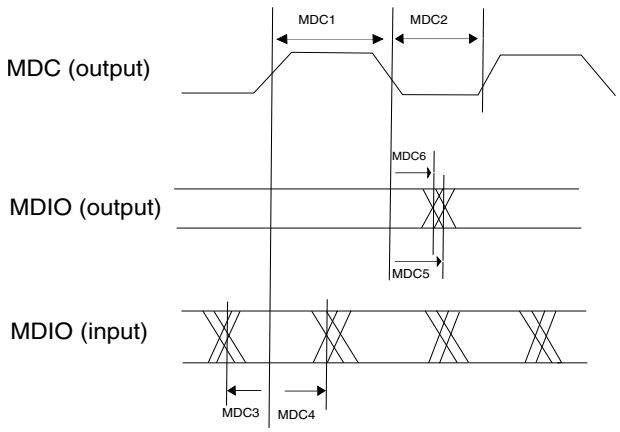


Figure 28. MII/RMII serial management channel timing diagram

6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specofications

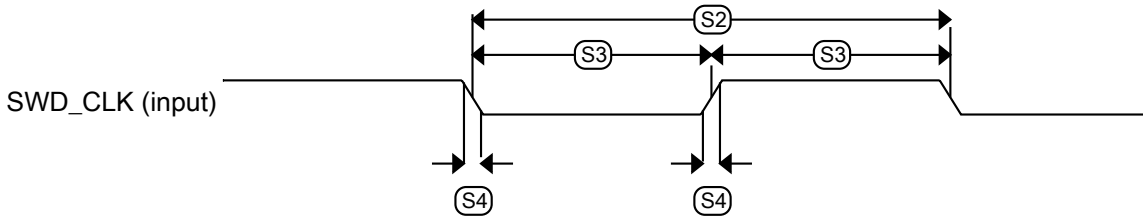


Figure 29. Serial wire clock input timing

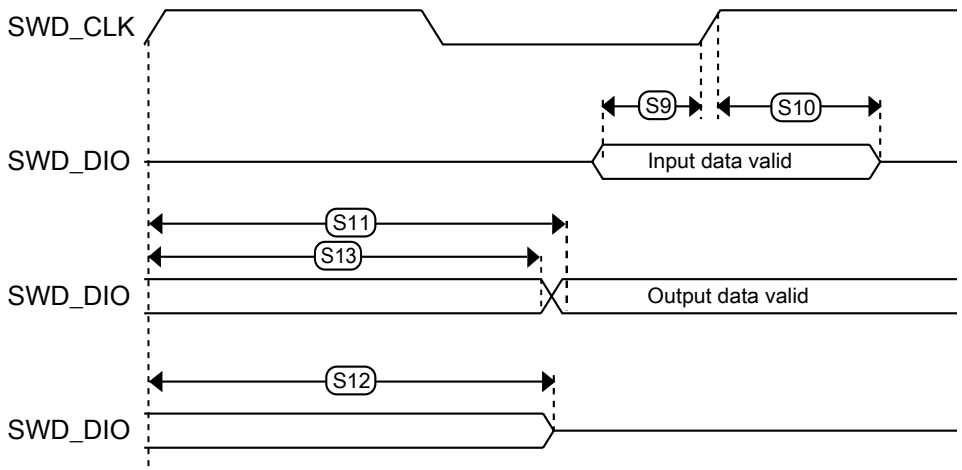


Figure 30. Serial wire data timing

6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 39. Trace specifications

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
—	Fsys	System frequency	80	48	40	112	80	4	MHz

Table continues on the next page...

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
			144	NA	NA	NA	NA	37	31	
			176	NA	NA	NA	NA	NA	30	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	32	26	NA	NA	NA	NA	NA	
			48	48	41	NA	NA	NA	NA	
			64	NA	37	36	36	35	NA	
			100	NA	NA	34	34	33	NA	
			144	NA	NA	NA	NA	36	30	
			176	NA	NA	NA	NA	NA	29	
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	32	11	NA	NA	NA	NA	NA	
			48	33	24	NA	NA	NA	NA	
			64	NA	26	25	25	23	NA	
			100	NA	NA	25	25	24	NA	
			144	NA	NA	NA	NA	30	24	
			176	NA	NA	NA	NA	NA	24	
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	32	NA	NA	NA	NA	NA	NA	
			48	23	19	NA	NA	NA	NA	
			64	NA	14	13	12	11	NA	
			100	NA	NA	13	12	11	NA	
			144	NA	NA	NA	NA	12	9	
			176	NA	NA	NA	NA	NA	9	
Thermal resistance, Junction to Case (Bottom) [6]	—	$R_{\theta JCBottom}$	32	1	NA					
			48	NA						
			64							
			100							
			144							
			176							

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes

		• Added footnote 'For S32K11x – FIRC/SOSC/FIRC/LPO; For S32K14x – FIRC/SOSC/FIRC/LPO/SPLL' to 'VLPS Mode: All clock sources disabled'
		• Updated numbers for:
		  • VLPR → VLPS
		  • VLPS → VLPR
		  • 'RUN → Compute operation'
		  • RUN → VLPS
		  • RUN → VLPR
		• In Power consumption :
		  • Updated specs for S32K142, S32K144, and S32K148
		  • Updated footnote 'Typical current numbers are indicative ...'
		  • Updated footnote 'The S32K148 data ...'
		  • Removed footnote 'Above S32K148 data is preliminary targets only'
		  • Added new table 'Power consumption at 3.3 V'
		• In General AC specifications :
		  • Updated max value and footnote of WFRST
		  • Updated symbol for not filtered pulse to 'WNFRST', updated min value, removed max. value, and added footnote
		• Fixed naming conventions to align with DS in DC electrical specifications at 3.3 V Range and DC electrical specifications at 5.0 V Range
		• Updated specs for AC electrical specifications at 3.3 V range and AC electrical specifications at 5 V range
		• In Device clock specifications :
		  • Updated f_{BUS} to 48 for 11x
		  • Added footnote to f_{BUS} for 14x
		• In External System Oscillator frequency specifications :
		  • Added specs for S32K11x
		  • Updated 't_{dc_extal}' for S32K14x
		  • Added footnote 'Frequecies below ... ' to 'f_{ec_extal}' and 't_{dc_extal}'
		• Splitted Flash timing specifications — commands for S32K14x and S32K11x
		• Updated Flash timing specifications — commands for S32K14x
		• In Reliability specifications :
		  • Added footnote 'Data retention period ... ' for 'tnvmretp1k' and 'tnvmretee'
		  • Minor update in footnote for 'nnvmwree16' 'nnvmwree256'
		• In QuadSPI AC specifications :
		  • Updated 'MCR[SCLKCFG[5]]' value to 0
		  • Updated 'Data Input Setup Time' HSRUN Internal DQS PAD Loopback value to 1.6
		  • Updated 'Data Input Setup Time' DDR External DQS min. value to 2
		  • Updated 'Data Input Hold Time' DDR External DQS min. value to 20
		  • Upadted figure 'QuadSPI output timing (SDR mode) diagram' and 'QuadSPI input timing (HyperRAM mode) diagram'
		• In 12-bit ADC electrical characteristics :
		  • Added note 'On reduced pin packages where ... '
		  • Removed max. value of 'I_{DDA_ADC}'
		  • Added note 'Due to triple ... '
		• In 12-bit ADC operating conditions, removed parameter 'ΔV_{DDA}'
		• In CMP with 8-bit DAC electrical specifications :
		  • Updated Typ. and Max. values of 'I_{DDLS}'
		  • Upadted Typ. value of 't_{DHSB}'
		  • Updated Typ. value of 'V_{HYST1}' , 'V_{HYST2}', and 'V_{HYST3}'
		• In LPSPI electrical specifications :
		  • Updated 'f_{periph}' and 'f_{op}', and 't_{SPSCK}'

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes
		• Updated specs for T_{JIT} Cycle-to-Cycle jitter to 300 ps • In QuadSPI AC specifications : • Updated specs for T_{iv} Data Output In-Valid Time • In figure 'QuadSPI output timing (SDR mode) diagram', marked Invalid area • In CMP with 8-bit DAC electrical specifications : • Removed '(VAIO)' from decription of V_{HYST0} • In LPSPI electrical specifications : • Added note 'Undefined' in figures 'LPSPI slave mode timing (CPHA = 0)' and 'LPSPI slave mode timing (CPHA = 1)'