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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mnt0vllt

- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
  - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
  - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
  - 128-bit Unique Identification (ID) number
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - System Memory Protection Unit (System MPU)
  - Cyclic Redundancy Check (CRC) module
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
- Timing and control
  - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- Package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

3 Ordering information

3.1 Selecting orderable part number

Not all part number combinations are available. See the attachment *S32K1xx_Orderable_Part_Number_ List.xlsx* attached with the Datasheet for a list of standard orderable part numbers.

4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate and the ramp rate assumes that the S32K1xx HW design guidelines in AN5426 are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. T_J (Junction temperature)=135 °C. Assumes T_A=125 °C for RUN mode

   T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

   - Assumes maximum θJA for 2s2p board. See Thermal characteristics
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

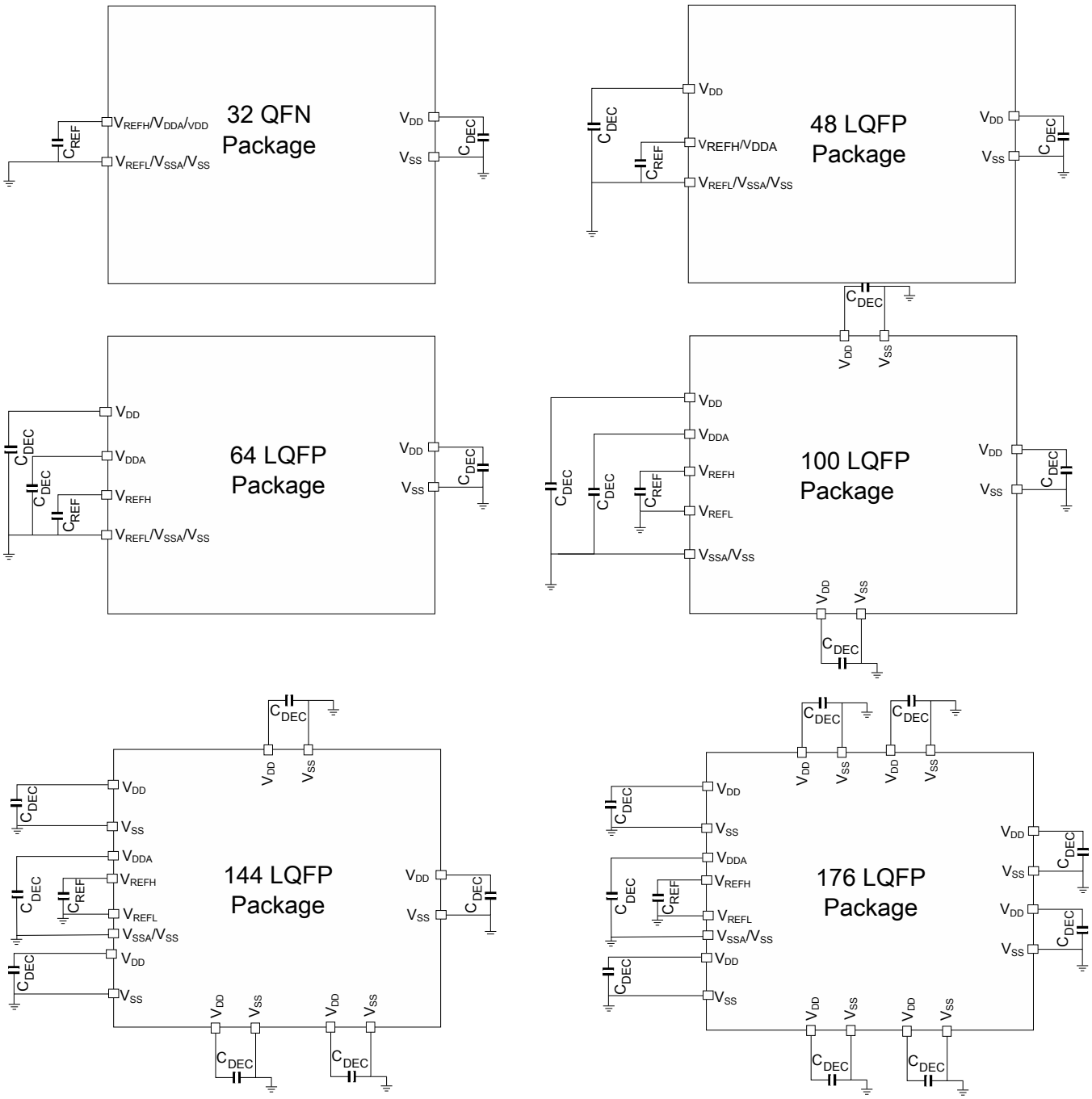
Device functionality is guaranteed up to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.7 V

Table 2. Voltage and current operating requirements 1

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	4
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.

4.4 Power and ground pins



NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB

Figure 5. Pinout decoupling

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. 3	Typ.	Max.	Unit
C_{REF}, 4, 5	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} 5, 6, 7	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
   - The protection/decoupling capacitors must be on the path of the trace connected to that component.
   - No trace exceeding 1 mm from the protection to the trace or to the ground.
   - The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
   - The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.

Table 7. Power consumption (Typicals unless stated otherwise) 1 (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (µA) [2]		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [3]		IDD/MHz (µA/MHz) [4]
			Peripherals disabled [5]	Peripherals enabled	Peripherals disabled [6]	Peripherals enabled use case 1[6]	Peripherals enabled use case 2[7]			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
		Max	1660	1736	3.48	3.55	NA	14.5	15.6	34.8	43.6	41.9	53.9	48.7	65.1	70.4	96.1	609
	105	Typ	560	577	2.49	2.54	4.03	10.9	11.9	29.8	37.8	37.6	47.5	45.2	61.5	63.8	89.1	565
		Max	2945	2970	4.40	4.47	NA	18.0	19.0	38.4	46.8	44.9	55.3	51.6	66.8	73.6	97.4	645
	125	Typ	NA	NA	NA	NA	4.85	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3990	4166	6.00	6.08	NA	23.4	24.5	44.3	52.5	50.9	61.3	57.5	71.6	NA		719

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and On-chip pulldown is enabled for all unused input pins.
2. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
3. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
4. Values mentioned for S32K14x devices are measured at RUN@80 MHz with peripherals disabled and values mentioned for S32K11x devices are measured at RUN@48 MHz with peripherals disabled.
5. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
6. Data collected using RAM
7. Numbers on limited samples size and data collected with Flash
8. The S32K148 data points assume that ENET/QuadSPI/SAI etc. are inactive.

The following table shows the power consumption targets for S32K148 in various mode of operations measure at 3.3 V.

Table 9. Power consumption at 3.3 V

Chip/Device	Ambient Temperature (°C)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA)[1]	
			Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI	Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI
S32K148	25	Typ	67.3	79.1	89.8	105.5
	85	Typ	67.4	79.2	95.6	105.9
		Max	82.5	88.2	109.7	117.4
	105	Typ	68.0	79.8	96.6	106.7
		Max	80.3	89.1	109.0	119.0
	125	Max	83.5	94.7	NA	

1. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.

4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5.3 DC electrical specifications at 3.3 V Range

NOTE

For details on the pad types defined in Table 11 and Table 12, see Reference Manual section *IO Signal Table* and IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Table 11. DC electrical specifications at 3.3 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	1
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	2
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.3 × V_{DD}	V	3
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	3.5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	3	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	14	—	—	mA	4
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	12	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	9.5	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	10	—	—	mA	5
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	16	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	15.5	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins [7]		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		60	kΩ	8
R_{PD}	Internal pulldown resistors	20		60	kΩ	9

1. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable
3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

Table 16. Device clock specifications [1] (continued)

Symbol	Description	Min.	Max.	Unit
f_{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) [3]				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40[4]	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode[5]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

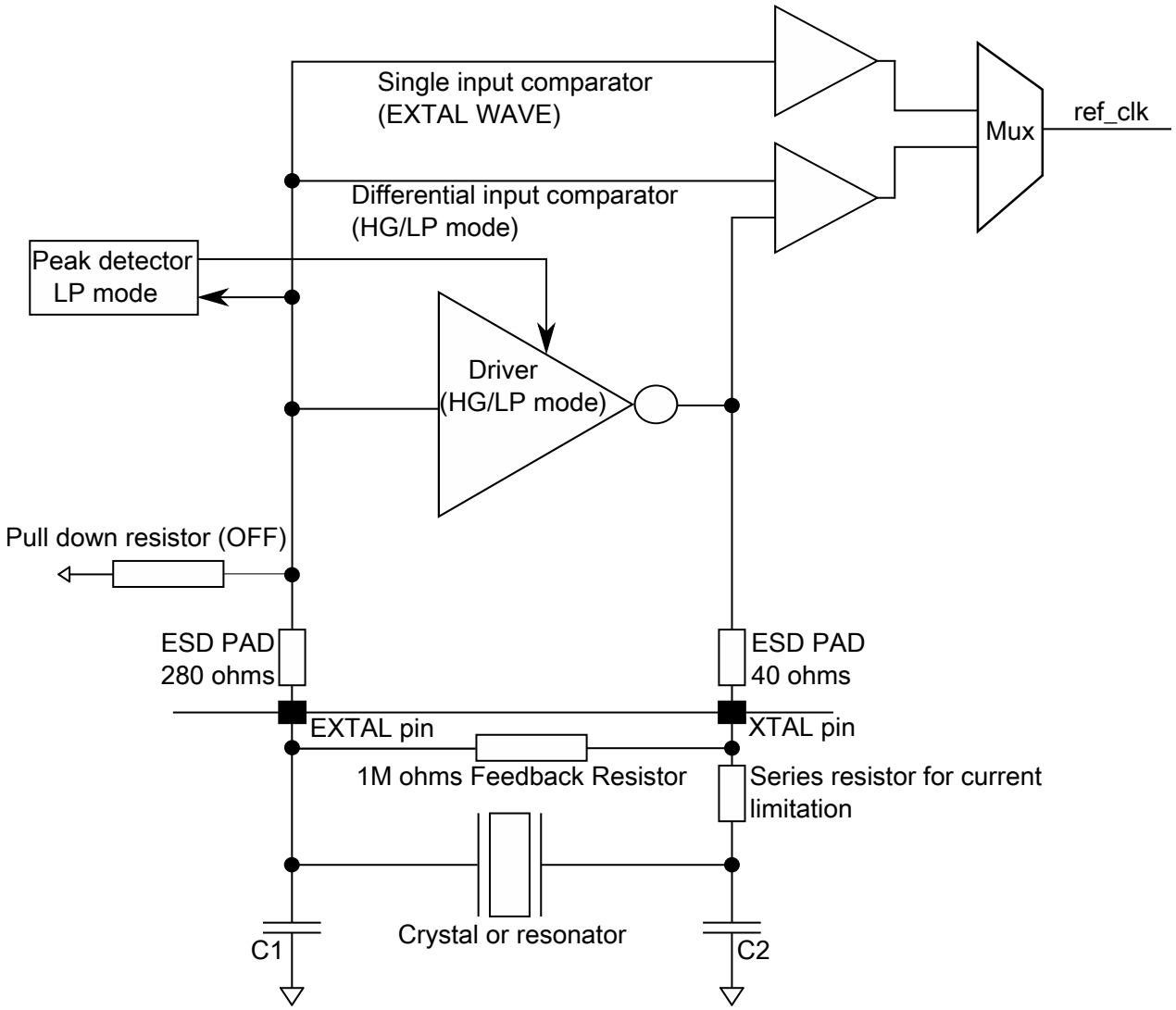


Figure 8. Oscillator connections scheme

Table 17. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz	2.2	—	13.7	mA/V	
	SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	1.15	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

Table 17. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

6.2.3 System Clock Generation (SCG) specifications

6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 19. Fast internal RC Oscillator electrical specifications

Symbol	Parameter[1]	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	$\%F_{FIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		3.4	5	µs[2]
T_{JIT}, [3]	Cycle-to-Cycle jitter	—	300	500	ps
T_{JIT}[3]	Long term jitter over 1000 cycles	—	0.04	0.1	$\%F_{FIRC}$

1. With FIRC regulator enable
2. Startup time is defined as the time between clock enablement and clock availability for system use.
3. FIRC as system clock

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 20. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	—	±3	$\%F_{SIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	—	±3.3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	9	12.5	µs[1]

1. Startup time is defined as the time between clock enablement and clock availability for system use.

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description[1]		S32K116		S32K118			
			Typ	Max	Typ	Max	Unit	Notes
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	µs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)	1st 32-bit write	200	550	200	550	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550		
		Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550		
$t_{quickwrClnup}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms	7

1. All command times assume 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 µs, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

6.3.1.2 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	—	—	years	1
$n_{nvmcycp}$	Cycling endurance	1 K	—	—	cycles	2, 3

Table continues on the next page...

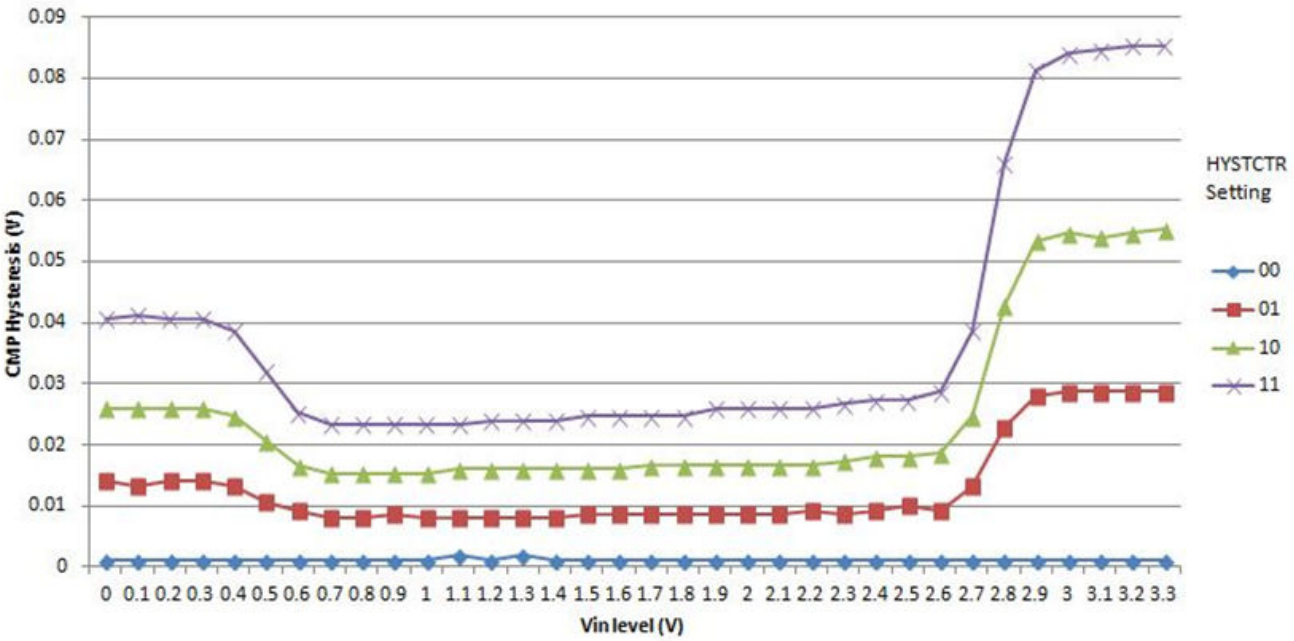


Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)

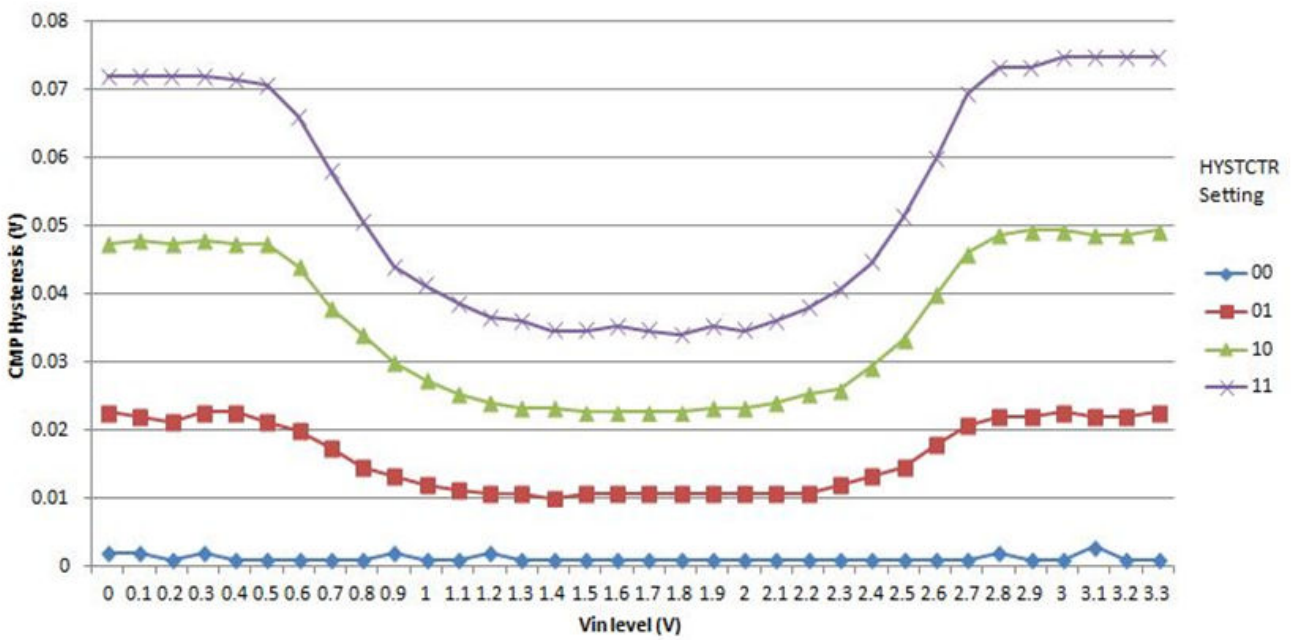


Figure 15. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 38. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	32	93	NA	NA	NA	NA	NA	°C/W
			48	79	71	NA	NA	NA	NA	
			64	NA	62	61	61	59	NA	
			100	NA	NA	53	52	51	NA	
			144	NA	NA	NA	NA	51	44	
			176	NA	NA	NA	NA	NA	42	
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Two layer board (1s1p)	$R_{\theta JA}$	32	50	NA	NA	NA	NA	NA	
			48	58	50	NA	NA	NA	NA	
			64	NA	46	45	45	44	NA	
			100	NA	NA	42	42	40	NA	
			144	NA	NA	NA	NA	44	37	
			176	NA	NA	NA	NA	NA	36	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	32	32	NA	NA	NA	NA	NA	
			48	55	47	NA	NA	NA	NA	
			64	NA	44	43	43	41	NA	
			100	NA	NA	40	40	39	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	35	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	32	77	NA	NA	NA	NA	NA	
			48	66	58	NA	NA	NA	NA	
			64	NA	50	49	49	48	NA	
			100	NA	NA	43	42	41	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	34	
Thermal resistance, Junction to Ambient (@200 ft/min)[1]	Two layer board (1s1p)	$R_{\theta JMA}$	32	43	NA	NA	NA	NA	NA	
			48	51	43	NA	NA	NA	NA	
			64	NA	39	38	38	37	NA	
			100	NA	NA	35	35	34	NA	

Table continues on the next page...

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
			144	NA	NA	NA	NA	37	31	
			176	NA	NA	NA	NA	NA	30	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	32	26	NA	NA	NA	NA	NA	
			48	48	41	NA	NA	NA	NA	
			64	NA	37	36	36	35	NA	
			100	NA	NA	34	34	33	NA	
			144	NA	NA	NA	NA	36	30	
			176	NA	NA	NA	NA	NA	29	
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	32	11	NA	NA	NA	NA	NA	
			48	33	24	NA	NA	NA	NA	
			64	NA	26	25	25	23	NA	
			100	NA	NA	25	25	24	NA	
			144	NA	NA	NA	NA	30	24	
			176	NA	NA	NA	NA	NA	24	
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	32	NA	NA	NA	NA	NA	NA	
			48	23	19	NA	NA	NA	NA	
			64	NA	14	13	12	11	NA	
			100	NA	NA	13	12	11	NA	
			144	NA	NA	NA	NA	12	9	
			176	NA	NA	NA	NA	NA	9	
Thermal resistance, Junction to Case (Bottom) [6]	—	$R_{\theta JCBottom}$	32	1	NA					
			48	NA						
			64							
			100							
			144							
			176							

Table continues on the next page...

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Package Top[7]	Natural Convection	Ψ_{JT}	32	1	NA	NA	NA	NA	NA	
			48	4	2	NA	NA	NA	NA	
			64	NA	2	2	2	2	NA	
			100	NA	NA	2	2	2	NA	
			144	NA	NA	NA	NA	2	1	
			176	NA	NA	NA	NA	NA	1	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.