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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 64MHz |
| Connectivity | CANbus, FlexIO, I²C, LINbus, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 58 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x12b SAR; D/A1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144mst0mlhr |

# Table of Contents

*Description Input Multiplexing sheet(s)* attached with Reference Manual.

| | | S32K11x | | S32K14x | | | |
|---|---|---|---|---|---|---|---|
| | Parameter | K116 | K118 | K142 | K144 | K146 | K148 |
| | Core | Arm® Cortex™-M0+ | | Arm® Cortex™-M4F | | | |
| | Frequency | 48 MHz | | 80 MHz (RUN mode) or 112 MHz (HSRUN mode)[1] | | | |
| System | IEEE-754 FPU | ○ | | ● | | | |
| System | Cryptographic Services Engine (CSEc)[1] | ● | | ● | | | |
| System | CRC module | 1x | | 1x | | | |
| System | ISO 26262 | capable up to ASIL-B | | capable up to ASIL-B | | | |
| System | Peripheral speed | up to 48 MHz | | up to 112 MHz (HSRUN) | | | |
| System | Crossbar | ● | | ● | | | |
| System | DMA | ● | | ● | | | |
| System | External Watchdog Monitor (EWM) | ○ | | ● | | | |
| System | Memory Protection Unit (MPU) | ● | | ● | | | |
| System | FIRC CMU | ● | | ○ | | | |
| System | Watchdog | 1x | | 1x | | | |
| System | Low power modes | ● | | ● | | | |
| System | HSRUN mode[1] | ○ | | ● | | | |
| System | Number of I/Os | up to 43 | up to 58 | up to 89 | | up to 128 | up to 156 |
| System | Single supply voltage | 2.7 - 5.5 V | | 2.7 - 5.5 V | | | |
| System | Ambient Operation Temperature ($T_A$) | -40ºC to +105ºC / +125ºC | | -40ºC to +105ºC / +125ºC | | | |
| Memory | Flash | 128 KB | 256 KB | 256 KB | 512 KB | 1 MB | 2 MB[2] |
| Memory | Error Correcting Code (ECC) | ● | | ● | | | |
| Memory | System RAM (including FlexRAM and MTB) | 17 KB | 25 KB | 32 KB | 64 KB | 128 KB | 256 KB |
| Memory | FlexRAM (also available as system RAM) | 2 KB | | 4 KB | | | |
| Memory | Cache | ○ | | 4 KB | | | |
| Memory | EEPROM emulated by FlexRAM[1] | 2 KB (up to 32 KB D-Flash) | | 4 KB (up to 64 KB D-Flash) | | | See footnote 3 |
| Memory | External memory interface | ○ | | ○ | | | QuadSPI incl. HyperBus™ |
| Timer | Low Power Interrupt Timer (LPIT) | 1x | | 1x | | | |
| Timer | FlexTimer (16-bit counter) 8 channels | 2x (16) | | 4x (32) | | 6x (48) | 8x (64) |
| Timer | Low Power Timer (LPTMR) | 1x | | 1x | | | |
| Timer | Real Time Counter (RTC) | 1x | | 1x | | | |
| Timer | Programmable Delay Block (PDB) | 1x | | 2x | | | |
| Analog | Trigger mux (TRGMUX) | 1x (43) | 1x (45) | 1x (64) | | 1x (73) | 1x (81) |
| Analog | 12-bit SAR ADC (1 Msps each) | 1x (13) | 1x (16) | 2x (16) | | 2x (24) | 2x (32) |
| Analog | Comparator with 8-bit DAC | 1x | | 1x | | | |
| Communication | 10/100 Mbps IEEE-1588 Ethernet MAC | ○ | | ○ | | | 1x |
| Communication | Serial Audio Interface (AC97, TDM, I2S) | ○ | | ○ | | | 2x |
| Communication | Low Power UART/LIN (LPUART) (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A, and SAE J2602) | 2x | | 2x | 3x | | |
| Communication | Low Power SPI (LPSPI) | 1x | 2x | 2x | 3x | | |
| Communication | Low Power I2C (LPI2C) | 1x | | 1x | | | 2x |
| Communication | FlexCAN (CAN-FD ISO/CD 11898-1) | 1x (1x with FD) | | 2x (1x with FD) | 3x (1x with FD) | 3x (2x with FD) | 3x (3x with FD) |
| Communication | FlexIO (8 pins configurable as UART, SPI, I2C, I2S) | 1x | | 1x | | | |
| IDEs | Debug & trace | SWD, MTB (1 KB), JTAG[4] | | SWD, JTAG (ITM, SWV, SWO) | | | SWD, JTAG (ITM, SWV, SWO), ETM |
| IDEs | Ecosystem (IDE, compiler, debugger) | NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems | | NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems | | | |
| Other | Packages[5] | 32-pin QFN<br>48-pin LQFP | 48-pin LQFP<br>64-pin LQFP | 64-pin LQFP<br>100-pin LQFP | 64-pin LQFP<br>100-pin LQFP<br>100-pin MAPBGA | 64-pin LQFP<br>100-pin MAPBGA<br>100-pin LQFP<br>144-pin LQFP | 100-pin MAPBGA<br>144-pin LQFP<br>176-pin LQFP |

LEGEND:
- ○ Not implemented
- ● Available on the device

1 No write or erase access to Flash module, including Security (CSEc) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.
2 Available when EEEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
3 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.
4 Only for Boundary Scan Register
5 See Dimensions section for package drawings

**Figure 3. S32K1xx product series comparison**

# 3 Ordering information

## 3.1 Selecting orderable part number

Not all part number combinations are available. See the attachment *S32K1xx_Orderable_Part_Number_ List.xlsx* attached with the Datasheet for a list of standard orderable part numbers.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input V = $V_{SS}$
7. Measured at input V = $V_{DD}$

## 5.5 AC electrical specifications at 3.3 V range

### Table 13. AC electrical specifications at 3.3 V Range

| Symbol | DSE | Rise time (nS) [1] | | Fall time (nS) [1] | | Capacitance (pF) [2] |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $tRF_{GPIO}$ | NA | 3.2 | 14.5 | 3.4 | 15.7 | 25 |
| | | 5.7 | 23.7 | 6.0 | 26.2 | 50 |
| | | 20.0 | 80.0 | 20.8 | 88.4 | 200 |
| $tRF_{GPIO-HD}$ | 0 | 3.2 | 14.5 | 3.4 | 15.7 | 25 |
| | | 5.7 | 23.7 | 6.0 | 26.2 | 50 |
| | | 20.0 | 80.0 | 20.8 | 88.4 | 200 |
| | 1 | 1.5 | 5.8 | 1.7 | 6.1 | 25 |
| | | 2.4 | 8.0 | 2.6 | 8.3 | 50 |
| | | 6.3 | 22.0 | 6.0 | 23.8 | 200 |
| $tRF_{GPIO-FAST}$ | 0 | 0.6 | 2.8 | 0.5 | 2.8 | 25 |
| | | 3.0 | 7.1 | 2.6 | 7.5 | 50 |
| | | 12.0 | 27.0 | 10.3 | 26.8 | 200 |
| | 1 | 0.4 | 1.3 | 0.38 | 1.3 | 25 |
| | | 1.5 | 3.8 | 1.4 | 3.9 | 50 |
| | | 7.4 | 14.9 | 7.0 | 15.3 | 200 |

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

## 5.6 AC electrical specifications at 5 V range

### Table 14. AC electrical specifications at 5 V Range

| Symbol | DSE | Rise time (nS)[1] | | Fall time (nS) [1] | | Capacitance (pF) [2] |
|---|---|---|---|---|---|---|
| | | Min. | Max . | Min. | Max. | |
| $tRF_{GPIO}$ | NA | 2.8 | 9.4 | 2.9 | 10.7 | 25 |
| | | 5.0 | 15.7 | 5.1 | 17.4 | 50 |
| | | 17.3 | 54.8 | 17.6 | 59.7 | 200 |
| $tRF_{GPIO-HD}$ | 0 | 2.8 | 9.4 | 2.9 | 10.7 | 25 |
| | | 5.0 | 15.7 | 5.1 | 17.4 | 50 |

*Table continues on the next page...*

**Table 14. AC electrical specifications at 5 V Range (continued)**

| Symbol | DSE | Rise time (nS)[1] | | Fall time (nS) [1] | | Capacitance (pF) [2] |
|---|---|---|---|---|---|---|
| | | Min. | Max . | Min. | Max. | |
| | | 17.3 | 54.8 | 17.6 | 59.7 | 200 |
| | 1 | 1.1 | 4.6 | 1.1 | 5.0 | 25 |
| | | 2.0 | 5.7 | 2.0 | 5.8 | 50 |
| | | 5.4 | 16.0 | 5.0 | 16.0 | 200 |
| $tRF_{GPIO-FAST}$ | 0 | 0.42 | 2.2 | 0.37 | 2.2 | 25 |
| | | 2.0 | 5.0 | 1.9 | 5.2 | 50 |
| | | 9.3 | 18.8 | 8.5 | 19.3 | 200 |
| | 1 | 0.37 | 0.9 | 0.35 | 0.9 | 25 |
| | | 1.2 | 2.7 | 1.2 | 2.9 | 50 |
| | | 6.0 | 11.8 | 6.0 | 12.3 | 200 |

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

## 5.7 Standard input pin capacitance

**Table 15. Standard input pin capacitance**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN\_D}$ | Input capacitance: digital pins | — | 7 | pF |

**NOTE**

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

## 5.8 Device clock specifications

**Table 16. Device clock specifications [1]**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| High Speed run mode[2] | | | | |
| $f_{SYS}$ | System and core clock | — | 112 | MHz |
| $f_{BUS}$ | Bus clock | — | 56 | MHz |
| $f_{FLASH}$ | Flash clock | — | 28 | MHz |
| Normal run mode (S32K11x series) | | | | |
| $f_{SYS}$ | System and core clock | — | 48 | MHz |
| $f_{BUS}$ | Bus clock | — | 48 | MHz |

*Table continues on the next page...*

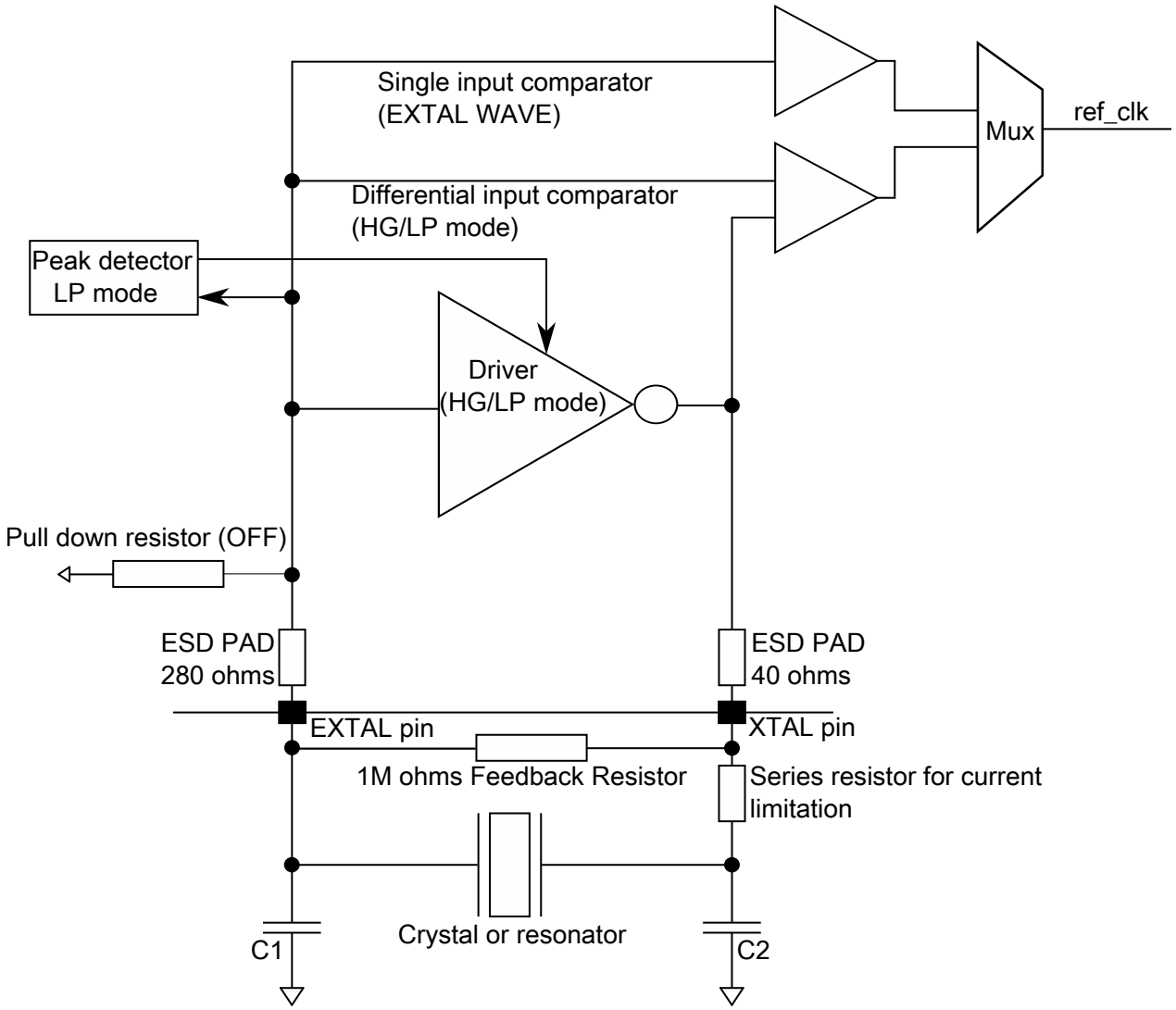


**Figure 8. Oscillator connections scheme**

**Table 17. External System Oscillator electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $g_{mXOSC}$ | Crystal oscillator transconductance | | | | | |
| | SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz | 2.2 | — | 13.7 | mA/V | |
| | SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz | 16 | — | 47 | mA/V | |
| $V_{IL}$ | Input low voltage — EXTAL pin in external clock mode | $V_{SS}$ | — | 1.15 | V | |
| $V_{IH}$ | Input high voltage — EXTAL pin in external clock mode | 0.7 * $V_{DD}$ | — | $V_{DD}$ | V | |
| $C_1$ | EXTAL load capacitance | — | — | — | | 1 |
| $C_2$ | XTAL load capacitance | — | — | — | | 1 |
| $R_F$ | Feedback resistor | | | | | 2 |
| | Low-gain mode (HGO=0) | — | — | — | MΩ | |

*Table continues on the next page...*

**Table 24. Flash command timing specifications for S32K11x (continued)**

| Symbol | Description[1] | | S32K116 | | S32K118 | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Typ | Max | Typ | Max | Unit | Notes |
| $t_{eewr32b}$ | 32-bit write to FlexRAM execution time | 32 KB EEPROM backup | 630 | 2000 | 630 | 2000 | µs | 3,4 |
| | | 48 KB EEPROM backup | — | — | — | — | | |
| | | 64 KB EEPROM backup | — | — | — | — | | |
| $t_{quickwr}$ | 32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write) | 1st 32-bit write | 200 | 550 | 200 | 550 | µs | 4,5,6 |
| | | 2nd through Next to Last (Nth-1) 32-bit write | 150 | 550 | 150 | 550 | | |
| | | Last (Nth) 32-bit write (time for write only, not cleanup) | 200 | 550 | 200 | 550 | | |
| $t_{quickwrClnup}$ | Quick Write Cleanup execution time | — | — | (# of Quick Writes ) * 2.0 | — | (# of Quick Writes ) * 2.0 | ms | 7 |

1. All command times assume 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 µs, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

**NOTE**

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

### 6.3.1.2 Reliability specifications

**Table 25. NVM reliability specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| When using as Program and Data Flash | | | | | | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | — | — | years | 1 |
| $n_{nvmcycp}$ | Cycling endurance | 1 K | — | — | cycles | 2, 3 |

*Table continues on the next page...*

## Table 26. QuadSPI electrical specifications (continued)

| FLASH PORT | Sym | Unit | FLASH A | | | | | | | | | | | | FLASH B | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | RUN[1] | | | | | | HSRUN[1] | | | | | | RUN/HSRUN[2] | | | |
| QuadSPI Mode | | | SDR | | | | | | SDR | | | | | | SDR | | DDR[3] | |
| | | | Internal Sampling | | Internal DQS | | | | Internal Sampling | | Internal DQS | | | | Internal Sampling | | External DQS | |
| | | | N1 | | PAD Loopback | | Internal Loopback | | N1 | | PAD Loopback | | Internal Loopback | | N1 | | External DQS | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| SCK Duty Cycle | $t_{SDC}$ | ns | tSCK/2 - 1.5 | tSCK/2 + 1.5 | tSCK/2 - 1.5 | tSCK/2 + 1.5 | tSCK/2 - 1.5 | tSCK/2 + 1.5 | tSCK/2 - 1.5 | tSCK/2 + 1.5 | tSCK/2 - 0.750 | tSCK/2 - 0.750 | tSCK/2 - 1.5 | tSCK/2 + 1.5 | tSCK/2 - 2.5 | tSCK/2 + 2.5 | tSCK/2 - 2.5 | tSCK/2 + 2.5 |
| Data Input Setup Time | $t_{IS}$ | ns | 15 | - | 2.5 | - | 10 | - | 14 | - | 1.6 | - | 9 | - | 25 | - | 2 | - |
| Data Input Hold Time | $t_{IH}$ | ns | 0 | - | 1 | - | 1 | - | 0 | - | 1 | - | 1 | - | 0 | - | 20 | - |
| Data Output Valid Time | $t_{OV}$ | ns | - | 4.5 | - | 4.5 | - | 4.5 | - | 4 | - | 4 | - | 4 | - | 10 | - | 10 |
| Data Output In-Valid Time | $t_{IV}$ | ns | - | 5 | - | 5 | - | 5 | - | 5 | - | 3[5] | - | 5 | - | 5 | 5 | - |
| CS to SCK Time [6] | $t_{CSSCK}$ | ns | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 10 | - | 10 | - |
| SCK to CS Time [7] | $t_{SCKCS}$ | ns | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - |
| Output Load | | pf | 25 | | 25 | | 25 | | 25 | | 25 | | 25 | | 25 | | 25 | |

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz,Output invalid time is 5 ns.
6. Program register value QuadSPI_FLSHCR[TCSS] = 4`h2
7. Program register value QuadSPI_FLSHCR[TCSH] = 4`h1

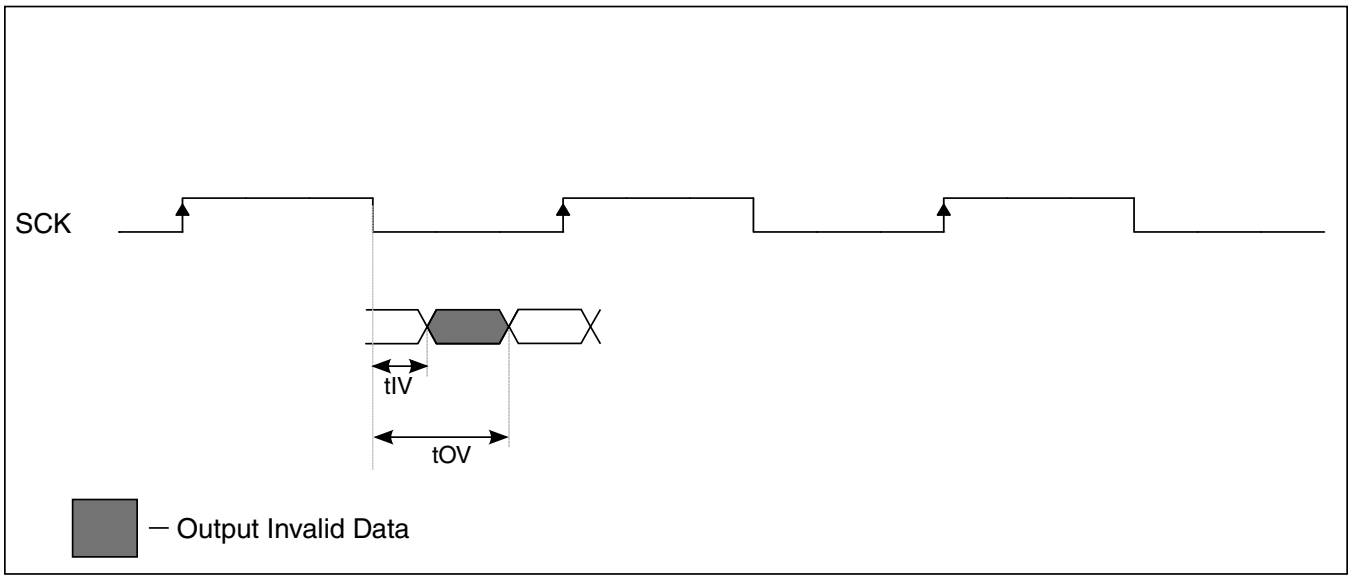


**Figure 12. QuadSPI output timing (HyperRAM mode) diagram**

# 6.4 Analog modules

## 6.4.1 ADC electrical specifications

### 6.4.1.1 12-bit ADC operating conditions

**Table 27. 12-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{REFH}$ | ADC reference voltage high | | See Voltage and current operating requirements for values | $V_{DDA}$ | See Voltage and current operating requirements for values | V | 2 |
| $V_{REFL}$ | ADC reference voltage low | | See Voltage and current operating requirements for values | 0 | See Voltage and current operating requirements for values | mV | 2 |
| $V_{ADIN}$ | Input voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| $R_S$ | Source impedendance | $f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | |
| $R_{SW1}$ | Channel Selection Switch Impedance | | — | 0.75 | 1.2 | kΩ | |
| $R_{AD}$ | Sampling Switch Impedance | | — | 2 | 5 | kΩ | |
| $C_{P1}$ | Pin Capacitance | | — | 10 | — | pF | |
| $C_{P2}$ | Analog Bus Capacitance | | — | — | 4 | pF | |
| $C_S$ | Sampling capacitance | | — | 4 | 5 | pF | |

*Table continues on the next page...*

### 6.4.1.2 12-bit ADC electrical characteristics

**NOTE**

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See AN5426 for details

**Table 28. 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SS}$)**

| Symbol | Description | Conditions [1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 2.7 | — | 3 | V | |
| $I_{DDA\_ADC}$ | Supply current per ADC | | — | 0.6 | — | mA | 3 |
| SMPLTS | Sample Time | | 275 | — | Refer to the *Reference Manual* | ns | |
| TUE[4] | Total unadjusted error | | — | ±4 | ±8 | LSB[5] | 6, 7, 8, 9 |
| DNL | Differential non-linearity | | — | ±1.0 | — | LSB[5] | 6, 7, 8, 9 |
| INL | Integral non-linearity | | — | ±2.0 | — | LSB[5] | 6, 7, 8, 9 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$=$V_{DDA}$=$V_{DD}$, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume $V_{DDA}$ = 3 V, Temp = 25 °C, $f_{ADCK}$ = 40 MHz, $R_{AS}$=20 Ω, and $C_{AS}$=10 nF.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to $V_{DD}$/$V_{SS}$ or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

## Table 29. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SS}$)

| Symbol | Description | Conditions [1] | Min. | Typ.[2] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 3 | — | 5.5 | V | |
| $I_{DDA\_ADC}$ | Supply current per ADC | | — | 1 | — | mA | 3 |
| SMPLTS | Sample Time | | 275 | — | Refer to the *Reference Manual* | ns | |
| TUE[4] | Total unadjusted error | | — | ±4 | ±8 | LSB[5] | 6, 7, 8, 9 |
| DNL | Differential non-linearity | | — | ±0.7 | — | LSB[5] | 6, 7, 8, 9 |
| INL | Integral non-linearity | | — | ±1.0 | — | LSB[5] | 6, 7, 8, 9 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$=$V_{DDA}$=$V_{DD}$, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume $V_{DDA}$ = 5.0 V, Temp = 25 °C, $f_{ADCK}$ = 40 MHz, $R_{AS}$=20 Ω, and $C_{AS}$=10 nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/$2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to $V_{DD}$/$V_{SS}$ or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

**NOTE**

- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

| Pin name | TGATE purpose |
|---|---|
| PTE8 | CMP0_IN3 |
| PTC3 | ADC0_SE11/CMP0_IN4 |
| PTC2 | ADC0_SE10/CMP0_IN5 |
| PTD7 | CMP0_IN6 |
| PTD6 | CMP0_IN7 |
| PTD28 | ADC1_SE22 |
| PTD27 | ADC1_SE21 |

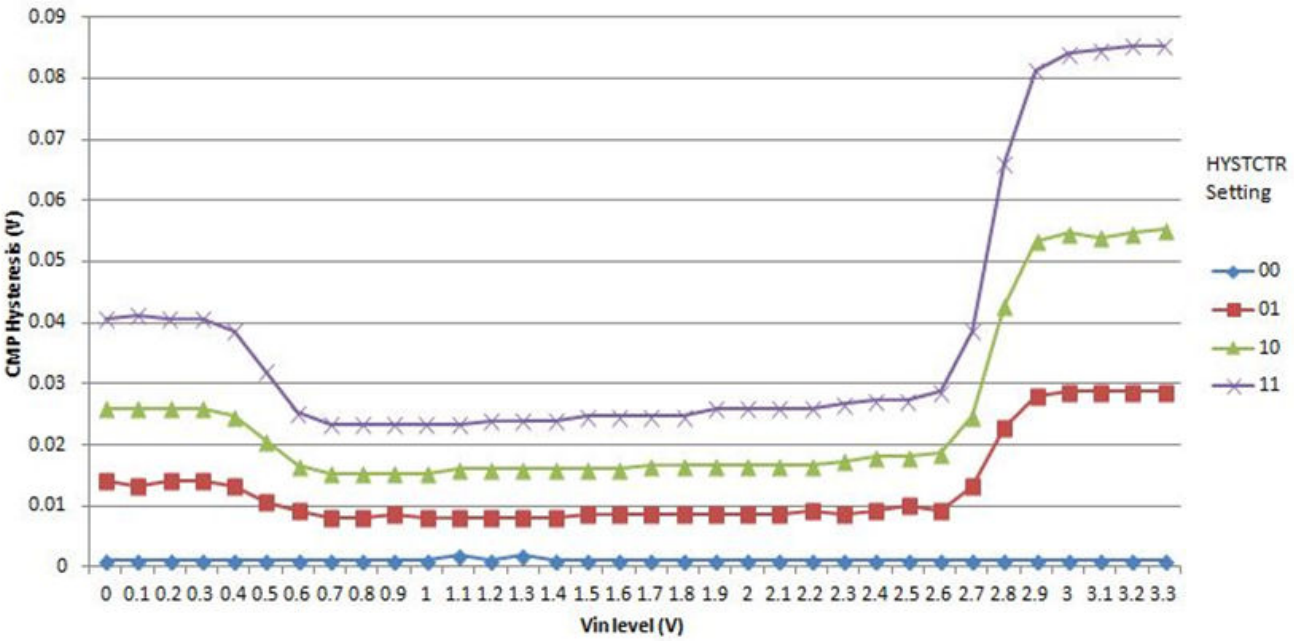


**Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)**

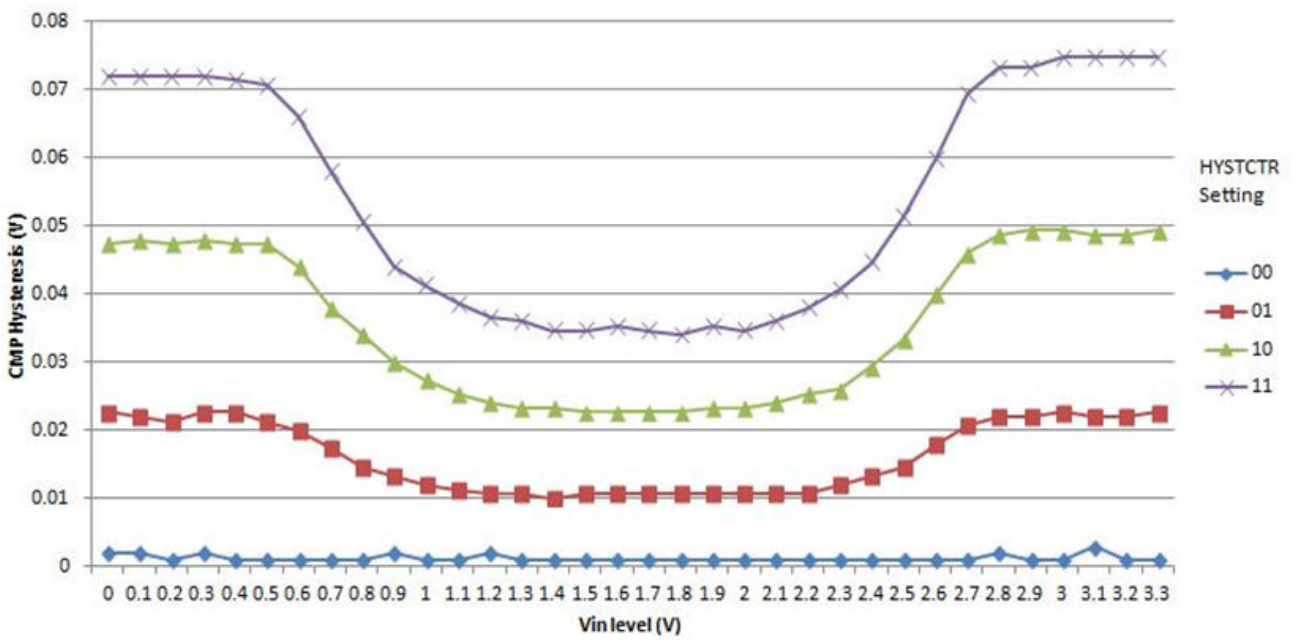


**Figure 15. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)**

# 6.5 Communication modules

## 6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

### 6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

## 6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting ( DSE = 1 ).

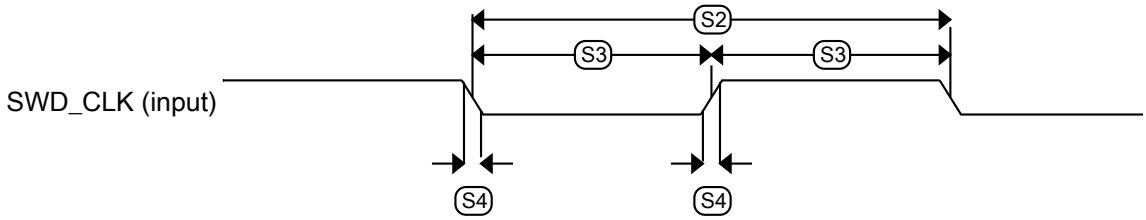


**Figure 29. Serial wire clock input timing**

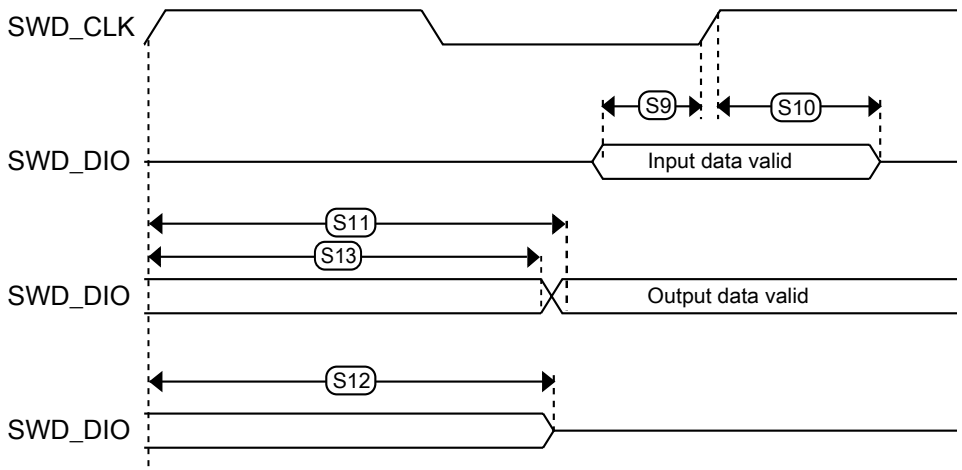


**Figure 30. Serial wire data timing**

## 6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN ), the interface should be OFF.

**Table 39. Trace specifications**

| | Symbol | Description | RUN Mode | | | HSRUN Mode | | VLPR Mode | Unit |
|---|---|---|---|---|---|---|---|---|---|
| — | Fsys | System frequency | 80 | 48 | 40 | 112 | 80 | 4 | MHz |

*Table continues on the next page...*

## Table 40. JTAG electrical specifications

| Symbol | Description | Run Mode | | | | HSRUN Mode | | | | VLPR Mode | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| JI | TCLK frequency of operation | | | | | | | | | | | | | MHz |
| | Boundary Scan | - | 20 | - | 20 | - | 20 | - | 20 | - | 10 | - | 10 | |
| | JTAG | - | 20 | - | 20 | - | 20 | - | 20 | - | 10 | - | 10 | |
| J2 | TCLK cycle period | 1/JI | - | 1/JI | - | 1/JI | - | 1/JI | - | 1/JI | - | 1/JI | - | ns |
| J3 | TCLK clock pulse width | | | | | | | | | | | | | ns |
| | Boundary Scan | J2/2 - 5 | J2/2 + 5 | J2/2 - 5 | J2/2 + 5 | J2/2 - 5 | J2/2 + 5 | J2/2 - 5 | J2/2 + 5 | J2/2 - 5 | J2/2 + 5 | J2/2 - 5 | J2/2 + 5 | |
| | JTAG | | | | | | | | | | | | | |
| J4 | TCLK rise and fall times | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 5 | - | 5 | - | 5 | - | 5 | - | 15 | - | 15 | - | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 5 | - | 5 | - | 5 | - | 5 | - | 8 | - | 8 | - | ns |
| J7 | TCLK low to boundary scan output data valid | - | 28 | - | 32 | - | 28 | - | 32 | - | 80 | - | 80 | ns |
| J8 | TCLK low to boundary scan output data invalid | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | |
| J9 | TCLK low to boundary scan output high-Z | - | 28 | - | 32 | - | 28 | - | 32 | - | 80 | - | 80 | ns |
| J10 | TMS, TDI input data setup time to TCLK rise | 3 | - | 3 | - | 3 | - | 3 | - | 15 | - | 15 | - | ns |
| J11 | TMS, TDI input data hold time after TCLK rise | 2 | - | 2 | - | 2 | - | 2 | - | 8 | - | 8 | - | ns |
| J12 | TCLK low to TDO data valid | - | 28 | - | 32 | - | 28 | - | 32 | - | 80 | - | 80 | ns |
| J13 | TCLK low to TDO data invalid | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| J14 | TCLK low to TDO high-Z | - | 28 | - | 32 | - | 28 | - | 32 | - | 80 | - | 80 | ns |

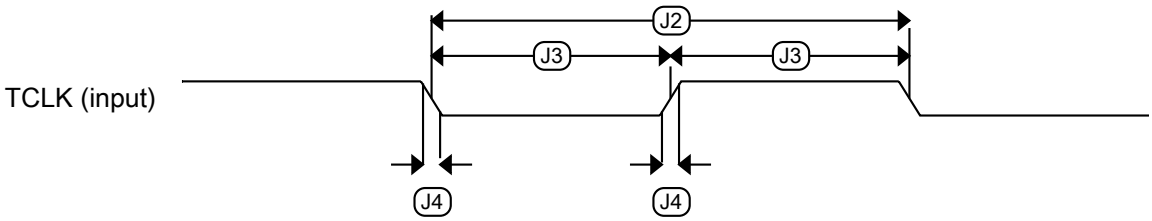


**Figure 32. Test clock input timing**

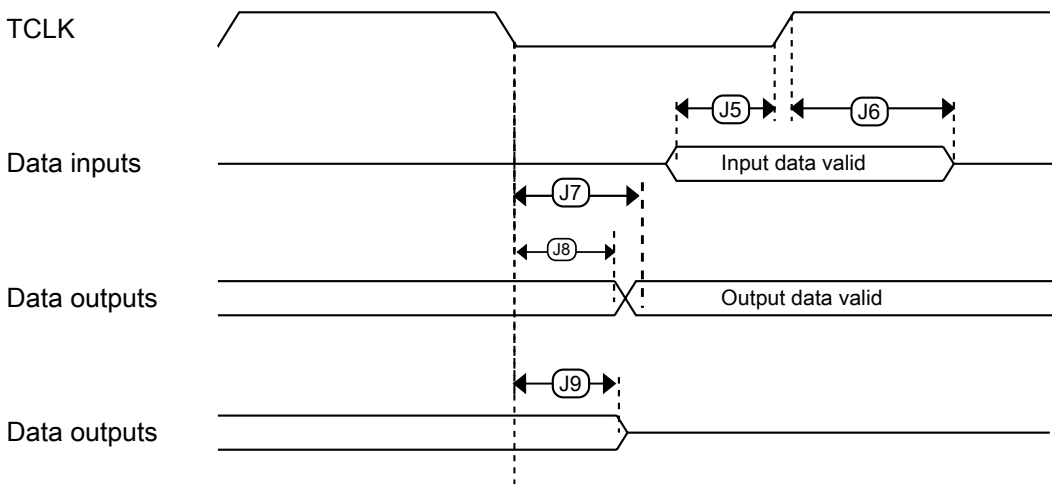


**Figure 33. Boundary scan (JTAG) timing**

## Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package

| Rating | Conditions | Symbol | Package | Values | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | S32K116 | S32K118 | S32K142 | S32K144 | S32K146 | S32K148 | |
| Thermal resistance, Junction to Ambient (Natural Convection)[1, 2] | Single layer board (1s) | $R_{\theta JA}$ | 32 | 93 | NA | NA | NA | NA | NA | °C/W |
| | | | 48 | 79 | 71 | NA | NA | NA | NA | |
| | | | 64 | NA | 62 | 61 | 61 | 59 | NA | |
| | | | 100 | NA | NA | 53 | 52 | 51 | NA | |
| | | | 144 | NA | NA | NA | NA | 51 | 44 | |
| | | | 176 | NA | NA | NA | NA | NA | 42 | |
| Thermal resistance, Junction to Ambient (Natural Convection)[1] | Two layer board (1s1p) | $R_{\theta JA}$ | 32 | 50 | NA | NA | NA | NA | NA | |
| | | | 48 | 58 | 50 | NA | NA | NA | NA | |
| | | | 64 | NA | 46 | 45 | 45 | 44 | NA | |
| | | | 100 | NA | NA | 42 | 42 | 40 | NA | |
| | | | 144 | NA | NA | NA | NA | 44 | 37 | |
| | | | 176 | NA | NA | NA | NA | NA | 36 | |
| Thermal resistance, Junction to Ambient (Natural Convection)[1, 2] | Four layer board (2s2p) | $R_{\theta JA}$ | 32 | 32 | NA | NA | NA | NA | NA | |
| | | | 48 | 55 | 47 | NA | NA | NA | NA | |
| | | | 64 | NA | 44 | 43 | 43 | 41 | NA | |
| | | | 100 | NA | NA | 40 | 40 | 39 | NA | |
| | | | 144 | NA | NA | NA | NA | 42 | 36 | |
| | | | 176 | NA | NA | NA | NA | NA | 35 | |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3] | Single layer board (1s) | $R_{\theta JMA}$ | 32 | 77 | NA | NA | NA | NA | NA | |
| | | | 48 | 66 | 58 | NA | NA | NA | NA | |
| | | | 64 | NA | 50 | 49 | 49 | 48 | NA | |
| | | | 100 | NA | NA | 43 | 42 | 41 | NA | |
| | | | 144 | NA | NA | NA | NA | 42 | 36 | |
| | | | 176 | NA | NA | NA | NA | NA | 34 | |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1] | Two layer board (1s1p) | $R_{\theta JMA}$ | 32 | 43 | NA | NA | NA | NA | NA | |
| | | | 48 | 51 | 43 | NA | NA | NA | NA | |
| | | | 64 | NA | 39 | 38 | 38 | 37 | NA | |
| | | | 100 | NA | NA | 35 | 35 | 34 | NA | |

*Table continues on the next page...*

## Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

| Rating | Conditions | Symbol | Package | Values | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | S32K116 | S32K118 | S32K142 | S32K144 | S32K146 | S32K148 | |
| Thermal resistance, Junction to Package Top[7] | Natural Convection | $\Psi_{JT}$ | 32 | 1 | NA | NA | NA | NA | NA | |
| | | | 48 | 4 | 2 | NA | NA | NA | NA | |
| | | | 64 | NA | 2 | 2 | 2 | 2 | NA | |
| | | | 100 | NA | NA | 2 | 2 | 2 | NA | |
| | | | 144 | NA | NA | NA | NA | 2 | 1 | |
| | | | 176 | NA | NA | NA | NA | NA | 1 | |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## Table 43. Revision History

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • Added footnotes $V_{ih}$ Input Buffer High Voltage and $V_{ih}$ Input Buffer Low Voltage<br>• Updated table: AC electrical specifications at 3.3 V range<br>• Updated table: AC electrical specifications at 5 V range<br>• In table: Standard input pin capacitance<br>  • Added footnote to Normal run mode (S32K14x series)<br>• Removed note from 1M ohms Feedback Resistor in figure Oscillator connections scheme<br>• In table: External System Oscillator electrical specifications<br>  • Updated typical of $I_{DDOSC}$ Supply current — low-gain mode (low-power mode) (HGO=0) 1 for 4 and 8 MHz<br>  • Removed rows for $I_{lk\_ext}$ EXTAL/XTAL impedence High-frequency, low-gain mode (low-power mode) and high-frequency, high-gain mode and $V_{EXTAL}$<br>  • Updated Typ. of $R_S$ low-gain mode<br>  • Updated description of $R_F$, $R_S$, and $V_{PP}$<br>  • Removed footnote from $R_F$ Feedback resistor<br>  • Updated footnote for $C_1$ $C_2$ and $R_F$<br>• In table: Table 18<br>  • Removed mention of high-frequency<br>  • Added HGO 0, 1 information<br>• In table: Fast internal RC Oscillator electrical specifications<br>  • Updated $F_{FIRC}$<br>  • Updated description of ΔF<br>  • Updated typ and max values of $T_{JIT}$ cycle-to-cycle jitter and $T_{JIT}$ Long term jitter over 1000 cycles<br>  • Added footnotes to $T_{JIT}$ cycle-to-cycle jitter and $T_{JIT}$ Long term jitter over 1000 cycles<br>  • Updated naming convention of $I_{DDFIRC}$ Supply current<br>  • Added footnote to $I_{DDFIRC}$ Supply current<br>  • Added footnote to column Parameter<br>• In table: Slow internal RC oscillator (SIRC) electrical specifications<br>  • Removed $V_{DD}$ Supply current in 2 MHz Mode<br>  • Removed footnote and updated description of ΔF<br>  • Updated footnote to $F_{SIRC}$ and $I_{DDSIRC}$<br>• In table: SPLL electrical specifications<br>  • Added row for $F_{SPLL\_REF}$ PLL Reference<br>  • Updated naming convention throughout the table<br>  • Updated the max value of $T_{SPLL\_LOCK}$ Lock detector detection time<br>• In table: Flash timing specifications — commands<br>  • Added footnotes:<br>  • All command times assumes ...<br>  • For all EEPROM Emulation terms ...<br>  • 'First time' EERAM writes after a POR ...<br>  • Removed footnote 'Assumes 25 MHz or ...'<br>  • Updated Max of $t_{eewr32bers}$<br>  • Added parameters $t_{quickwr}$ and $t_{quickwrClnup}$<br>• In table: Reliability specifications<br>  • Removed Typ. values for all parameters<br>  • Removed footnote 'Typical values represent ... '<br>  • Added footnote 'Any other EEE driver usage ... '<br>• Updated QuadSPI AC specifications<br>• Removed topic: Reliability, Safety and Security modules<br>• In table: 12-bit ADC operating conditions<br>  • Updated $V_{DDA}$ |

*Table continues on the next page...*

## Table 43. Revision History

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • Updated specs for $T_{JIT}$ Cycle-to-Cycle jitter to 300 ps<br>• In QuadSPI AC specifications :<br>• Updated specs for $T_{iv}$ Data Output In-Valid Time<br>• In figure 'QuadSPI output timing (SDR mode) diagram', marked Invalid area<br>• In CMP with 8-bit DAC electrical specifications :<br>• Removed '(VAIO)' from decription of $V_{HYST0}$<br>• In LPSPI electrical specifications :<br>• Added note 'Undefined' in figures 'LPSPI slave mode timing (CPHA = 0)' and 'LPSPI slave mode timing (CPHA = 1)' |