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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

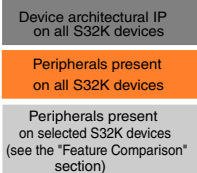
Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	112MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k144uft0vlhr

- Communications interfaces
 - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
 - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
 - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
 - Up to three FlexCAN modules (with optional CAN-FD support)
 - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
 - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
 - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
 - 128-bit Unique Identification (ID) number
 - Error-Correcting Code (ECC) on flash and SRAM memories
 - System Memory Protection Unit (System MPU)
 - Cyclic Redundancy Check (CRC) module
 - Internal watchdog (WDOG)
 - External Watchdog monitor (EWM) module
- Timing and control
 - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
 - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
 - Two Programmable Delay Blocks (PDB) with flexible trigger system
 - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
 - 32-bit Real Time Counter (RTC)
- Package
 - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

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2 Feature comparison

NOTE

Availability of peripherals depends on the pin availability in a particular package. For more information see *IO Signal*

Table 5. V_{DD} supply LVR, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- RUN Mode:
 - Clock source: FIRC
 - SYS_CLK/CORE_CLK = 48 MHz
 - BUS_CLK = 48 MHz
 - FLASH_CLK = 24 MHz
- HSRUN Mode:
 - Clock source: SPL
 - SYS_CLK/CORE_CLK = 112 MHz
 - BUS_CLK = 56 MHz
 - FLASH_CLK = 28 MHz
- VLPR Mode:
 - Clock source: SIRC
 - SYS_CLK/CORE_CLK = 4 MHz
 - BUS_CLK = 4 MHz
 - FLASH_CLK = 1 MHz
- STOP1/STOP2 Mode:
 - Clock source: FIRC
 - SYS_CLK/CORE_CLK = 48 MHz
 - BUS_CLK = 48 MHz
 - FLASH_CLK = 24 MHz
- VLPS Mode: All clock sources disabled ¹

Table 6. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	μs

Table continues on the next page...

1.

- For S32K11x – FIRC/SOSC
- For S32K14x – FIRC/SOSC/SPLL

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	μs
	STOP1 → RUN	0.07	0.075	0.08	μs
	STOP2 → RUN	0.07	0.075	0.08	μs
	VLPR → RUN	19	—	26	μs
	VLPR → VLPS	5.1	5.7	6.5	μs
	VLPS → VLPR	18.8	23	27.75	μs
	RUN → Compute operation	0.72	0.75	0.77	μs
	HSRUN → Compute operation	0.3	0.31	0.35	μs
	RUN → STOP1	0.35	0.38	0.4	μs
	RUN → STOP2	0.2	0.23	0.25	μs
	RUN → VLPS	0.3	0.35	0.4	μs
	RUN → VLPR	3.5	3.8	5	μs
	VLPS → Asynchronous DMA Wakeup	105	110	125	μs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	Pin reset → Code execution	—	214	—	μs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes_Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table [Table 7](#). For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

Table 7. Power consumption (Typicals unless stated otherwise) 1 (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (μA) ²		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) ³		IDD/MHz (μA/MHz) ⁴
			Peripherals disabled ⁵	Peripherals enabled	Peripherals disabled ⁶	Peripherals enabled use case ¹⁶	Peripherals enabled use case ²⁷			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
	105	Max	1660	1736	3.48	3.55	NA	14.5	15.6	34.8	43.6	41.9	53.9	48.7	65.1	70.4	96.1	609
		Typ	560	577	2.49	2.54	4.03	10.9	11.9	29.8	37.8	37.6	47.5	45.2	61.5	63.8	89.1	565
		Max	2945	2970	4.40	4.47	NA	18.0	19.0	38.4	46.8	44.9	55.3	51.6	66.8	73.6	97.4	645
	125	Typ	NA	NA	NA	NA	4.85	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
		Max	3990	4166	6.00	6.08	NA	23.4	24.5	44.3	52.5	50.9	61.3	57.5	71.6	NA	NA	719

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5\text{ V}$, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and On-chip pulldown is enabled for all unused input pins.
2. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
3. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
4. Values mentioned for S32K14x devices are measured at RUN@80 MHz with peripherals disabled and values mentioned for S32K11x devices are measured at RUN@48 MHz with peripherals disabled.
5. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
6. Data collected using RAM
7. Numbers on limited samples size and data collected with Flash
8. The S32K148 data points assume that ENET/QuadSPI/SAI etc. are inactive.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

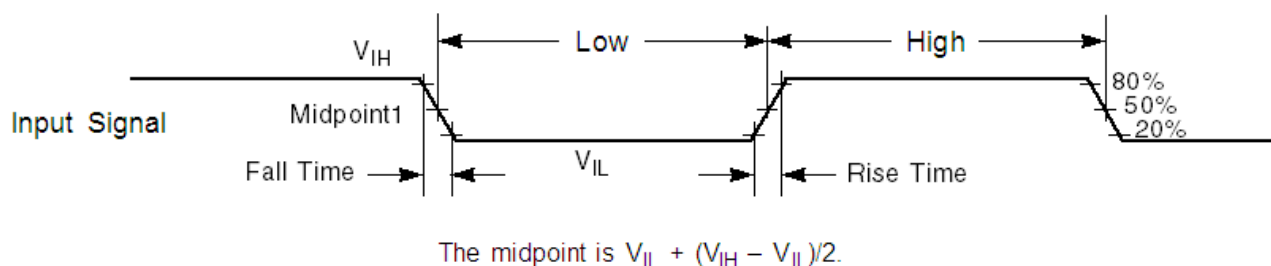


Figure 7. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	RESET input filtered pulse	—	10	ns	4
WNFRST	RESET input not filtered pulse	Maximum of (100 ns, bus clock period)	—	ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Maximum length of RESET pulse which will be filtered by internal filter.
5. Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter. This number depends on bus clock period also. For example, in VLPR mode bus clock is 4 MHz, which make clock period of 250 ns. In this case, minimum pulse width which will cause reset is 250 ns. For faster bus clock frequencies which have clock period less than 100 ns, the minimum pulse width not filtered will be 100 ns.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input $V = V_{SS}$
7. Measured at input $V = V_{DD}$

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max.	Min.	Max.	
tRF _{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
tRF _{GPIO-HD}	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
tRF _{GPIO-FAST}	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max .	Min.	Max.	
tRF _{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
tRF _{GPIO-HD}	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

**Table 17. External System Oscillator electrical specifications
(continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when $g_{mXOSC} > 5 * gm_crit$. The gm_crit is defined as:

$$gm_crit = 4 * ESR * (2\pi F)^2 * (C_0 + C_L)^2$$

where:

- g_{mXOSC} is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2 / (C_1 + C_2)]$
- C_s is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

- When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
 - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

6.2.3 System Clock Generation (SCG) specifications

6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 19. Fast internal RC Oscillator electrical specifications

Symbol	Parameter ¹	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	% F_{FIRC}
ΔF_{125}	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	% F_{FIRC}
T_{Startup}	Startup time		3.4	5	μs ²
T_{JIT}^3	Cycle-to-Cycle jitter	—	300	500	ps
T_{JIT}^3	Long term jitter over 1000 cycles	—	0.04	0.1	% F_{FIRC}

1. With FIRC regulator enable

2. Startup time is defined as the time between clock enablement and clock availability for system use.

3. FIRC as system clock

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 20. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	—	±3	% F_{SIRC}
ΔF_{125}	Frequency deviation across process, voltage, and temperature < 125°C	—	—	±3.3	% F_{SIRC}
T_{Startup}	Startup time	—	9	12.5	μs ¹

1. Startup time is defined as the time between clock enablement and clock availability for system use.

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit Notes	
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
t _{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t _{eevr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
t _{eevr16b}	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
t _{eevr32bers}	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	μs	
t _{eevr32b}	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	μs	3,4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
t _{quickwr}	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	μs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit Notes	
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
	setting (32-bit write complete, ready for next 32-bit write)	Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550	200	550	200	550		
$t_{\text{quickwrClnup}}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms	7

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 μ s, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

Table 24. Flash command timing specifications for S32K11x

Symbol	Description ¹		S32K116		S32K118		Unit Notes	
			Typ	Max	Typ	Max		
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	0.36	—	0.36	ms	
		64 KB flash	—	—	—	—		
		128 KB flash	—	1.2	—	—		
		256 KB flash	—	—	—	2		
		512 KB flash	—	—	—	—		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	μ s	
		4 KB flash	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	100	—	100	μ s	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	μ s	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	15	300	15	300	ms	2
		64 KB flash	—	—	—	—		
		128 KB flash	120	1100	—	—		
		256 KB flash	—	—	250	2125		
		512 KB flash	—	—	—	—		

Table continues on the next page...

Table 31. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	—	23	80	
V _{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	—	46	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	—	32	120	
I _{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	μA
	5V Reference Voltage	—	10	16	μA
INL ⁵	8-bit DAC integral non-linearity	−0.75	—	0.75	LSB ⁶
DNL	8-bit DAC differential non-linearity	−0.5	—	0.5	LSB ⁶
t _{DDAC}	Initialization and switching settling time	—	—	30	μs

1. Difference at input > 200mV
2. Applied $\pm (100 \text{ mV} + V_{\text{HYST0}/1/2/3+ \text{ max. of } V_{\text{AIO}})$ around switch point.
3. Applied $\pm (30 \text{ mV} + 2 \times V_{\text{HYST0}/1/2/3+ \text{ max. of } V_{\text{AIO}})$ around switch point.
4. Applied $\pm (100 \text{ mV} + V_{\text{HYST0}/1/2/3})$.
5. Calculation method used: Linear Regression Least Square Method
6. $1 \text{ LSB} = V_{\text{reference}}/256$

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

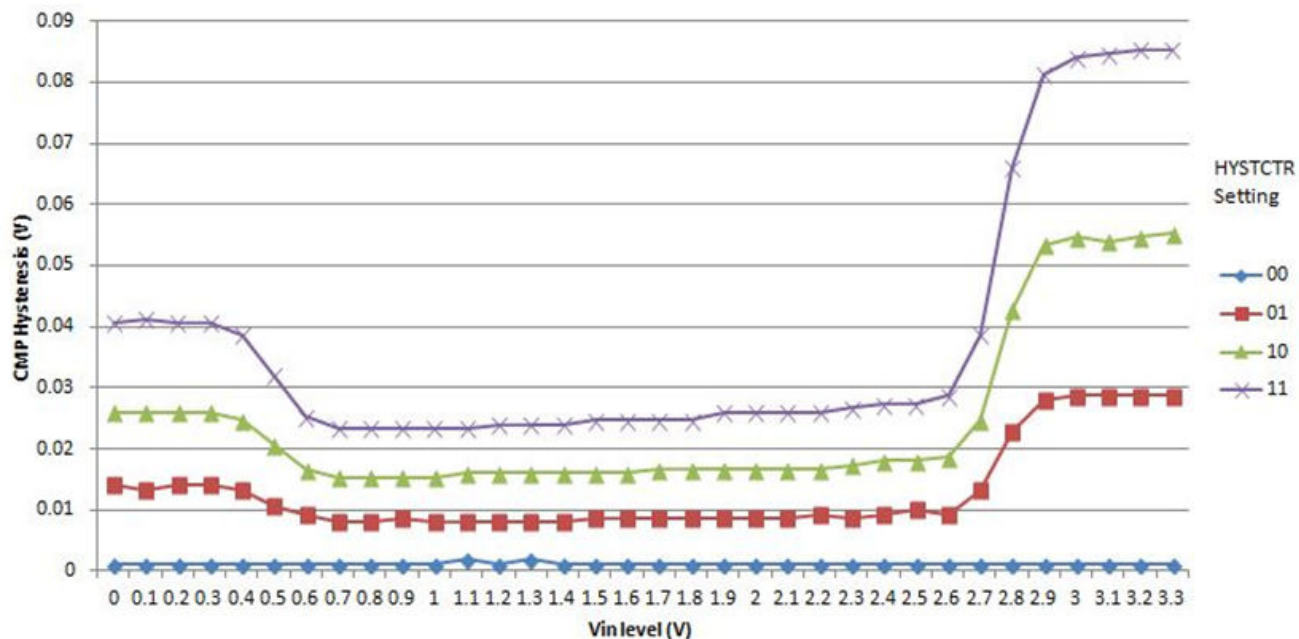


Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)

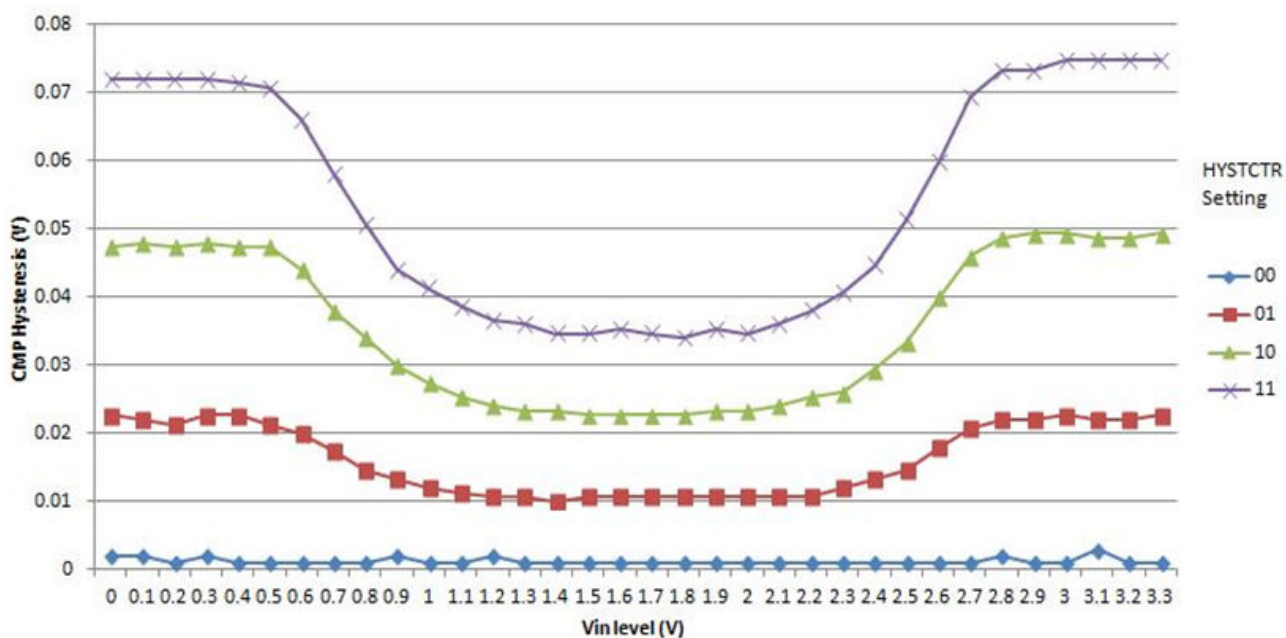


Figure 15. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

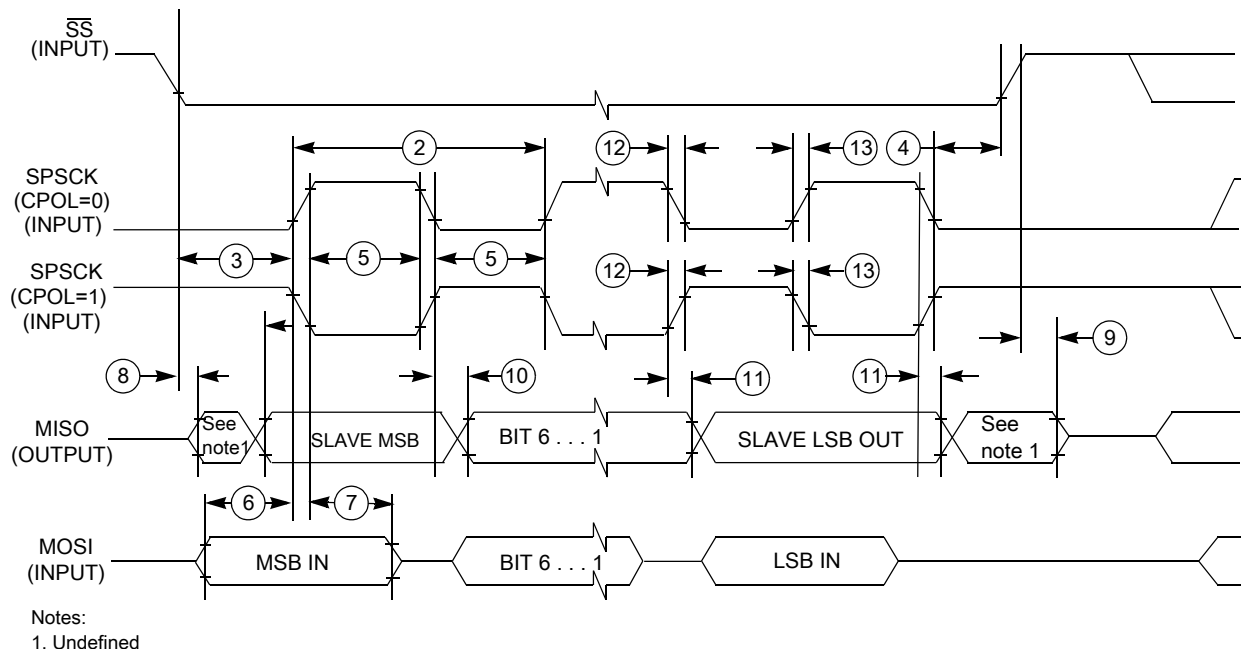


Figure 20. LPSPI slave mode timing (CPHA = 0)

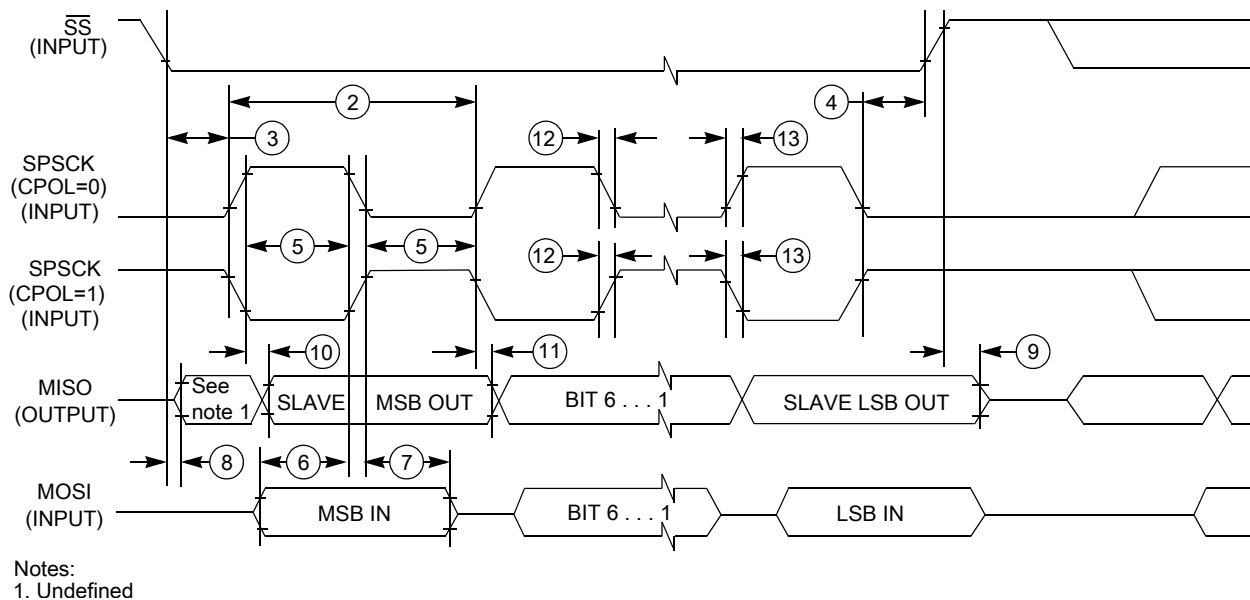


Figure 21. LPSPI slave mode timing (CPHA = 1)

6.5.3 LPI2C electrical specifications

See [General AC specifications](#) for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual*.

6.5.4 FlexCAN electrical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

6.5.5 SAI electrical specifications

The following table describes the SAI electrical characteristics.

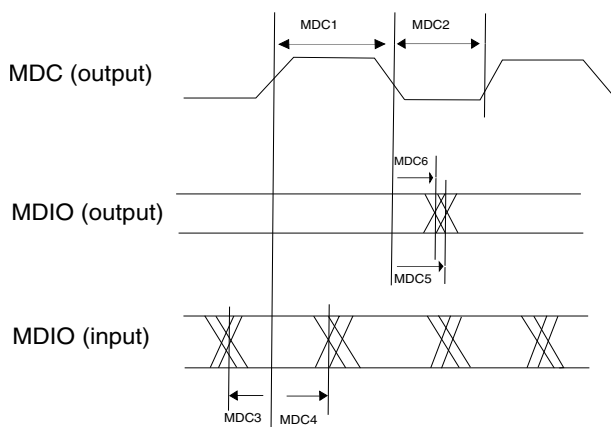
- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 33. Master mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	—	ns
S4	SAI_BCLK pulse width high/low	45%	55%	BCLK period
S5	SAI_RXD input setup before SAI_BCLK	28	—	ns
S6	SAI_RXD input hold after SAI_BCLK	0	—	ns
S7	SAI_BCLK to SAI_TXD output valid	—	8	ns
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	ns
S9	SAI_FS input setup before SAI_BCLK	28	—	ns
S10	SAI_FS input hold after SAI_BCLK	0	—	ns
S11	SAI_BCLK to SAI_FS output valid	—	8	ns
S12	SAI_BCLK to SAI_FS output invalid	-2	—	ns

Table 37. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

**Figure 28. MII/RMII serial management channel timing diagram**

6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specifications

Table 38. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

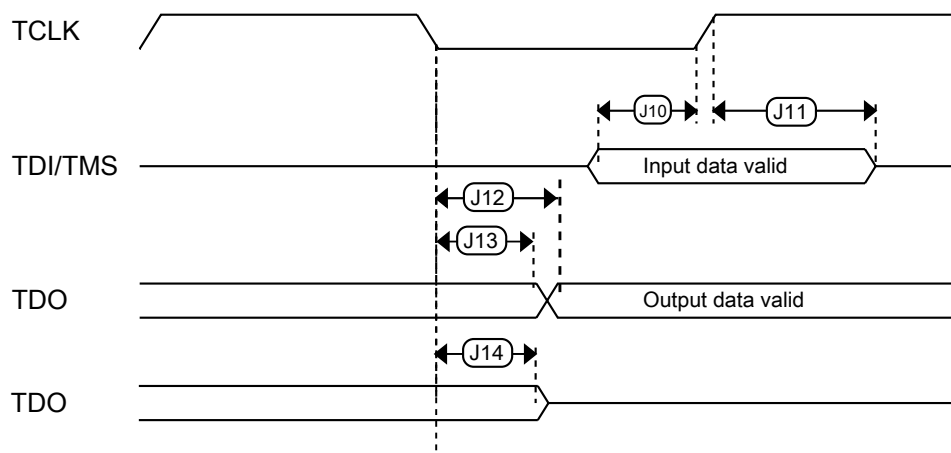


Figure 34. Test Access Port timing

7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

Table 43. Revision History

Rev. No.	Date	Substantial Changes
		- Added footnote 'For S32K11x – FIRC/SOSC/FIRC/LPO; For S32K14x – FIRC/SOSC/FIRC/LPO/SPLL' to 'VLPS Mode: All clock sources disabled' - Updated numbers for: - VLPR → VLPS - VLPS → VLPR 'RUN → Compute operation' - RUN → VLPS - RUN → VLPR - In Power consumption : - Updated specs for S32K142, S32K144, and S32K148 - Updated footnote 'Typical current numbers are indicative ...' - Updated footnote 'The S32K148 data ...' - Removed footnote 'Above S32K148 data is preliminary targets only' - Added new table 'Power consumption at 3.3 V' - In General AC specifications : - Updated max value and footnote of WFRST - Updated symbol for not filtered pulse to 'WNFRST', updated min value, removed max. value, and added footnote - Fixed naming conventions to align with DS in DC electrical specifications at 3.3 V Range and DC electrical specifications at 5.0 V Range - Updated specs for AC electrical specifications at 3.3 V range and AC electrical specifications at 5 V range - In Device clock specifications : - Updated f_{BUS} to 48 for 11x - Added footnote to f_{BUS} for 14x - In External System Oscillator frequency specifications : - Added specs for S32K11x - Updated 't_{dc_extal}' for S32K14x - Added footnote 'Frequencies below ...' to 'f_{ec_extal}' and 't_{dc_extal}' - Splitted Flash timing specifications — commands for S32K14x and S32K11x - Updated Flash timing specifications — commands for S32K14x - In Reliability specifications : - Added footnote 'Data retention period ...' for 'tnvmretp1k' and 'tnvmreteet' - Minor update in footnote for 'nnvmwree16' 'nnvmwree256' - In QuadSPI AC specifications : - Updated 'MCR[SCLKCFG[5]]' value to 0 - Updated 'Data Input Setup Time' HSRUN Internal DQS PAD Loopback value to 1.6 - Updated 'Data Input Setup Time' DDR External DQS min. value to 2 - Updated 'Data Input Hold Time' DDR External DQS min. value to 20 - Updated figure 'QuadSPI output timing (SDR mode) diagram' and 'QuadSPI input timing (HyperRAM mode) diagram' - In 12-bit ADC electrical characteristics : - Added note 'On reduced pin packages where ...' - Removed max. value of 'I_{DDA_ADC}' - Added note 'Due to triple ...' - In 12-bit ADC operating conditions, removed parameter 'ΔV_{DDA}' - In CMP with 8-bit DAC electrical specifications : - Updated Typ. and Max. values of 'I_{DDL5}' - Updated Typ. value of 't_{DHSB}' - Updated Typ. value of 'V_{HYST1}', 'V_{HYST2}', and 'V_{HYST3}' - In LPSPFI electrical specifications : - Updated 'f_{periph}' and 'f_{op}', and 't_{SPSCK}'

Table continues on the next page...