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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	128
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k146hat0mlqt

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. ³	Typ.	Max.	Unit
C_{REF} ^{4, 5}	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} ^{5, 6, 7}	Recommended decoupling capacitance	70	100	—	nF

- V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
- All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
- Minimum recommendation is after considering component aging and tolerance.
- For improved performance, it is recommended to use 10 μ F, 0.1 μ F and 1 nF capacitors in parallel.
- All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
- Contact your local Field Applications Engineer for details on best analog routing practices.
- The filtering used for decoupling the device supplies must comply with the following best practices rules:
 - The protection/decoupling capacitors must be on the path of the trace connected to that component.
 - No trace exceeding 1 mm from the protection to the trace or to the ground.
 - The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
 - The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	μs
	STOP1 → RUN	0.07	0.075	0.08	μs
	STOP2 → RUN	0.07	0.075	0.08	μs
	VLPR → RUN	19	—	26	μs
	VLPR → VLPS	5.1	5.7	6.5	μs
	VLPS → VLPR	18.8	23	27.75	μs
	RUN → Compute operation	0.72	0.75	0.77	μs
	HSRUN → Compute operation	0.3	0.31	0.35	μs
	RUN → STOP1	0.35	0.38	0.4	μs
	RUN → STOP2	0.2	0.23	0.25	μs
	RUN → VLPS	0.3	0.35	0.4	μs
	RUN → VLPR	3.5	3.8	5	μs
	VLPS → Asynchronous DMA Wakeup	105	110	125	μs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	Pin reset → Code execution	—	214	—	μs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes_Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table [Table 7](#). For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

Table 16. Device clock specifications 1 (continued)

Symbol	Description	Min.	Max.	Unit
f_{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) ³				
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40 ⁴	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode ⁵				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section [Feature comparison](#) for the availability of modes and other specifications.
2. Only available on some devices. See section [Feature comparison](#).
3. With SPLL as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

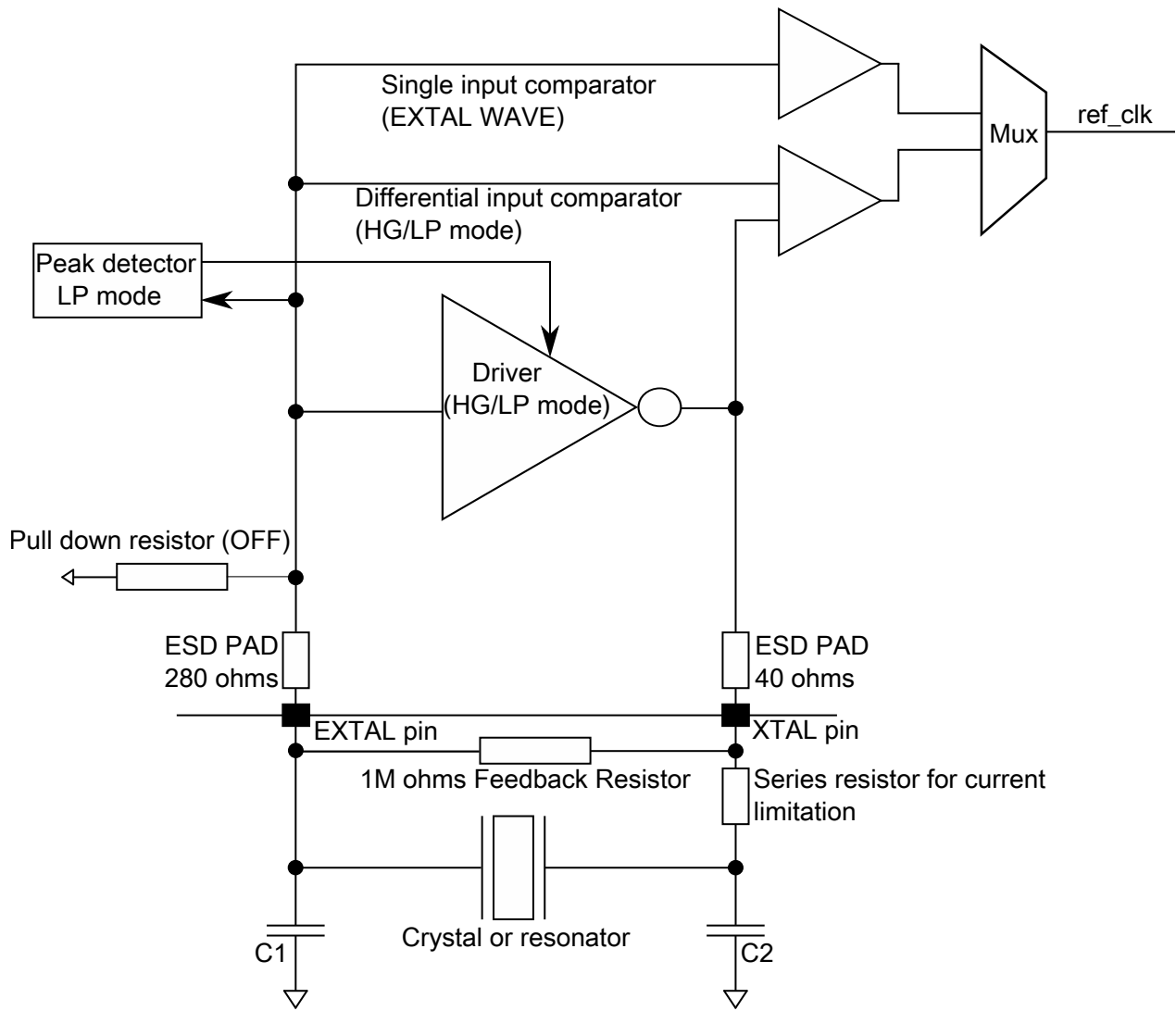


Figure 8. Oscillator connections scheme

Table 17. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g _{mXOSC}	Crystal oscillator transconductance					
	SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz	2.2	—	13.7	mA/V	
	SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz	16	—	47	mA/V	
V _{IL}	Input low voltage — EXTAL pin in external clock mode	V _{SS}	—	1.15	V	
V _{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V _{DD}	—	V _{DD}	V	
C ₁	EXTAL load capacitance	—	—	—		1
C ₂	XTAL load capacitance	—	—	—		1
R _F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

**Table 17. External System Oscillator electrical specifications
(continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when $g_{mXOSC} > 5 * gm_crit$. The gm_crit is defined as:

$$gm_crit = 4 * ESR * (2\pi F)^2 * (C_0 + C_L)^2$$

where:

- g_{mXOSC} is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2 / (C_1 + C_2)]$
- C_s is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

- When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
 - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit	Notes
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
t _{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t _{eevr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	3·4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
t _{eevr16b}	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	3·4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
t _{eevr32bers}	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	μs	
t _{eevr32b}	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	μs	3·4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
t _{quickwr}	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	μs	4·5·6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit	Notes
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
	setting (32-bit write complete, ready for next 32-bit write)	Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550	200	550	200	550		
$t_{\text{quickwrClnup}}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms	7

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 μs , as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

Table 24. Flash command timing specifications for S32K11x

Symbol	Description ¹		S32K116		S32K118		Unit	Notes
			Typ	Max	Typ	Max		
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	0.36	—	0.36	ms	
		64 KB flash	—	—	—	—		
		128 KB flash	—	1.2	—	—		
		256 KB flash	—	—	—	2		
		512 KB flash	—	—	—	—		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	μs	
		4 KB flash	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	100	—	100	μs	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	μs	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	15	300	15	300	ms	2
		64 KB flash	—	—	—	—		
		128 KB flash	120	1100	—	—		
		256 KB flash	—	—	250	2125		
		512 KB flash	—	—	—	—		

Table continues on the next page...

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description ¹		S32K116		S32K118		Unit	Notes
			Typ	Max	Typ	Max		
t _{eewr32b}	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	μs	3·4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
t _{quickwr}	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)	1st 32-bit write	200	550	200	550	μs	4·5·6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550		
		Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550		
t _{quickwrClnup}	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms	7

- All command times assume 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
- Maximum times for erase parameters based on expectations at cycling end-of-life.
- For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
- 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
- Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
- Quick Write times may take up to 550 μs, as additional cleanup may occur when crossing sector boundaries.
- Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

6.3.1.2 Reliability specifications**Table 25. NVM reliability specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	—	—	years	1
η _{nvmcycp}	Cycling endurance	1 K	—	—	cycles	2, 3

Table continues on the next page...

Table 26. QuadSPI electrical specifications

FLASH PORT	Sym	Unit	FLASH A											FLASH B				
			RUN ¹						HSRUN ¹					RUN/HSRUN ²				
			SDR						SDR					SDR		DDR ³		
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS			Internal Sampling		External DQS		
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback	N1		External DQS		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Register Settings																		
MCR[DDR_EN]		-	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
MCR[DQS_EN]		-	0	1	1	0	1	1	0	1	1	0	1	0	1			
MCR[SCLKCFG[0]]		-	-	1	0	-	1	0	-	1	0	-	-	-	-	-	-	-
MCR[SCLKCFG[1]]		-	-	1	0	-	1	0	-	1	0	-	-	-	-	-	-	-
MCR[SCLKCFG[2]]		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
MCR[SCLKCFG[3]]		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
MCR[SCLKCFG[5]]		-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
SMPR[FSPHS]		-	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0
SMPR[FSDLY]		-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SOCCR [SOCCFG[7:0]]			-	0	23	-	0	30	-	0	30	-	-	-	-	-	-	-
SOCCR[SOCCFG[15:8]]		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	30	
FLSHCR[TDH]		-	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x01		
Timing Parameters																		
SCK Clock Frequency	f _{SCK}	MHz	-	38	-	64	-	48	-	40	-	80	-	50	-	20	-	20 ⁴
SCK Clock Period	t _{SCK}	ns	1/SCK	-	1/SCK	-	1/SCK	-	1/SCK	-	1/SCK	-	1/SCK	-	50.0	-	50.0 ⁴	-

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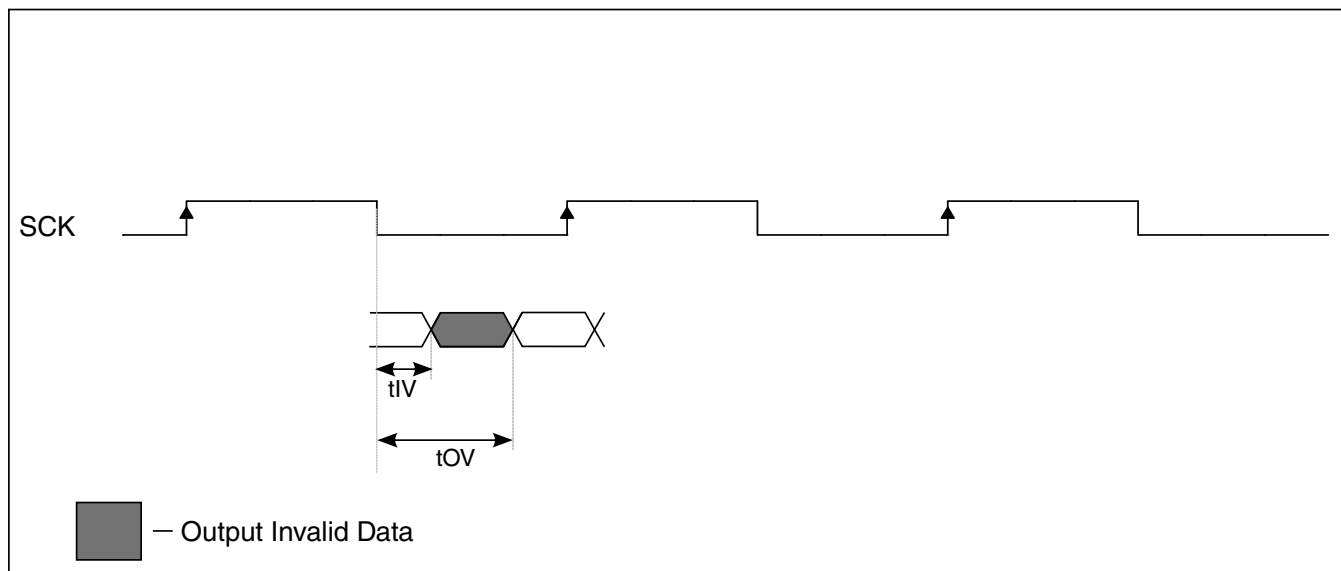


Figure 12. QuadSPI output timing (HyperRAM mode) diagram

6.4 Analog modules

6.4.1 ADC electrical specifications

6.4.1.1 12-bit ADC operating conditions

Table 27. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V_{REFH}	ADC reference voltage high		See Voltage and current operating requirements for values	V_{DDA}	See Voltage and current operating requirements for values	V	2
V_{REFL}	ADC reference voltage low		See Voltage and current operating requirements for values	0	See Voltage and current operating requirements for values	mV	2
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
R_S	Source impedandance	$f_{ADCK} < 4 \text{ MHz}$	—	—	5	k Ω	
R_{SW1}	Channel Selection Switch Impedance		—	0.75	1.2	k Ω	
R_{AD}	Sampling Switch Impedance		—	2	5	k Ω	
C_{P1}	Pin Capacitance		—	10	—	pF	
C_{P2}	Analog Bus Capacitance		—	—	4	pF	
C_S	Sampling capacitance		—	4	5	pF	

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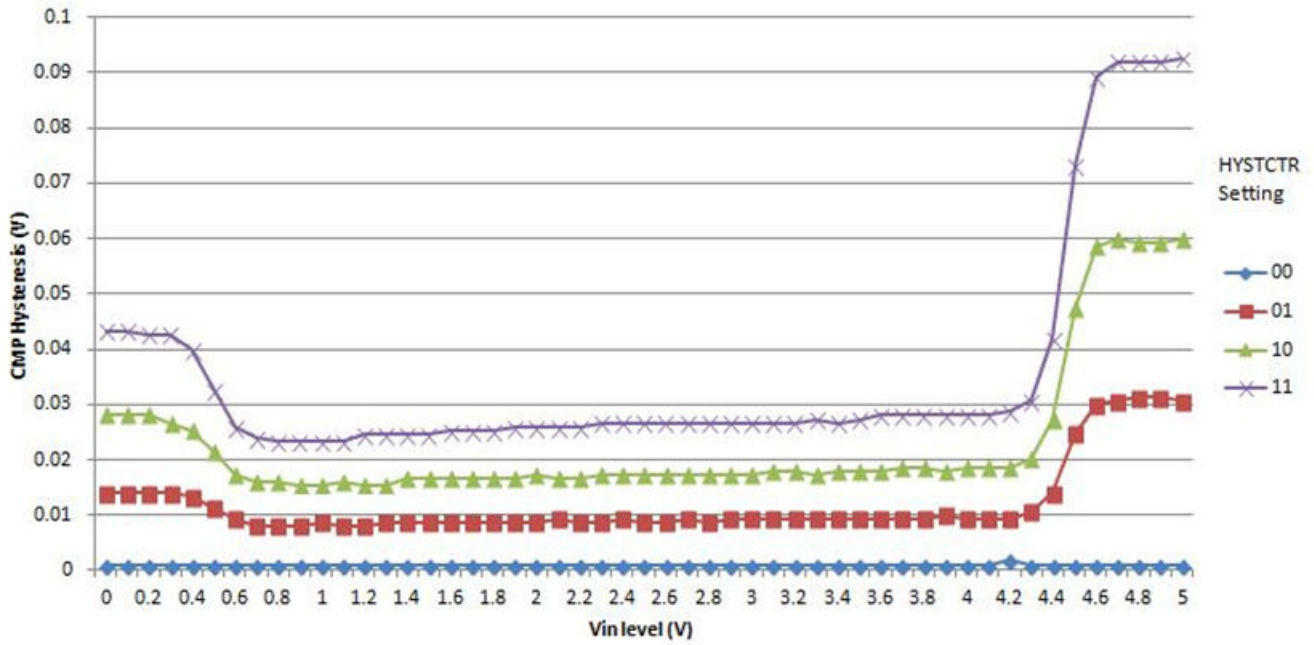


Figure 16. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 0)

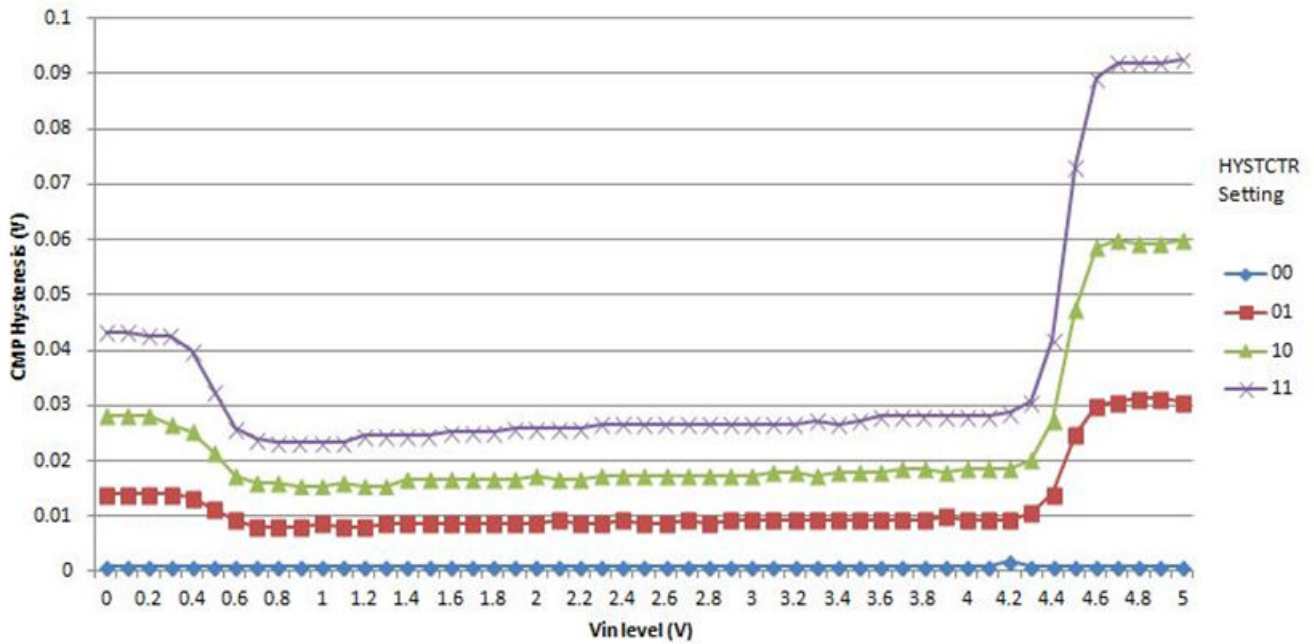


Figure 17. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 1)

Table 32. LPSPI electrical specifications 1 (continued)

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²				VLPR Mode				Unit	
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO			
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
4	t _{Lag} ⁹	Enable lag time (After SPSCCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns	
			Master	(SCKPCS+1)*t _{periph} -25	-	(SCKPCS+1)*t _{periph} -25	-	(SCKPCS+1)*t _{periph} -25	-	(SCKPCS+1)*t _{periph} -25	-	(SCKPCS+1)*t _{periph} -25	-	(SCKPCS+1)*t _{periph} -50	-		(SCKPCS+1)*t _{periph} -50
			Master Loopback ⁵														
			Master Loopback(slow) ⁶														
5	t _{WSPSCCK} ¹⁰	Clock(SPSCCK) high or low time (SPSCCK duty cycle)	Slave	t _{SPSCCK} /2-3	t _{SPSCCK} /2+3	t _{SPSCCK} /2-3	t _{SPSCCK} /2+3	t _{SPSCCK} /2-3	t _{SPSCCK} /2+3	t _{SPSCCK} /2-3	t _{SPSCCK} /2+3	t _{SPSCCK} /2-5	t _{SPSCCK} /2+5	t _{SPSCCK} /2-5	t _{SPSCCK} /2+5	ns	
			Master														
			Master Loopback ⁵														
			Master Loopback(slow) ⁶														
6	t _{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns	
			Master	29	-	38	-	26	-	37 ¹¹ 32 ¹²	-	72	-	78	-		
			Master Loopback ⁵	7	-	8	-	5	-	7	-	20	-	20	-		
			Master Loopback(slow) ⁶	8	-	10	-	7	-	9	-	20	-	20	-		
7	t _{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns	
			Master	0	-	0	-	0	-	0	-	0	-	0	-		
			Master Loopback ⁵	3	-	3	-	2	-	3	-	11	-	11	-		
			Master Loopback(slow) ⁶	3	-	3	-	3	-	3	-	12	-	12	-		

Table continues on the next page...

Table 32. LPSPI electrical specifications¹ (continued)

Num	Symbol	Description	Conditions	Run Mode ²				HSRUN Mode ²				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
8	t_a	Slave access time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
9	t_{dis}	Slave MISO (SOUT) disable time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
10	t_v	Data valid (after SPSCCK edge)	Slave	-	30	-	39	-	26	-	36 ¹¹ 31 ¹²	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback ⁵	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow) ⁶	-	8	-	10	-	7	-	9	-	44	-	44	
11	t_{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback ⁵	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	
			Master Loopback(slow) ⁶	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	$t_{RI/FI}$	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-	-	-	-	-	-	-	-	-	-	-		
			Master Loopback ⁵	-	-	-	-	-	-	-	-	-	-	-		
			Master Loopback(slow) ⁶	-	-	-	-	-	-	-	-	-	-	-		
13	$t_{RO/FO}$	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-	-	-	-	-	-	-	-	-	-	-		
			Master Loopback ⁵	-	-	-	-	-	-	-	-	-	-	-		

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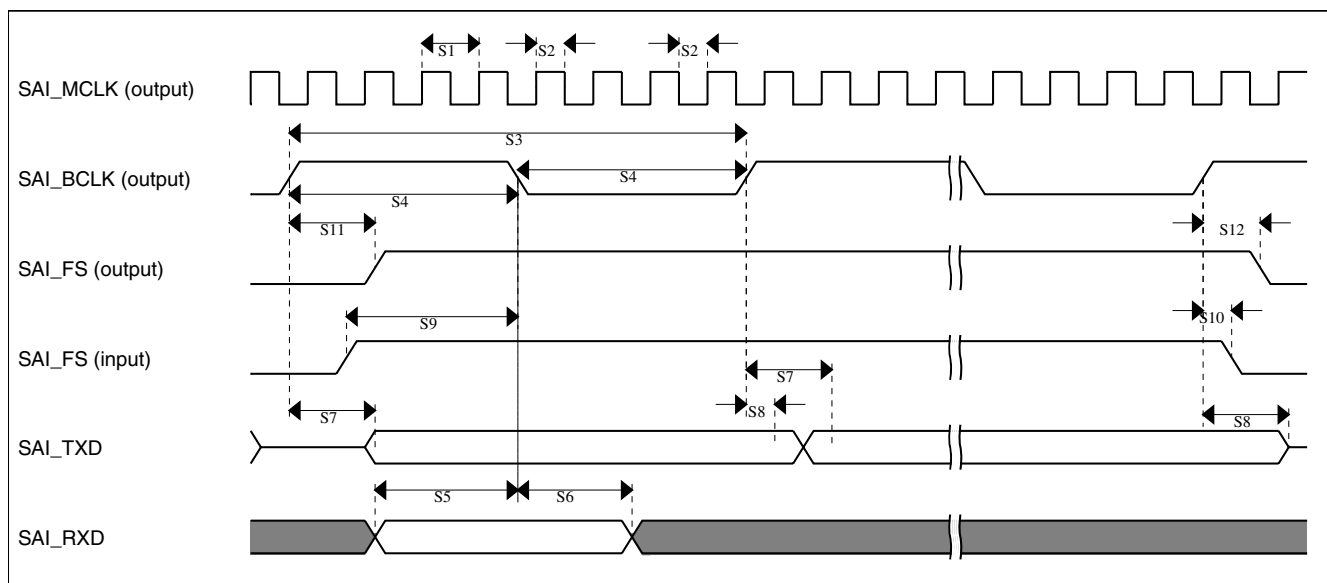


Figure 22. SAI Timing — Master modes

Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14 ¹	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

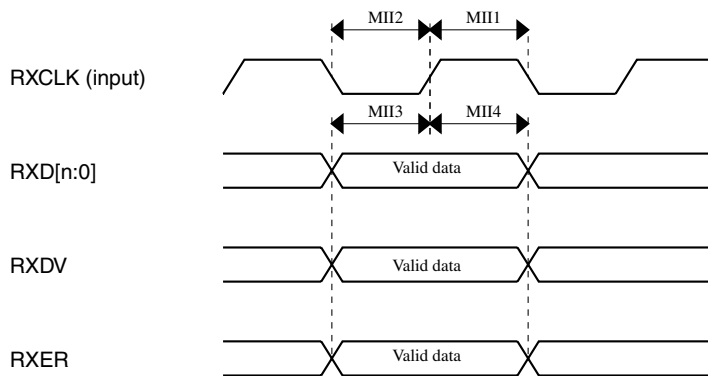


Figure 24. MII receive diagram

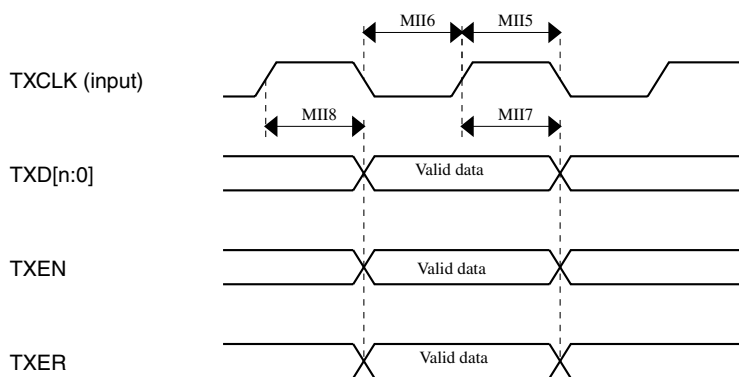


Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 40. JTAG electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
J1	TCLK frequency of operation													MHz
	Boundary Scan	-	20	-	20	-	20	-	20	-	10	-	10	
	JTAG	-	20	-	20	-	20	-	20	-	10	-	10	
J2	TCLK cycle period	1/J1	-	1/J1	-	1/J1	-	1/J1	-	1/J1	-	1/J1	-	ns
J3	TCLK clock pulse width													ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	5	-	5	-	15	-	15	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	5	-	5	-	8	-	8	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	3	-	3	-	15	-	15	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	2	-	2	-	8	-	8	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J , can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package ($^{\circ}\text{C}$)
- $R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)
- $R_{\theta JC}$ = junction to case thermal resistance ($^{\circ}\text{C}/\text{W}$)
- $R_{\theta CA}$ = case to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release
2	03 March 2017	<ul style="list-style-type: none"> • Updated description of QSPI and Clock interfaces in Key Features section • Updated figure: High-level architecture diagram for the S32K1xx family • Updated figure: S32K1xx product series comparison • Added note in section Selecting orderable part number • Updated figure: Ordering information • In table: Absolute maximum ratings : <ul style="list-style-type: none"> • Added footnote to I_{INJPAD_DC} • Updated min and max value of I_{INJPAD_DC} • Updated description, max and min values for I_{INJSUM} • Updated $V_{IN_TRANSIENT}$ • In table: Voltage and current operating requirements : <ul style="list-style-type: none"> • Renamed V_{SUP_OFF} • Updated max value of V_{DD_OFF} • Removed V_{INA} and V_{IN} • Added V_{REFH} and V_{REFL} • Updated footnote "Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V ..." • Removed I_{NJSUM_AF} • Updated footnotes in table Table 4 • Updated section Power mode transition operating behaviors • In table: Power consumption <ul style="list-style-type: none"> • Added footnote "With PMC_REGSC[CLKBIASDIS] ... " • Updated conditions for VLPR • Removed Idd/MHz for S32K144 • Updated numbers for S32K142 and S32K148 • Removed use case footnotes • In section Modes configuration : <ul style="list-style-type: none"> • Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes_Master_configuration_sheet' • In table: DC electrical specifications at 3.3 V Range : <ul style="list-style-type: none"> • Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage • Added footnote to High drive port pins • In table: DC electrical specifications at 5.0 V Range :

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		<ul style="list-style-type: none"> Updated 3.3 V numbers and added footnote against f_{op}, t_{SU}, and t_V in HSRUN Mode Added footnote to 't_{WSPCK}' Updated Thermal characteristics for S32K11x
6	31 Jan 2018	<ul style="list-style-type: none"> Changed the representation of ARM trademark throughout. Removed S32K142 from 'Caution' In 'Key features', added the following note under 'Power management', 'Memory and memory interfaces', and 'Reliability, safety and security': <ul style="list-style-type: none"> No write or erase access to ... In High-level architecture diagram for the S32K14x family, added the following footnote: <ul style="list-style-type: none"> No write or erase access to ... In High-level architecture diagram for the S32K11x family : <ul style="list-style-type: none"> Minor editorial update: Fixed the placement of SRAM, under 'Flash memory controller' block Updated figure: S32K1xx product series comparison : <ul style="list-style-type: none"> Updated footnote 1, and added against 'HSRUN' in addition to 'HW security module (CSEc)' and 'EEPROM emulated by FlexRAM'. Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148. Updated channel count for S32K116 in row '12-bit SAR ADC (1 MSPS each)'. Updated Ordering information Updated Flash timing specifications — commands for S32K148, S32K142, S32K146, S32K116, and S32K118.
7	19 April 2018	<ul style="list-style-type: none"> Changed Caution to Notes <ul style="list-style-type: none"> Updated the wordings of Notes and removed S32K146 Added 'Following two are the available ...' In 'Key features' : <ul style="list-style-type: none"> Editorial updates Updated the note under Power management, Memory and memory interfaces, and Safety and security. Updated FlexIO under Communications interfaces Added ENET and SAI under Communications interfaces Updated Cryptographic Services Engine (CSEc) under 'Safety and security' In High-level architecture diagram for the S32K14x family : <ul style="list-style-type: none"> Minor editorial updates Updated note 3 In High-level architecture diagram for the S32K11x family : <ul style="list-style-type: none"> Minor editorial updates In figure: S32K1xx product series comparison : <ul style="list-style-type: none"> Editorial updates Updated Frequency for S32K14x Updated footnote 4 Added footnote 5 In Ordering information : <ul style="list-style-type: none"> Renamed section, updated the starting paragraph Updated the figure In Voltage and current operating requirements, updated the note In Power consumption : <ul style="list-style-type: none"> Updated specs for S32K146 Removed section 'Modes configuration', and moved its content under the first paragraph. In 12-bit ADC operating conditions :

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes
		<ul style="list-style-type: none"> • Updated specs for T_{JIT} Cycle-to-Cycle jitter to 300 ps • In QuadSPI AC specifications : <ul style="list-style-type: none"> • Updated specs for T_{iv} Data Output In-Valid Time • In figure 'QuadSPI output timing (SDR mode) diagram', marked Invalid area • In CMP with 8-bit DAC electrical specifications : <ul style="list-style-type: none"> • Removed '(VAIO)' from decription of V_{HYST0} • In LPSPi electrical specifications : <ul style="list-style-type: none"> • Added note 'Undefined' in figures 'LPSPi slave mode timing (CPHA = 0)' and 'LPSPi slave mode timing (CPHA = 1)'