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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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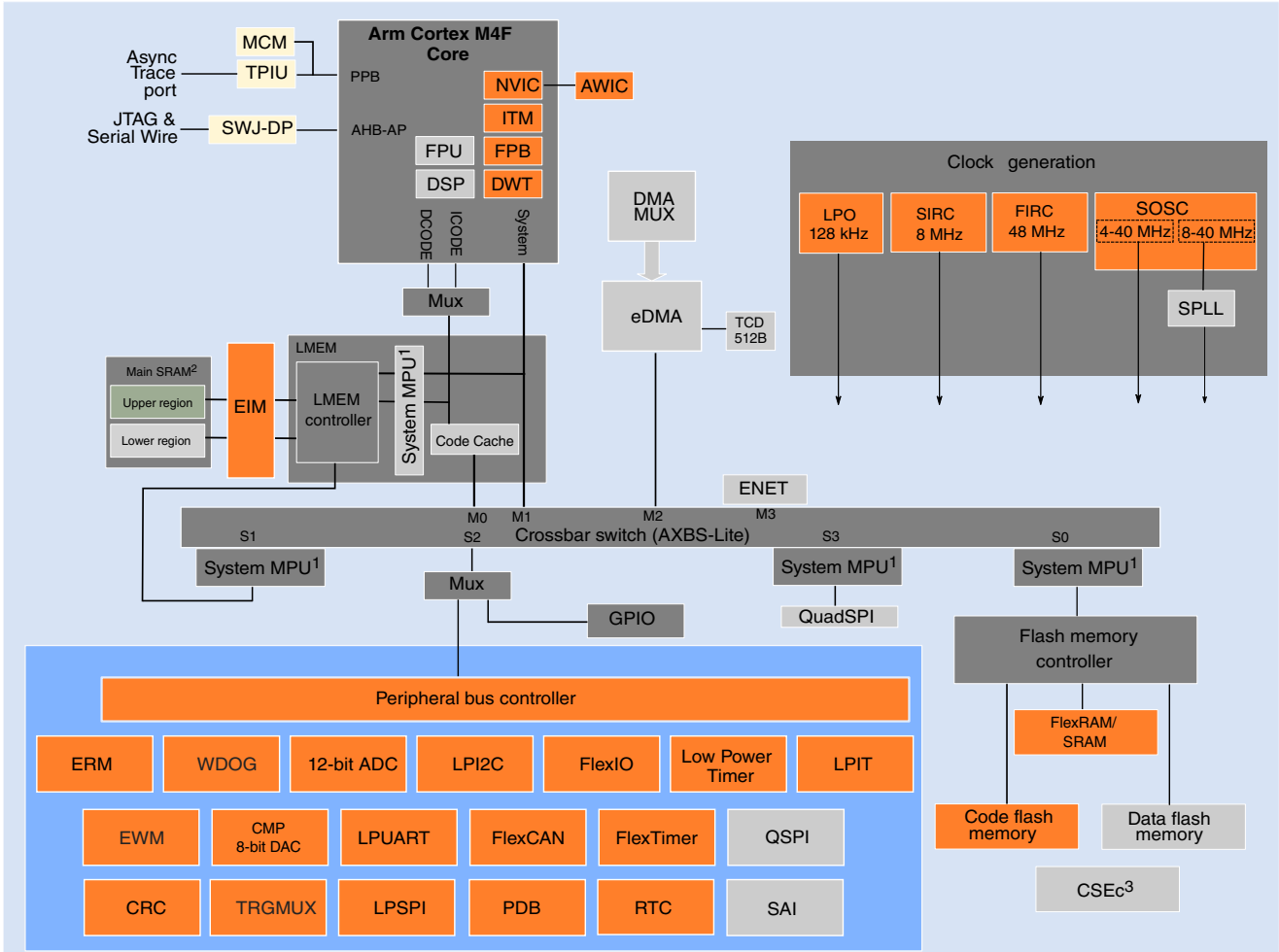
Details

Product Status	Active
Core Processor	ARM® Cortex® -M4F
Core Size	32-Bit Single-Core
Speed	112MHz
Connectivity	CANbus, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	128
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b SAR; D/A1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k146uat0vlqt

- Communications interfaces
 - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
 - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
 - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
 - Up to three FlexCAN modules (with optional CAN-FD support)
 - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
 - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
 - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
 - 128-bit Unique Identification (ID) number
 - Error-Correcting Code (ECC) on flash and SRAM memories
 - System Memory Protection Unit (System MPU)
 - Cyclic Redundancy Check (CRC) module
 - Internal watchdog (WDOG)
 - External Watchdog monitor (EWM) module
- Timing and control
 - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
 - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
 - Two Programmable Delay Blocks (PDB) with flexible trigger system
 - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
 - 32-bit Real Time Counter (RTC)
- Package
 - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

1 Block diagram

Following figures show superset high level architecture block diagrams of S32K14x series and S32K11x series respectively. Other devices within the family have a subset of the features. See [Feature comparison](#) for chip specific values.



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Each Crossbar master (Core, DMA, Ethernet) can be assigned different access rights to each protected memory region. The Arm M4 core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

3: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.

Key:

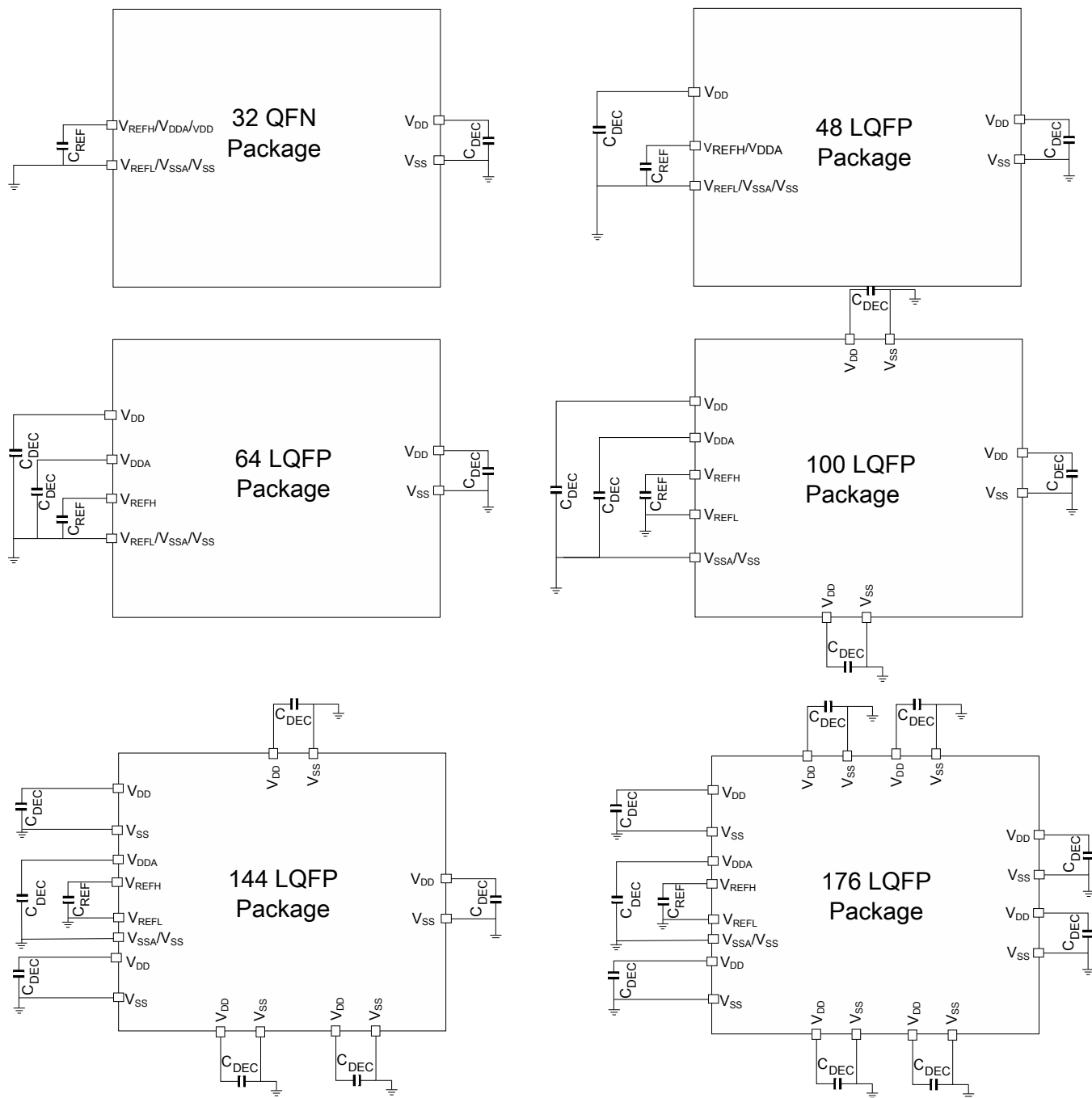
Device architectural IP on all S32K devices

Peripherals present on all S32K devices

Peripherals present on selected S32K devices (see the "Feature Comparison" section)

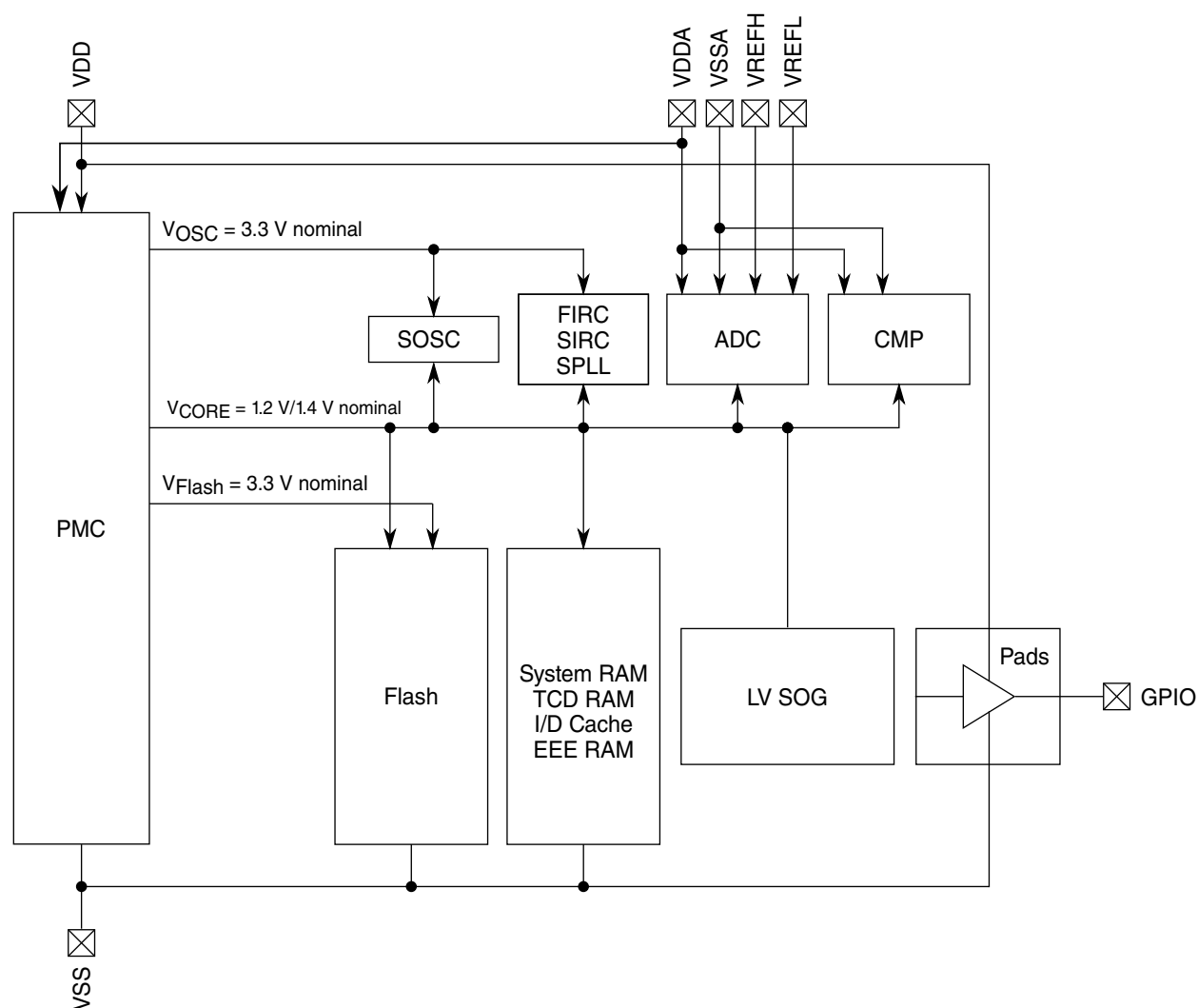
Figure 1. High-level architecture diagram for the S32K14x family

4.4 Power and ground pins



NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB

Figure 5. Pinout decoupling



*Note: VSSA and VSS are shorted at package level

Figure 6. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 5. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	1
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1

Table continues on the next page...

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	μs
	STOP1 → RUN	0.07	0.075	0.08	μs
	STOP2 → RUN	0.07	0.075	0.08	μs
	VLPR → RUN	19	—	26	μs
	VLPR → VLPS	5.1	5.7	6.5	μs
	VLPS → VLPR	18.8	23	27.75	μs
	RUN → Compute operation	0.72	0.75	0.77	μs
	HSRUN → Compute operation	0.3	0.31	0.35	μs
	RUN → STOP1	0.35	0.38	0.4	μs
	RUN → STOP2	0.2	0.23	0.25	μs
	RUN → VLPS	0.3	0.35	0.4	μs
	RUN → VLPR	3.5	3.8	5	μs
	VLPS → Asynchronous DMA Wakeup	105	110	125	μs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	μs
	Pin reset → Code execution	—	214	—	μs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes_Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table [Table 7](#). For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

Table 8. VLPS additional use-case power consumption at typical conditions

Use-case	Description	Temp.	Device						Unit
			S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
VLPS and RTC	Clock source: LPO or RTC_CLKIN	25	TBD	TBD	30	30	30	40	μA
		85	TBD	TBD	110	170	180	240	μA
		105	TBD	TBD	230	330	350	490	μA
		125	TBD	TBD	570	680	810	1250	μA
VLPS and LPUART TX/RX	- Clock source: SIRC - Transmitting or receiving continuously using DMA - Baudrate: 19.2 kbps	25	TBD	TBD	230	230	250	250	μA
		85	TBD	TBD	320	400	410	490	μA
		105	TBD	TBD	490	550	600	850	μA
		125	TBD	TBD	890	1070	1250	1960	μA
VLPS and LPUART wake-up	- Clock source: SIRC - Wake-up address feature enabled - Baudrate: 19.2 kbps	25	TBD	TBD	100	100	110	110	μA
		85	TBD	TBD	170	240	280	350	μA
		105	TBD	TBD	260	400	480	600	μA
		125	TBD	TBD	530	580	1000	1280	μA
VLPS and LPI2C master	- Clock Source: SIRC - Transmit/receive using DMA - Baudrate: 100 kHz	25	TBD	TBD	670	690	820	900	μA
		85	TBD	TBD	880	960	1220	1370	μA
		105	TBD	TBD	1080	1250	1660	2060	μA
		125	TBD	TBD	1970	1980	2860	3690	μA
VLPS and LPI2C slave wake-up	- Clock source: SIRC - Wake-up address feature enabled - Baudrate: 100 kHz	25	TBD	TBD	250	250	270	280	μA
		85	TBD	TBD	340	340	410	510	μA
		105	TBD	TBD	430	430	610	810	μA
		125	TBD	TBD	740	760	1170	1540	μA
VLPS and LPSPi master	- Clock source: SIRC - Transmit/receive using DMA - Baudrate: 500 kHz	25	TBD	TBD	2.99	3.19	3.75	4.11	mA
		85	TBD	TBD	3.26	3.7	4.35	4.93	mA
		105	TBD	TBD	3.5	4.2	4.93	5.74	mA
		125	TBD	TBD	3.93	4.63	5.97	7.38	mA
VLPS and LPiT	- Clock source: SIRC 1 channel enable - Mode: 32-bit periodic counter	25	TBD	TBD	100	100	120	130	μA
		85	TBD	TBD	190	250	260	320	μA
		105	TBD	TBD	310	410	440	570	μA
		125	TBD	TBD	640	750	910	1280	μA

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input $V = V_{SS}$
7. Measured at input $V = V_{DD}$

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max.	Min.	Max.	
tRF _{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
tRF _{GPIO-HD}	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
tRF _{GPIO-FAST}	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max .	Min.	Max.	
tRF _{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
tRF _{GPIO-HD}	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

Table 14. AC electrical specifications at 5 V Range (continued)

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max.	Min.	Max.	
	1	17.3	54.8	17.6	59.7	200
		1.1	4.6	1.1	5.0	25
		2.0	5.7	2.0	5.8	50
		5.4	16.0	5.0	16.0	200
tRF _{GPIO-FAST}	0	0.42	2.2	0.37	2.2	25
		2.0	5.0	1.9	5.2	50
		9.3	18.8	8.5	19.3	200
	1	0.37	0.9	0.35	0.9	25
		1.2	2.7	1.2	2.9	50
		6.0	11.8	6.0	12.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 15. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C _{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to [External System Oscillator electrical specifications](#) for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 16. Device clock specifications 1

Symbol	Description	Min.	Max.	Unit
High Speed run mode ²				
f _{SYS}	System and core clock	—	112	MHz
f _{BUS}	Bus clock	—	56	MHz
f _{FLASH}	Flash clock	—	28	MHz
Normal run mode (S32K11x series)				
f _{SYS}	System and core clock	—	48	MHz
f _{BUS}	Bus clock	—	48	MHz

Table continues on the next page...

Table 18. External System Oscillator frequency specifications

Symbol	Description	Min.		Typ.		Max.		Unit	Notes
		S32K14x	S32K11x	S32K14x	S32K11x	S32K14x	S32K11x		
f _{osc_hi}	Oscillator crystal or resonator frequency	4		—		40		MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—		—		50	48	MHz	1
t _{dc_extal}	Input clock duty cycle (external clock mode)	48		50		52		%	1
t _{cst}	Crystal Start-up Time								
	8 MHz low-gain mode (HGO=0)	—		1.5		—		ms	2
	8 MHz high-gain mode (HGO=1)	—		2.5		—			
	40 MHz low-gain mode (HGO=0)	—		2		—			
	40 MHz high-gain mode (HGO=1)	—		2		—			

1. Frequencies below 40 MHz can be used for degraded duty cycle upto 40-60%
2. Proper PC board layout procedures must be followed to achieve specifications.

6.3.1.1 Flash timing specifications — commands

Table 23. Flash command timing specifications for S32K14x

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit Notes	
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	
		64 KB flash	—	0.5	—	0.5	—	0.5	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	—	2	—	—	—	—	—	—		
		512 KB flash	—	—	—	1.8	—	2	—	2		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	—	75	—	75	μ s	
		4 KB flash	—	100	—	100	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	95	—	95	—	95	—	100	μ s	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	90	225	90	225	μ s	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	—	—	—	—	—	—	—	—	ms	2
		64 KB flash	30	550	30	550	30	550	—	—		
		128 KB flash	—	—	—	—	—	—	—	—		
		256 KB flash	250	2125	—	—	—	—	—	—		
		512 KB flash	—	—	250	4250	250	4250	250	4250		
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	12	130	12	130	ms	2
$t_{pgmseck}$	Program Section execution time (1KB flash)	—	5	—	5	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	2.8	—	2.3	—	5.2	—	8.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	—	30	—	30	μ s	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	90	—	90	—	μ s	
t_{ersall}	Erase All Blocks execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	—	35	—	35	μ s	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2800	400	4900	700	10000	1400	17000	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	70	—	70	—	70	—	—	—	ms	3
		64 KB EEPROM backup	71	—	71	—	71	—	150	—		

Table continues on the next page...

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit Notes	
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
t _{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t _{eevr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
t _{eevr16b}	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	μs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
t _{eevr32bers}	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	μs	
t _{eevr32b}	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	μs	3,4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
t _{quickwr}	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	μs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

6.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See [AN5426](#) for details

Table 28. 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
V_{DDA}	Supply voltage		2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC		—	0.6	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the <i>Reference Manual</i>	ns	
TUE ⁴	Total unadjusted error		—	±4	±8	LSB ⁵	6, 7, 8, 9
DNL	Differential non-linearity		—	±1.0	—	LSB ⁵	6, 7, 8, 9
INL	Integral non-linearity		—	±2.0	—	LSB ⁵	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}=V_{DD}$, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume $V_{DDA} = 3\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 40\text{ MHz}$, $R_{AS}=20\text{ }\Omega$, and $C_{AS}=10\text{ nF}$.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

6.4.2 CMP with 8-bit DAC electrical specifications

Table 31. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DDHS}	Supply current, High-speed mode ¹				μA
	-40 - 125 °C	—	230	300	
I _{DDL}	Supply current, Low-speed mode ¹				μA
	-40 - 105 °C	—	6	11	
	-40 - 125 °C		6	13	
V _{AIN}	Analog input voltage	0	0 - V _{DDA}	V _{DDA}	V
V _{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
V _{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
t _{DHSB}	Propagation delay, High-speed mode ²				ns
	-40 - 105 °C	—	35	200	
	-40 - 125 °C		35	300	
t _{DL}	Propagation delay, Low-speed mode ²				μs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
t _{DH}	Propagation delay, High-speed mode ³				ns
	-40 - 105 °C	—	70	400	
	-40 - 125 °C	—	70	500	
t _{DL}	Propagation delay, Low-speed mode ³				μs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
t _{IDH}	Initialization delay, High-speed mode ⁴				μs
	-40 - 125 °C	—	1.5	3	
t _{IDL}	Initialization delay, Low-speed mode ⁴				μs
	-40 - 125 °C	—	10	30	
V _{HYST0}	Analog comparator hysteresis, Hyst0				mV
	-40 - 125 °C	—	0	—	
V _{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 °C	—	19	66	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 °C	—	15	40	
V _{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 °C	—	34	133	

Table continues on the next page...

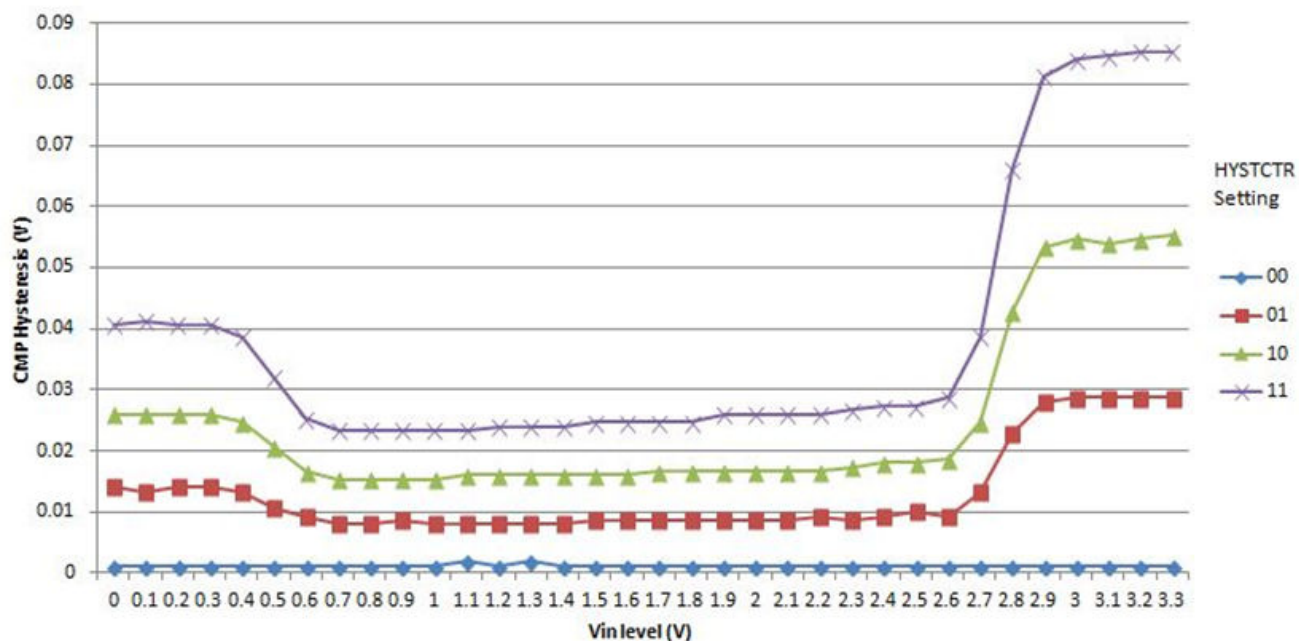


Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)

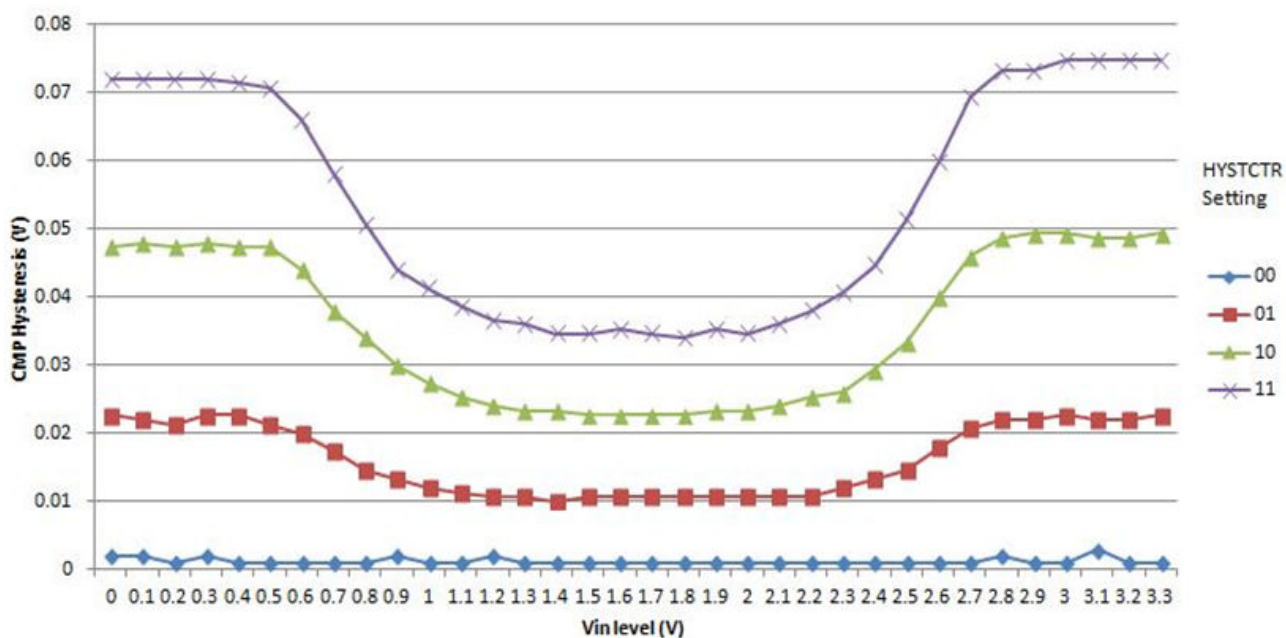


Figure 15. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

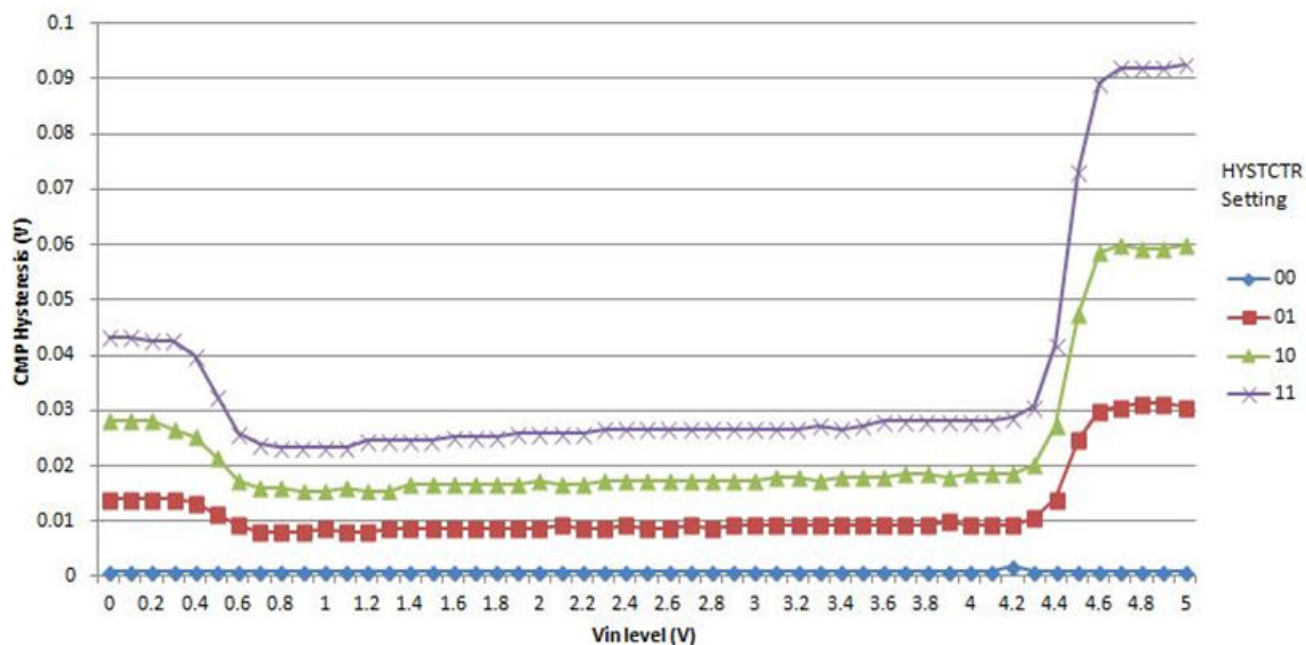


Figure 16. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 0)

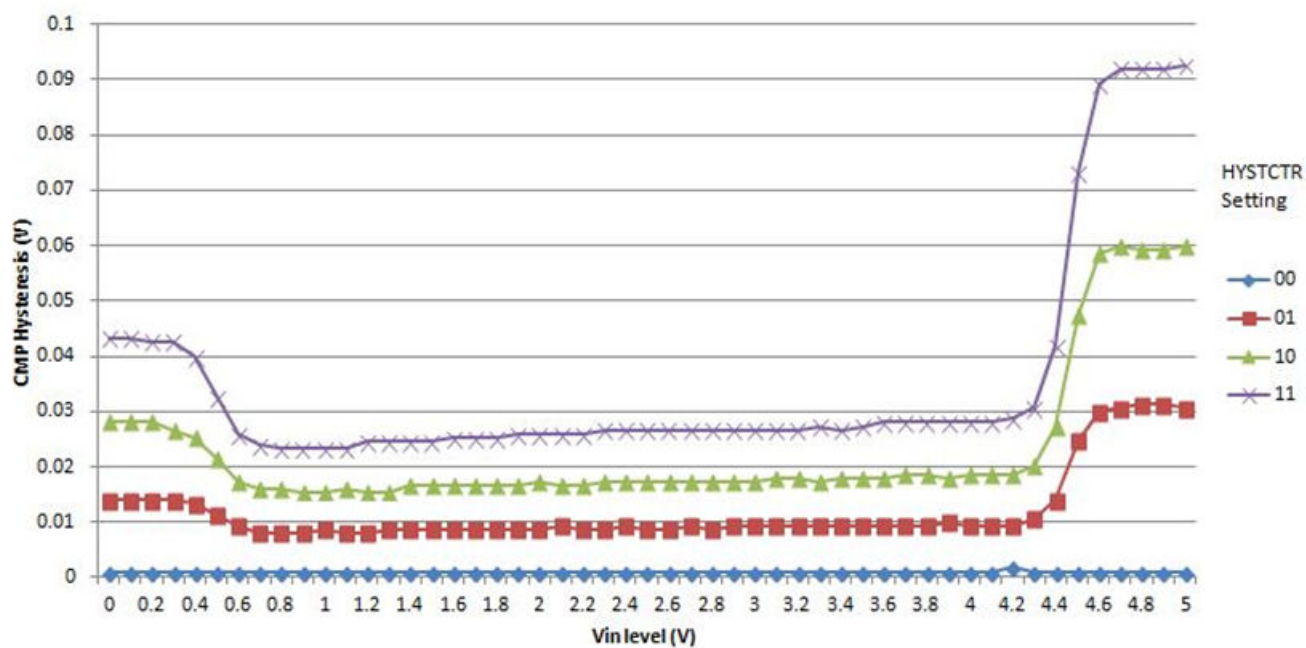


Figure 17. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 1)

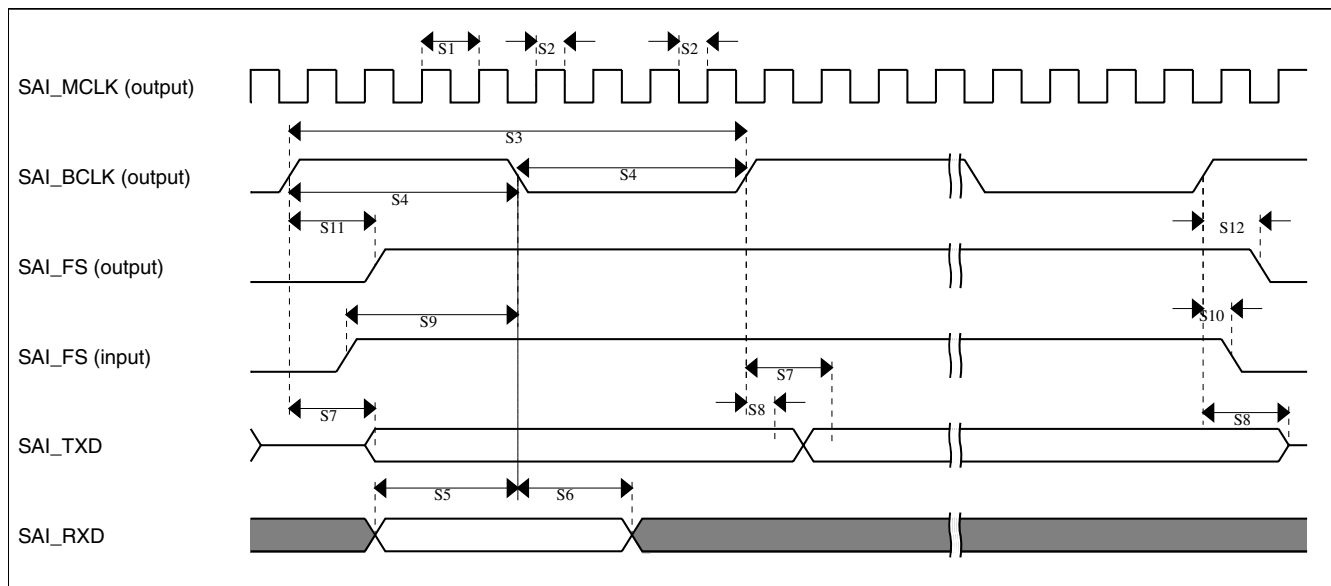


Figure 22. SAI Timing — Master modes

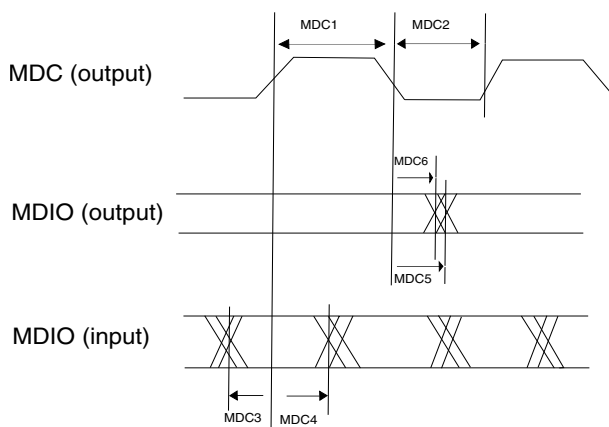
Table 34. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14 ¹	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

Table 37. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

**Figure 28. MII/RMII serial management channel timing diagram**

6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specifications

Table 40. JTAG electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
J1	TCLK frequency of operation													MHz
	Boundary Scan	-	20	-	20	-	20	-	20	-	10	-	10	
	JTAG	-	20	-	20	-	20	-	20	-	10	-	10	
J2	TCLK cycle period	1/J1	-	1/J1	-	1/J1	-	1/J1	-	1/J1	-	1/J1	-	ns
J3	TCLK clock pulse width													ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG													
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	5	-	5	-	15	-	15	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	5	-	5	-	8	-	8	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	3	-	3	-	15	-	15	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	2	-	2	-	8	-	8	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release
2	03 March 2017	- Updated description of QSPI and Clock interfaces in Key Features section - Updated figure: High-level architecture diagram for the S32K1xx family - Updated figure: S32K1xx product series comparison - Added note in section Selecting orderable part number - Updated figure: Ordering information - In table: Absolute maximum ratings : - Added footnote to I_{INJPAD_DC} - Updated min and max value of I_{INJPAD_DC} - Updated description, max and min values for I_{INJSUM} - Updated $V_{IN_TRANSIENT}$ - In table: Voltage and current operating requirements : - Renamed V_{SUP_OFF} - Updated max value of V_{DD_OFF} - Removed V_{INA} and V_{IN} - Added V_{REFH} and V_{REFL} - Updated footnote "Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V ..." - Removed I_{NJSUM_AF} - Updated footnotes in table Table 4 - Updated section Power mode transition operating behaviors - In table: Power consumption - Added footnote "With PMC_REGSC[CLKBIASDIS] ..." - Updated conditions for VLPR - Removed I_{dd}/MHz for S32K144 - Updated numbers for S32K142 and S32K148 - Removed use case footnotes - In section Modes configuration : - Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes_Master_configuration_sheet' - In table: DC electrical specifications at 3.3 V Range : - Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage - Added footnote to High drive port pins - In table: DC electrical specifications at 5.0 V Range :

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Fixed the typo in R_{SW1} - In LPSPi electrical specifications : - Updated t_{Lead} and t_{Lag} - Added footnote in Figure: LPSPi slave mode timing (CPHA = 0) and Figure: LPSPi slave mode timing (CPHA = 1) - In Thermal characteristics : - Updated the name of table: Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package - Deleted specs for $R_{\theta JC}$ for 32 QFN package - Added '$R_{\theta JCBottom}$'
8	18 June 2018	- In attachment 'S32K1xx_Power_Modes_Configuration': - Updated VLPR peripherals disabled and Peripherals Enabled use case #1, using 4 Mhz for System clock, 2 Mhz for bus clock, and 1Mhz for flash. - Removed S32K116 from Notes - In figure: S32K1xx product series comparison : - Added note 'Availability of peripherals depends on the pin availability ...' - Updated 'Ambient Operation Temperature' row - Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148 - In Ordering information : - Updated figure for 'Y: Optional feature' - Updated footnote 3 - In Power and ground pins : - In figure 'Power diagram', updated V_{Flash} frequency to 3.3 V - In Power mode transition operating behaviors : - Updated footnote for 'VLPS Mode: All clock sources disabled' - In Power consumption : - Added IDD's for S32K116 - Added VLPR Peripherals enabled use case 2 at 125 °C/Typicals - Renamed VLPR 'Peripherals enabled' to 'Peripherals enabled use case 1' - Added footnote 'Data collected using RAM' to VLPR 'Peripherals disabled' and VLPR 'Peripherals enabled use case 1' - Updated VLPS Peripherals enabled at 25 °C/Typicals for S32K142 and S32K144 to 40 μA and 42 μA respectively - Added table 'VLPS additional use-case power consumption at typical conditions' - In DC electrical specifications at 3.3 V Range : - Updated naming conventions - Added specs for GPIO-FAST pad - In DC electrical specifications at 5.0 V Range : - Updated naming conventions - Added specs for GPIO-FAST pad - In AC electrical specifications at 3.3 V range : - Updated naming conventions - Added specs for GPIO-FAST pad - In AC electrical specifications at 5 V range : - Updated naming conventions - Added specs for GPIO-FAST pad - In External System Oscillator electrical specifications : - Clarified description of g_{mXOSC} - Updated V_{IL} max. to 1.15 V - In Fast internal RC Oscillator (FIRC) electrical specifications :