Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

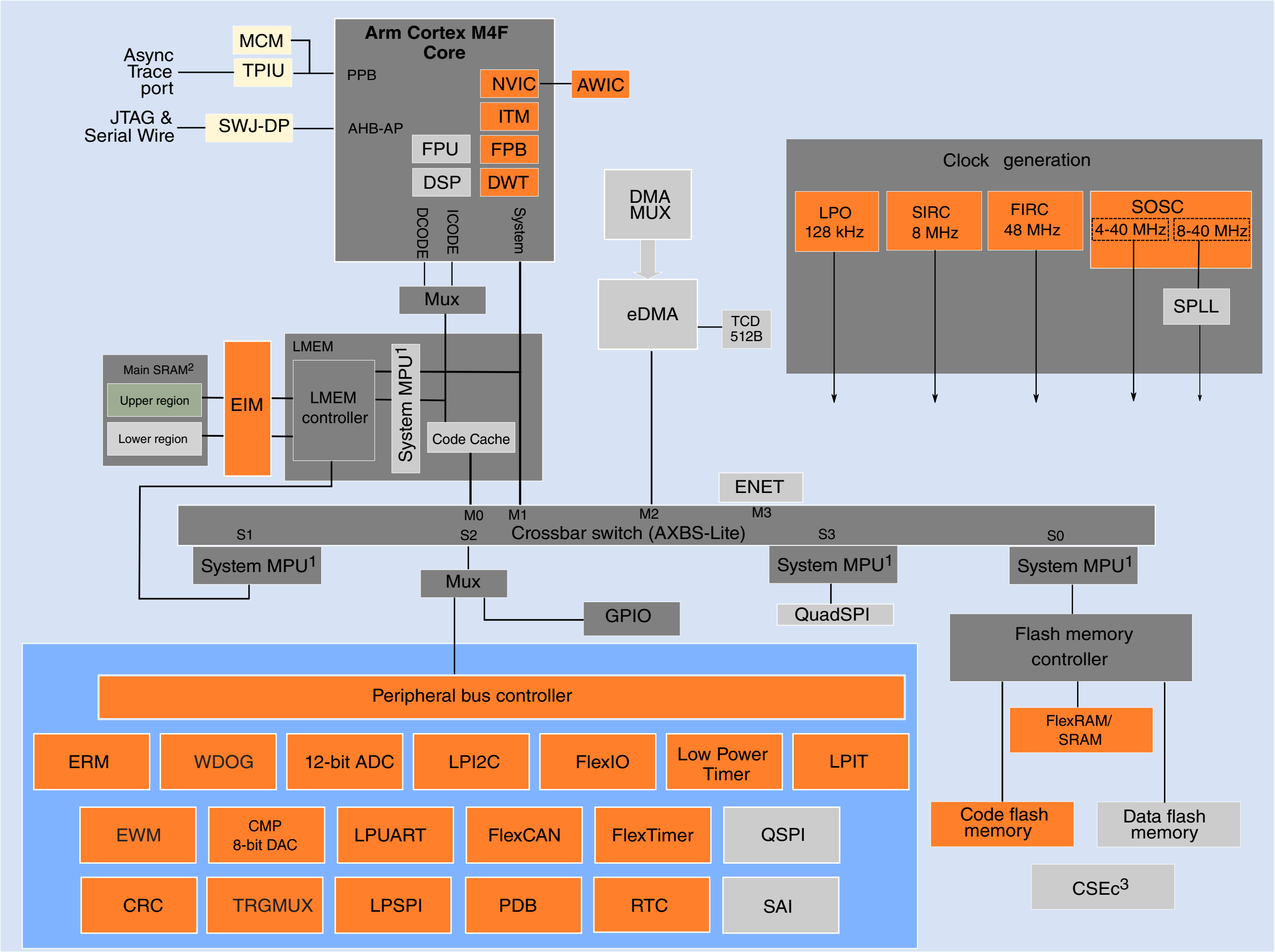
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	128
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b SAR; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k148hat0mlqt

1 Block diagram

Following figures show superset high level architecture block diagrams of S32K14x series and S32K11x series respectively. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Each Crossbar master (Core, DMA, Ethernet) can be assigned different access rights to each protected memory region. The Arm M4 core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

3: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.

Key:

Device architectural IP on all S32K devices

Peripherals present on all S32K devices

Peripherals present on selected S32K devices (see the "Feature Comparison" section)

Figure 1. High-level architecture diagram for the S32K14x family

Description Input Multiplexing sheet(s) attached with Reference Manual.

		S32K11x		S32K14x			
	Parameter	**K116**	**K118**	**K142**	**K144**	**K146**	**K148**
	Core	Arm® Cortex™-M0+		Arm® Cortex™-M4F			
	Frequency	48 MHz		80 MHz (RUN mode) or 112 MHz (HSRUN mode)[1]			
System	IEEE-754 FPU	○		●			
	Cryptographic Services Engine (CSEc)[1]	●		●			
	CRC module	1x		1x			
	ISO 26262	capable up to ASIL-B		capable up to ASIL-B			
	Peripheral speed	up to 48 MHz		up to 112 MHz (HSRUN)			
	Crossbar	●		●			
	DMA	●		●			
	External Watchdog Monitor (EWM)	○		●			
	Memory Protection Unit (MPU)	●		●			
	FIRC CMU	●		○			
	Watchdog	1x		1x			
	Low power modes	●		●			
	HSRUN mode[1]	○		●			
	Number of I/Os	up to 43	up to 58	up to 89		up to 128	up to 156
	Single supply voltage	2.7 - 5.5 V		2.7 - 5.5 V			
	Ambient Operation Temperature (T_a)	-40°C to +105°C / +125°C		-40°C to +105°C / +125°C			
Memory	Flash	128 KB	256 KB	256 KB	512 KB	1 MB	2 MB[2]
	Error Correcting Code (ECC)	●		●			
	System RAM (including FlexRAM and MTB)	17 KB	25 KB	32 KB	64 KB	128 KB	256 KB
	FlexRAM (also available as system RAM)	2 KB		4 KB			
	Cache	○		4 KB			
	EEPROM emulated by FlexRAM[1]	2 KB (up to 32 KB D-Flash)		4 KB (up to 64 KB D-Flash)			See footnote 3
	External memory interface	○		○			QuadSPI incl. HyperBus™
Timer	Low Power Interrupt Timer (LPIT)	1x		1x			
	FlexTimer (16-bit counter) 8 channels	2x (16)		4x (32)		6x (48)	8x (64)
	Low Power Timer (LPTMR)	1x		1x			
	Real Time Counter (RTC)	1x		1x			
	Programmable Delay Block (PDB)	1x		2x			
Analog	Trigger mux (TRGMUX)	1x (43)	1x (45)	1x (64)		1x (73)	1x (81)
	12-bit SAR ADC (1 Msps each)	1x (13)	1x (16)	2x (16)		2x (24)	2x (32)
	Comparator with 8-bit DAC	1x		1x			
Communication	10/100 Mbps IEEE-1588 Ethernet MAC	○		○			1x
	Serial Audio Interface (AC97, TDM, I2S)	○		○			2x
	Low Power UART/LIN (LPUART) (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A, and SAE J2602)	2x		2x	3x		
	Low Power SPI (LPSPI)	1x	2x	2x	3x		
	Low Power I2C (LPI2C)	1x		1x			2x
	FlexCAN (CAN-FD ISO/CD 11898-1)	1x (1x with FD)		2x (1x with FD)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		1x			
IDEs	Debug & trace	SWD, MTB (1 KB), JTAG[4]		SWD, JTAG (ITM, SWV, SWO)			SWD, JTAG (ITM, SWV, SWO), ETM
	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems		NXP S32 Design Studio (GCC) + SDK, IAR, GHS, Arm®, Lauterbach, iSystems			
Other	Packages[5]	32-pin QFN 48-pin LQFP	48-pin LQFP 64-pin LQFP	64-pin LQFP 100-pin LQFP	64-pin LQFP 100-pin LQFP 100-pin MAPBGA	64-pin LQFP 100-pin MAPBGA 100-pin LQFP 144-pin LQFP	100-pin MAPBGA 144-pin LQFP 176-pin LQFP

LEGEND:

○ Not implemented
● Available on the device
1 No write or erase access to Flash module, including Security (CSEc) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.
2 Available when EEEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
3 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.
4 Only for Boundary Scan Register
5 See Dimensions section for package drawings

Figure 3. S32K1xx product series comparison

4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate and the ramp rate assumes that the S32K1xx HW design guidelines in AN5426 are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. T_J (Junction temperature)=135 °C. Assumes T_A=125 °C for RUN mode

   T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

   - Assumes maximum θJA for 2s2p board. See Thermal characteristics
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

Device functionality is guaranteed up to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.7 V

Table 2. Voltage and current operating requirements [1]

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	4
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH}$ = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.

5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
6. Open drain outputs must be pulled to V_{DD}.
7. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.

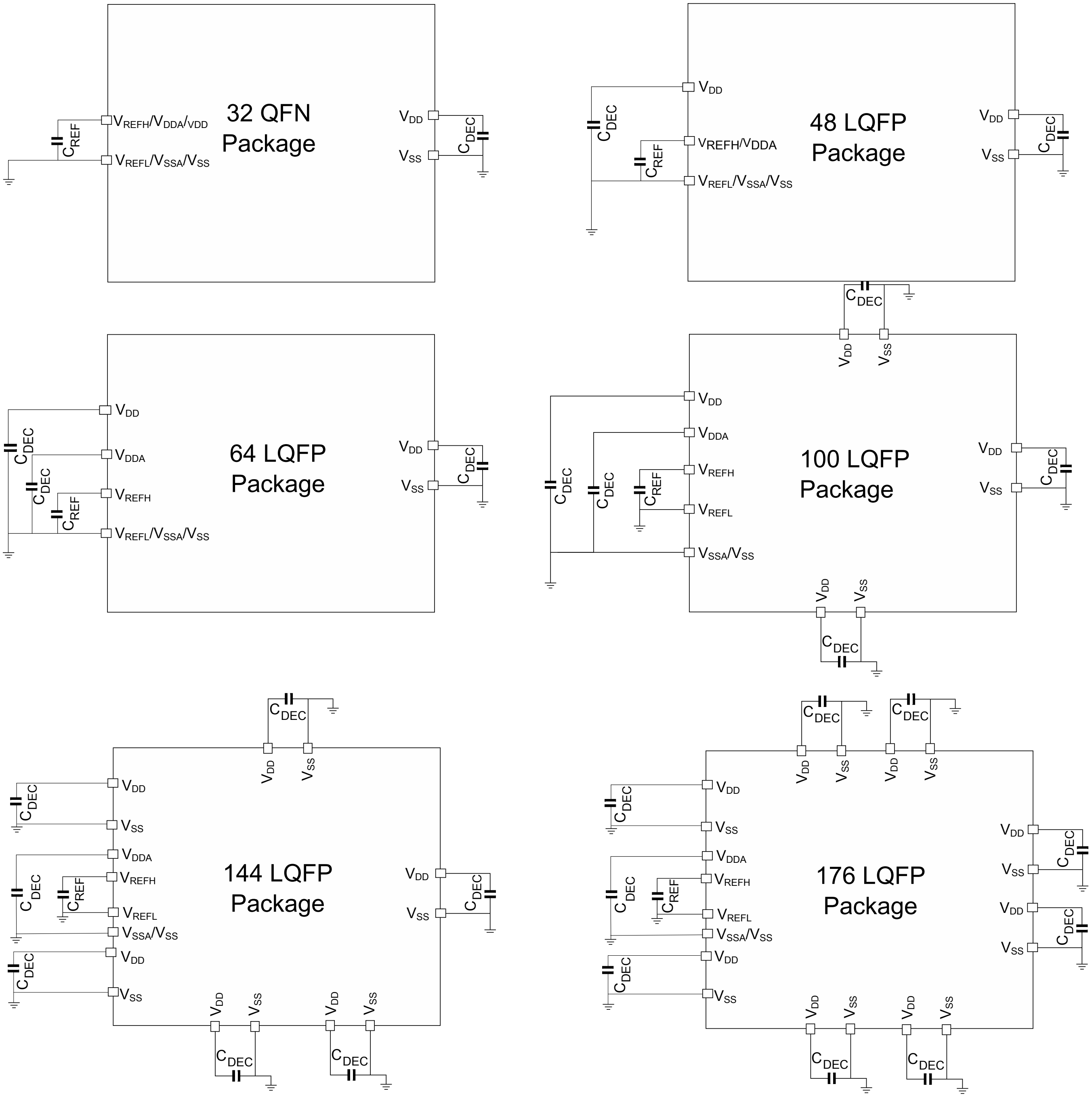
4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP, 100 LQFP, and 100 MAP-BGA packages.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ \text{C-Grade Part}}$	Ambient temperature under bias	–40	—	85[1]	℃
$T_{J\ \text{C-Grade Part}}$	Junction temperature under bias	–40	—	105[1]	℃
$T_{A\ \text{V-Grade Part}}$	Ambient temperature under bias	–40	—	105[1]	℃
$T_{J\ \text{V-Grade Part}}$	Junction temperature under bias	–40	—	125[1]	℃
$T_{A\ \text{M-Grade Part}}$	Ambient temperature under bias	–40	—	125[2]	℃
$T_{J\ \text{M-Grade Part}}$	Junction temperature under bias	–40	—	135[2]	℃

1. Values mentioned are measured at ≤ 112 MHz in HSRUN mode.
2. Values mentioned are measured at ≤ 80 MHz in RUN mode.

4.4 Power and ground pins



NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB

Figure 5. Pinout decoupling

Table 4. Supplies decoupling capacitors [1], [2]

Symbol	Description	Min. [3]	Typ.	Max.	Unit
C_{REF}, [4], [5]	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC}[5], [6], [7]	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
    - The protection/decoupling capacitors must be on the path of the trace connected to that component.
    - No trace exceeding 1 mm from the protection to the trace or to the ground.
    - The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
    - The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.

Table 7. Power consumption (Typicals unless stated otherwise) [1]

Chip/Device	Ambient Temperature (°C)		VLPS (µA) [2]		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [3]		IDD/MHz (µA/MHz) [4]
			Peripherals disabled [5]	Peripherals enabled	Peripherals disabled [6]	Peripherals enabled use case 1 [6]	Peripherals enabled use case 2 [7]			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
S32K116	25	Typ	26	40	1.05	1.07	TBD	6.3	7.2	11.8	20.3	NA						245
	85	Typ	76	93	1.1	1.11	TBD	6.6	7.5	12	20.6							251
		Max	287	300	1.39	1.4	NA	8	8.9	13.4	22.1							279
	105	Typ	139	164	1.15	1.16	TBD	6.8	7.7	12.3	20.8							255
		Max	590	603	1.68	1.69	NA	9.2	10.1	14.5	23.1							302
	125	Typ	NA	NA	NA	NA	TBD	NA	NA	NA	NA							NA
		Max	891	904	2.02	2.04	NA	10.4	11.3	15.6	24.1							325
S32K118	25	Typ	26	38	1.9	2.5	TBD	7	12	TBD	TBD	NA						TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	42							TBD
S32K142	25	Typ	29	40	1.17	1.21	2.19	6.4	7.4	17.3	24.6	24.5	31.3	28.8	37.5	40.5	52.2	360
	85	Typ	128	137	1.48	1.51	2.31	7	8	17.6	24.9	25	31.6	29.1	37.7	41.1	52.5	364
		Max	335	360	1.87	1.89	NA	8.6	9.4	22	28.2	26.9	33.5	32	40	44	55.6	400
	105	Typ	240	257	1.58	1.61	2.44	7.6	8.3	18.3	25.7	25.5	31.9	29.8	38	41.5	53.1	373
		Max	740	791	2.32	2.34	NA	9.9	10.9	23.1	30.2	27.8	35.3	33.8	40.7	44.9	57.4	423
	125	Typ	NA	NA	NA	NA	2.84	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA

Table continues on the next page...

Table 7. Power consumption (Typicals unless stated otherwise) [1] (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (µA) [2]		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [3]		IDD/MHz (µA/MHz) [4]
			Peripherals disabled [5]	Peripherals enabled	Peripherals disabled [6]	Peripherals enabled use case 1[6]	Peripherals enabled use case 2[7]			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
		Max	1660	1736	3.48	3.55	NA	14.5	15.6	34.8	43.6	41.9	53.9	48.7	65.1	70.4	96.1	609
	105	Typ	560	577	2.49	2.54	4.03	10.9	11.9	29.8	37.8	37.6	47.5	45.2	61.5	63.8	89.1	565
		Max	2945	2970	4.40	4.47	NA	18.0	19.0	38.4	46.8	44.9	55.3	51.6	66.8	73.6	97.4	645
	125	Typ	NA	NA	NA	NA	4.85	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3990	4166	6.00	6.08	NA	23.4	24.5	44.3	52.5	50.9	61.3	57.5	71.6	NA		719

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and On-chip pulldown is enabled for all unused input pins.
2. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
3. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
4. Values mentioned for S32K14x devices are measured at RUN@80 MHz with peripherals disabled and values mentioned for S32K11x devices are measured at RUN@48 MHz with peripherals disabled.
5. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
6. Data collected using RAM
7. Numbers on limited samples size and data collected with Flash
8. The S32K148 data points assume that ENET/QuadSPI/SAI etc. are inactive.

Table 8. VLPS additional use-case power consumption at typical conditions

Use-case	Description	Temp.	Device						Unit
			S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
VLPS and RTC	• Clock source: LPO or RTC_CLKIN	25	TBD	TBD	30	30	30	40	µA
		85	TBD	TBD	110	170	180	240	µA
		105	TBD	TBD	230	330	350	490	µA
		125	TBD	TBD	570	680	810	1250	µA
VLPS and LPUART TX/RX	• Clock source: SIRC • Transmiting or receiving continuously using DMA • Baudrate: 19.2 kbps	25	TBD	TBD	230	230	250	250	µA
		85	TBD	TBD	320	400	410	490	µA
		105	TBD	TBD	490	550	600	850	µA
		125	TBD	TBD	890	1070	1250	1960	µA
VLPS and LPUART wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 19.2 kbps	25	TBD	TBD	100	100	110	110	µA
		85	TBD	TBD	170	240	280	350	µA
		105	TBD	TBD	260	400	480	600	µA
		125	TBD	TBD	530	580	1000	1280	µA
VLPS and LPI2C master	• Clock Source: SIRC • Transmit/receive using DMA • Baudrate: 100 kHz	25	TBD	TBD	670	690	820	900	µA
		85	TBD	TBD	880	960	1220	1370	µA
		105	TBD	TBD	1080	1250	1660	2060	µA
		125	TBD	TBD	1970	1980	2860	3690	µA
VLPS and LPI2C slave wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 100 kHz	25	TBD	TBD	250	250	270	280	µA
		85	TBD	TBD	340	340	410	510	µA
		105	TBD	TBD	430	430	610	810	µA
		125	TBD	TBD	740	760	1170	1540	µA
VLPS and LPSPI master	• Clock source: SIRC • Transmit/receive using DMA • Baudrate: 500 kHz	25	TBD	TBD	2.99	3.19	3.75	4.11	mA
		85	TBD	TBD	3.26	3.7	4.35	4.93	mA
		105	TBD	TBD	3.5	4.2	4.93	5.74	mA
		125	TBD	TBD	3.93	4.63	5.97	7.38	mA
VLPS and LPIT	• Clock source: SIRC • 1 channel enable • Mode: 32-bit periodic counter	25	TBD	TBD	100	100	120	130	µA
		85	TBD	TBD	190	250	260	320	µA
		105	TBD	TBD	310	410	440	570	µA
		125	TBD	TBD	640	750	910	1280	µA

Table 14. AC electrical specifications at 5 V Range (continued)

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
		17.3	54.8	17.6	59.7	200
	1	1.1	4.6	1.1	5.0	25
		2.0	5.7	2.0	5.8	50
		5.4	16.0	5.0	16.0	200
$tRF_{GPIO-FAST}$	0	0.42	2.2	0.37	2.2	25
		2.0	5.0	1.9	5.2	50
		9.3	18.8	8.5	19.3	200
	1	0.37	0.9	0.35	0.9	25
		1.2	2.7	1.2	2.9	50
		6.0	11.8	6.0	12.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 15. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 16. Device clock specifications [1]

Symbol	Description	Min.	Max.	Unit
High Speed run mode[2]				
f_{SYS}	System and core clock	—	112	MHz
f_{BUS}	Bus clock	—	56	MHz
f_{FLASH}	Flash clock	—	28	MHz
Normal run mode (S32K11x series)				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	48	MHz

Table continues on the next page...

Table 18. External System Oscillator frequency specifications

<table>
<tr><th rowspan="2">Symbol</th><th rowspan="2">Description</th><th colspan="2">Min.</th><th colspan="2">Typ.</th><th colspan="2">Max.</th><th rowspan="2">Unit</th><th rowspan="2">Notes</th></tr>
<tr><th>S32K14x</th><th>S32K11x</th><th>S32K14x</th><th>S32K11x</th><th>S32K14x</th><th>S32K11x</th></tr>
<tr><td>f_{osc_hi}</td><td>Oscillator crystal or resonator frequency</td><td colspan="2">4</td><td colspan="2">—</td><td colspan="2">40</td><td>MHz</td><td></td></tr>
<tr><td>f_{ec_extal}</td><td>Input clock frequency (external clock mode)</td><td colspan="2">—</td><td colspan="2">—</td><td>50</td><td>48</td><td>MHz</td><td>1</td></tr>
<tr><td>t_{dc_extal}</td><td>Input clock duty cycle (external clock mode)</td><td colspan="2">48</td><td colspan="2">50</td><td colspan="2">52</td><td>%</td><td>1</td></tr>
<tr><td rowspan="5">t_{cst}</td><td colspan="9">Crystal Start-up Time</td></tr>
<tr><td>8 MHz low-gain mode (HGO=0)</td><td colspan="2">—</td><td colspan="2">1.5</td><td colspan="2">—</td><td rowspan="4">ms</td><td rowspan="4">2</td></tr>
<tr><td>8 MHz high-gain mode (HGO=1)</td><td colspan="2">—</td><td colspan="2">2.5</td><td colspan="2">—</td></tr>
<tr><td>40 MHz low-gain mode (HGO=0)</td><td colspan="2">—</td><td colspan="2">2</td><td colspan="2">—</td></tr>
<tr><td>40 MHz high-gain mode (HGO=1)</td><td colspan="2">—</td><td colspan="2">2</td><td colspan="2">—</td></tr>
</table>

1. Frequencies below 40 MHz can be used for degraded duty cycle upto 40-60%
2. Proper PC board layout procedures must be followed to achieve specifications.

Table 25. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using FlexMemory feature : FlexRAM as Emulated EEPROM						
$t_{nvmretee}$	Data retention	5	—	—	years	4
	Write endurance					5, 6, 7
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	100 K	—	—	writes	
$n_{nvmwree256}$	• EEPROM backup to FlexRAM ratio = 256	1.6 M	—	—	writes	

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
3. Cycling endurance is per DFlash or PFlash Sector.
4. Data retention period per block begins upon initial user factory programming or after each subsequent erase. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.
5. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across product temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
6. For usage of any EEE driver other than the FlexMemory feature, the endurance spec will fall back to the specified endurance value of the D-Flash specification (1K).
7. FlexMemory calculator tool is available at NXP web site for help in estimation of the maximum write endurance achievable at specific EEPROM/FlexRAM ratios. The “In Spec” portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- QuadSPI trace length should be 3 inches.
- For non-Quad mode of operation if external device doesn’t have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

Table 26. QuadSPI electrical specifications

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Register Settings																		
MCR[DDR_EN]		-	0		0		0		0		0		0		0		1	
MCR[DQS_EN]		-	0		1		1		0		1		1		0		1	
MCR[SCLKCFG[0]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[1]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[2]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[3]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[5]]		-	0		0		0		0		0		0		0		1	
SMPR[FSPHS]		-	0		1		0		0		1		0		0		0	
SMPR[FSDLY]		-	0		0		0		0		0		0		0		0	
SOCCR [SOCCFG[7:0]]			-		0		23		-		0		30		-		-	
SOCCR[SOCCFG[15:8]]		-	-		-		-		-		-		-		-		30	
FLSHCR[TDH]		-	0x00		0x00		0x00		0x00		0x00		0x00		0x00		0x01	
Timing Parameters																		
SCK Clock Frequency	f_{SCK}	MHz	-	38	-	64	-	48	-	40	-	80	-	50	-	20	-	20[4]
SCK Clock Period	t_{SCK}	ns	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	50.0	-	50.0[4]	-

Table continues on the next page...

Table 26. QuadSPI electrical specifications (continued)

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCK Duty Cycle	t_{SDC}	ns	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 0.750	tSCK/2 - 0.750	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 2.5	tSCK/2 + 2.5	tSCK/2 - 2.5	tSCK/2 + 2.5
Data Input Setup Time	t_{IS}	ns	15	-	2.5	-	10	-	14	-	1.6	-	9	-	25	-	2	-
Data Input Hold Time	t_{IH}	ns	0	-	1	-	1	-	0	-	1	-	1	-	0	-	20	-
Data Output Valid Time	t_{OV}	ns	-	4.5	-	4.5	-	4.5	-	4	-	4	-	4	-	10	-	10
Data Output In-Valid Time	t_{IV}	ns	-	5	-	5	-	5	-	5	-	3[5]	-	5	-	5	5	-
CS to SCK Time [6]	t_{CSSCK}	ns	5	-	5	-	5	-	5	-	5	-	5	-	10	-	10	-
SCK to CS Time [7]	t_{SCKCS}	ns	5	-	5	-	5	-	5	-	5	-	5	-	5	-	5	-
Output Load		pf	25		25		25		25		25		25		25		25	

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz,Output invalid time is 5 ns.
6. Program register value QuadSPI_FLSHCR[TCSS] = 4`h2
7. Program register value QuadSPI_FLSHCR[TCSH] = 4`h1

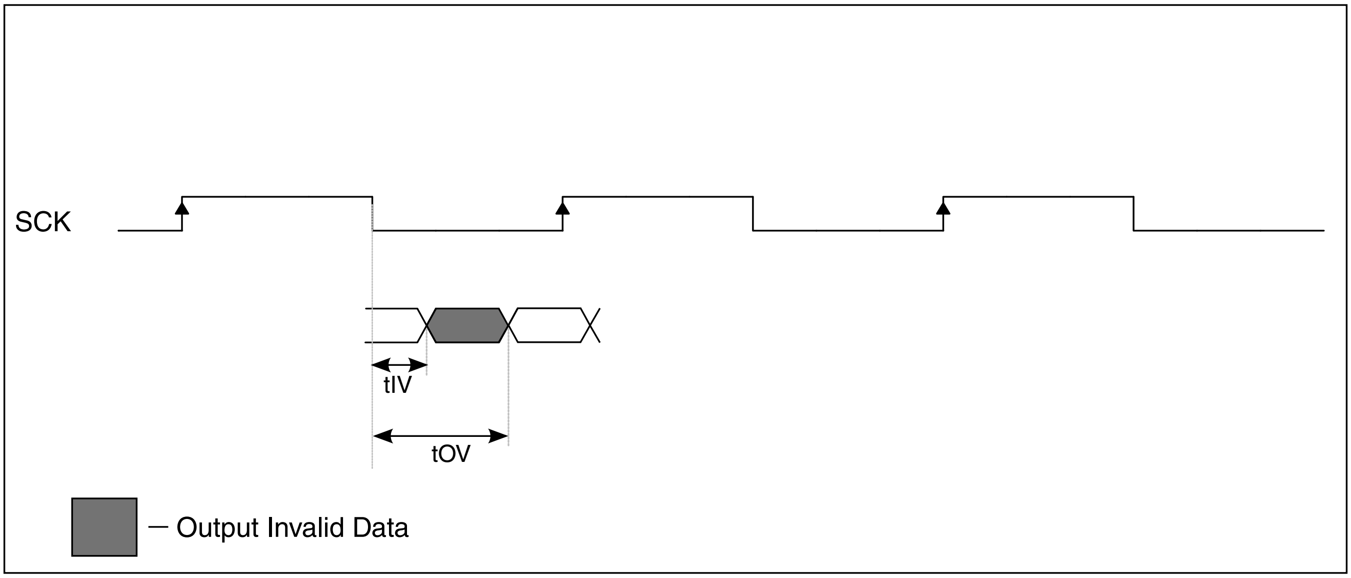


Figure 12. QuadSPI output timing (HyperRAM mode) diagram

6.4 Analog modules

6.4.1 ADC electrical specifications

6.4.1.1 12-bit ADC operating conditions

Table 27. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{REFH}	ADC reference voltage high		See Voltage and current operating requirements for values	V_{DDA}	See Voltage and current operating requirements for values	V	2
V_{REFL}	ADC reference voltage low		See Voltage and current operating requirements for values	0	See Voltage and current operating requirements for values	mV	2
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
R_S	Source impedendance	$f_{ADCK} < 4$ MHz	—	—	5	kΩ	
R_{SW1}	Channel Selection Switch Impedance		—	0.75	1.2	kΩ	
R_{AD}	Sampling Switch Impedance		—	2	5	kΩ	
C_{P1}	Pin Capacitance		—	10	—	pF	
C_{P2}	Analog Bus Capacitance		—	—	4	pF	
C_S	Sampling capacitance		—	4	5	pF	

Table continues on the next page...

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 32. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
8	t_a	Slave access time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
9	t_{dis}	Slave MISO (SOUT) disable time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
10	t_v	Data valid (after SPSCK edge)	Slave	-	30	-	39	-	26	-	36 [11] 31 [12]	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback[5]	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow)[6]	-	8	-	10	-	7	-	9	-	44	-	44	
11	t_{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback[5]	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	
			Master Loopback(slow)[6]	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	$t_{RI/FI}$	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		
			Master Loopback[5]	-		-		-		-		-		-		
			Master Loopback(slow)[6]	-		-		-		-		-		-		
13	$t_{RO/FO}$	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		
			Master Loopback [5]	-		-		-		-		-		-		

Table continues on the next page...

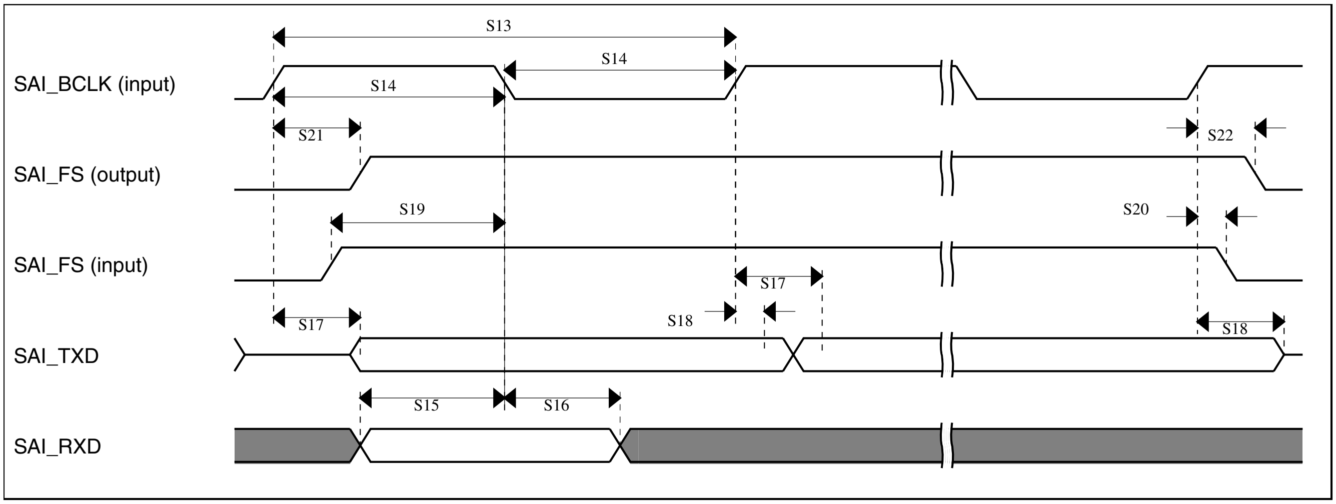


Figure 23. SAI Timing — Slave modes

6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 35. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

Table 38. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

Table 43. Revision History

<table>
<tr><th>Rev. No.</th><th>Date</th><th>Substantial Changes</th></tr>
<tr><td></td><td></td><td>

Added footnote 'For S32K11x – FIRC/SOSC/FIRC/LPO; For S32K14x – FIRC/SOSC/FIRC/LPO/SPLL' to 'VLPS Mode: All clock sources disabled'
Updated numbers for:

VLPR → VLPS
VLPS → VLPR
'RUN → Compute operation'
RUN → VLPS
RUN → VLPR

In Power consumption :

Updated specs for S32K142, S32K144, and S32K148
Updated footnote 'Typical current numbers are indicative ...'
Updated footnote 'The S32K148 data ...'
Removed footnote 'Above S32K148 data is preliminary targets only'
Added new table 'Power consumption at 3.3 V'

In General AC specifications :

Updated max value and footnote of WFRST
Updated symbol for not filtered pulse to 'WNFRST', updated min value, removed max. value, and added footnote

Fixed naming conventions to align with DS in DC electrical specifications at 3.3 V Range and DC electrical specifications at 5.0 V Range
Updated specs for AC electrical specifications at 3.3 V range and AC electrical specifications at 5 V range
In Device clock specifications :

Updated f_{BUS} to 48 for 11x
Added footnote to f_{BUS} for 14x

In External System Oscillator frequency specifications :

Added specs for S32K11x
Updated 't_{dc_extal}' for S32K14x
Added footnote 'Frequecies below ... ' to 'f_{ec_extal}' and 't_{dc_extal}'

Splitted Flash timing specifications — commands for S32K14x and S32K11x
Updated Flash timing specifications — commands for S32K14x
In Reliability specifications :

Added footnote 'Data retention period ... ' for 'tnvmretp1k' and 'tnvmretee'
Minor update in footnote for 'nnvmwree16' 'nnvmwree256'

In QuadSPI AC specifications :

Updated 'MCR[SCLKCFG[5]]' value to 0
Updated 'Data Input Setup Time' HSRUN Internal DQS PAD Loopback value to 1.6
Updated 'Data Input Setup Time' DDR External DQS min. value to 2
Updated 'Data Input Hold Time' DDR External DQS min. value to 20
Upadted figure 'QuadSPI output timing (SDR mode) diagram' and 'QuadSPI input timing (HyperRAM mode) diagram'

In 12-bit ADC electrical characteristics :

Added note 'On reduced pin packages where ... '
Removed max. value of 'I_{DDA_ADC}'
Added note 'Due to triple ... '

In 12-bit ADC operating conditions, removed parameter 'ΔV_{DDA}'
In CMP with 8-bit DAC electrical specifications :

Updated Typ. and Max. values of 'I_{DDLS}'
Upadted Typ. value of 't_{DHSB}'
Updated Typ. value of 'V_{HYST1}' , 'V_{HYST2}', and 'V_{HYST3}'

In LPSPI electrical specifications :

Updated 'f_{periph}' and 'f_{op}', and 't_{SPSCK}'

</td></tr>
</table>

Table continues on the next page...