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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	128
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b SAR; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k148hft0vlqr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

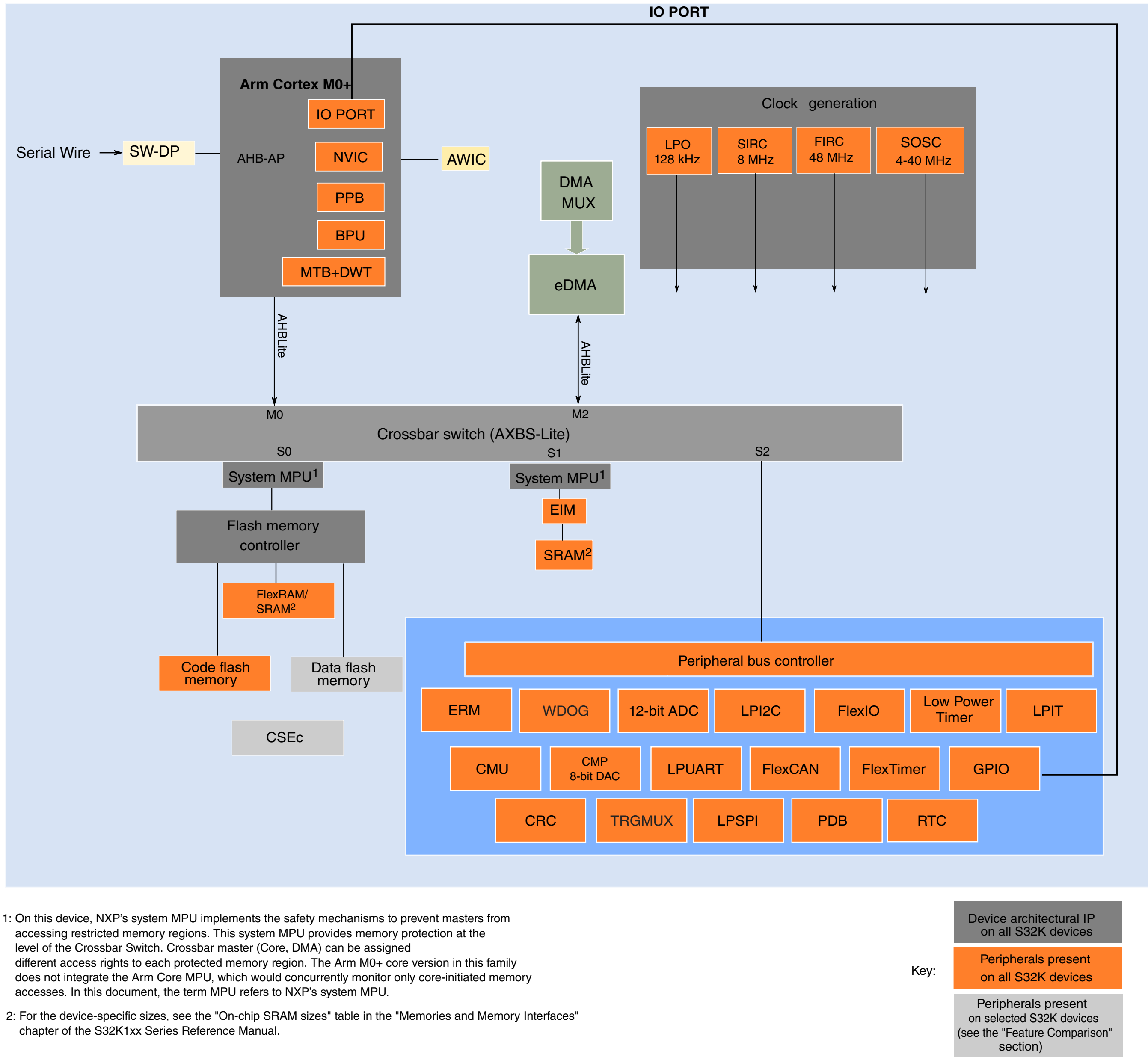


Figure 2. High-level architecture diagram for the S32K11x family

2 Feature comparison

The following figure summarizes the memory, peripherals and packaging options for the S32K1xx devices. All devices which share a common package are pin-to-pin compatible.

NOTE

Availability of peripherals depends on the pin availability in a particular package. For more information see *IO Signal*

4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate and the ramp rate assumes that the S32K1xx HW design guidelines in AN5426 are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. T_J (Junction temperature)=135 °C. Assumes T_A=125 °C for RUN mode

   T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

   - Assumes maximum θJA for 2s2p board. See Thermal characteristics
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

Device functionality is guaranteed up to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.7 V

Table 2. Voltage and current operating requirements [1]

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	4
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.

Table 5. V_{DD} supply LVR, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- RUN Mode:
  - Clock source: FIRC
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
  - FLASH_CLK = 24 MHz
- HSRUN Mode:
  - Clock source: SPLL
  - SYS_CLK/CORE_CLK = 112 MHz
  - BUS_CLK = 56 MHz
  - FLASH_CLK = 28 MHz
- VLPR Mode:
  - Clock source: SIRC
  - SYS_CLK/CORE_CLK = 4 MHz
  - BUS_CLK = 4 MHz
  - FLASH_CLK = 1 MHz
- STOP1/STOP2 Mode:
  - Clock source: FIRC
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
  - FLASH_CLK = 24 MHz
- VLPS Mode: All clock sources disabled [1]

Table 6. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	μs

Table continues on the next page...

1.
   - For S32K11x – FIRC/SOSC
   - For S32K14x – FIRC/SOSC/SPLL

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	µs
	STOP1 → RUN	0.07	0.075	0.08	µs
	STOP2 → RUN	0.07	0.075	0.08	µs
	VLPR → RUN	19	—	26	µs
	VLPR → VLPS	5.1	5.7	6.5	µs
	VLPS → VLPR	18.8	23	27.75	µs
	RUN → Compute operation	0.72	0.75	0.77	µs
	HSRUN → Compute operation	0.3	0.31	0.35	µs
	RUN → STOP1	0.35	0.38	0.4	µs
	RUN → STOP2	0.2	0.23	0.25	µs
	RUN → VLPS	0.3	0.35	0.4	µs
	RUN → VLPR	3.5	3.8	5	µs
	VLPS → Asynchronous DMA Wakeup	105	110	125	µs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	Pin reset → Code execution	—	214	—	µs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes _Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table Table 7. For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

Table 7. Power consumption (Typicals unless stated otherwise) [1] (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (μA) [2]		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [3]		
			Peripherals disabled [5]	Peripherals enabled	Peripherals disabled [6]	Peripherals enabled use case 1 [6]	Peripherals enabled use case 2 [7]			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	IDD/MHz (μA/MHz) [4]
		Max	1637	1694	3.1	3.21	NA	12.7	13.7	25	32.9	30.7	38.8	36	43.8	NA		450
S32K144	25	Typ	29.8	42	1.48	1.50	2.91	7	7.7	19.7	26.9	25.1	33.3	30.2	39.6	43.3	55.6	378
	85	Typ	150	159	1.72	1.85	3.08	7.2	8.1	20.4	27.1	26.1	33.5	30.5	40	43.9	56.1	381
		Max	359	384	2.60	2.65	NA	9.2	9.9	23.2	29.6	29.3	36.2	34.8	42.1	46.3	59.7	435
	105	Typ	256	273	1.80	2.10	3.23	7.8	8.5	20.6	27.4	26.6	33.8	31.2	40.5	44.8	57.1	390
		Max	850	900	2.65	2.70	NA	10.3	11.1	23.9	30.6	30.3	37.3	35.6	43.5	47.9	61.3	445
	125	Typ	NA	NA	NA	NA	3.65	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	1960	1998	3.18	3.25	NA	12.9	13.8	26.9	33.6	35	40.3	38.7	46.8	NA		484
S32K146	25	Typ	37	47	1.57	1.61	3.3	8	9.2	23.4	31.4	30.5	40.2	36.2	47.6	52	68.3	452
	85	Typ	207	209	1.79	1.83	3.54	8.9	10.1	24.4	32.4	31.5	41.3	37.2	48.7	53.3	69.8	465
		Max	974	981	3.32	3.38	NA	12.7	13.9	29.3	37.9	36.7	47	42.4	54.4	60.3	78	530
	105	Typ	419	422	1.99	2.04	3.78	9.8	11	25.3	33.4	32.5	42.2	38.1	49.6	54.4	70.8	477
		Max	2004	2017	4.06	4.13	NA	17.1	18.3	34.1	42.6	41.3	51.4	46.9	58.8	65.7	82.8	587
	125	Typ	NA	NA	NA	NA	4.44	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3358	3380	5.28	5.38	NA	22.6	23.7	40.2	48.8	47.3	57.4	52.8	64.8	NA		660
S32K148[8]	25	Typ	38	54	2.17	2.20	3.45	8.5	9.6	27.6	34.9	35.5	45.3	42.1	57.7	60.3	83.3	526
	85	Typ	336	357	2.30	2.35	3.74	10.1	11.1	29.1	37.0	36.8	46.6	43.4	59.9	62.9	88.7	543

Table continues on the next page...

Table 8. VLPS additional use-case power consumption at typical conditions

Use-case	Description	Temp.	Device						Unit
			S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
VLPS and RTC	• Clock source: LPO or RTC_CLKIN	25	TBD	TBD	30	30	30	40	µA
		85	TBD	TBD	110	170	180	240	µA
		105	TBD	TBD	230	330	350	490	µA
		125	TBD	TBD	570	680	810	1250	µA
VLPS and LPUART TX/RX	• Clock source: SIRC • Transmiting or receiving continuously using DMA • Baudrate: 19.2 kbps	25	TBD	TBD	230	230	250	250	µA
		85	TBD	TBD	320	400	410	490	µA
		105	TBD	TBD	490	550	600	850	µA
		125	TBD	TBD	890	1070	1250	1960	µA
VLPS and LPUART wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 19.2 kbps	25	TBD	TBD	100	100	110	110	µA
		85	TBD	TBD	170	240	280	350	µA
		105	TBD	TBD	260	400	480	600	µA
		125	TBD	TBD	530	580	1000	1280	µA
VLPS and LPI2C master	• Clock Source: SIRC • Transmit/receive using DMA • Baudrate: 100 kHz	25	TBD	TBD	670	690	820	900	µA
		85	TBD	TBD	880	960	1220	1370	µA
		105	TBD	TBD	1080	1250	1660	2060	µA
		125	TBD	TBD	1970	1980	2860	3690	µA
VLPS and LPI2C slave wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 100 kHz	25	TBD	TBD	250	250	270	280	µA
		85	TBD	TBD	340	340	410	510	µA
		105	TBD	TBD	430	430	610	810	µA
		125	TBD	TBD	740	760	1170	1540	µA
VLPS and LPSPI master	• Clock source: SIRC • Transmit/receive using DMA • Baudrate: 500 kHz	25	TBD	TBD	2.99	3.19	3.75	4.11	mA
		85	TBD	TBD	3.26	3.7	4.35	4.93	mA
		105	TBD	TBD	3.5	4.2	4.93	5.74	mA
		125	TBD	TBD	3.93	4.63	5.97	7.38	mA
VLPS and LPIT	• Clock source: SIRC • 1 channel enable • Mode: 32-bit periodic counter	25	TBD	TBD	100	100	120	130	µA
		85	TBD	TBD	190	250	260	320	µA
		105	TBD	TBD	310	410	440	570	µA
		125	TBD	TBD	640	750	910	1280	µA

The following table shows the power consumption targets for S32K148 in various mode of operations measure at 3.3 V.

Table 9. Power consumption at 3.3 V

Chip/Device	Ambient Temperature (°C)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA)[1]	
			Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI	Peripherals enabled + QSPI	Peripherals enabled + ENET + SAI
S32K148	25	Typ	67.3	79.1	89.8	105.5
	85	Typ	67.4	79.2	95.6	105.9
		Max	82.5	88.2	109.7	117.4
	105	Typ	68.0	79.8	96.6	106.7
		Max	80.3	89.1	109.0	119.0
	125	Max	83.5	94.7	NA	

1. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.

4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

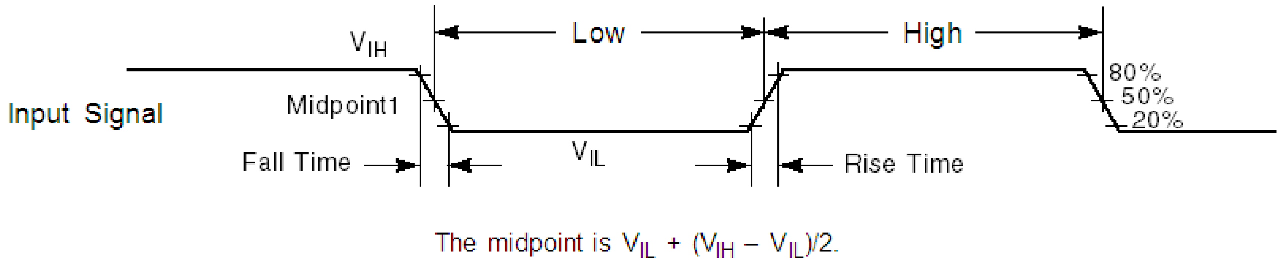


Figure 7. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	$\overline{\text{RESET}}$ input filtered pulse	—	10	ns	4
WNFRST	$\overline{\text{RESET}}$ input not filtered pulse	Maximum of (100 ns, bus clock period)	—	ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Maximum length of $\overline{\text{RESET}}$ pulse which will be filtered by internal filter.
5. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter. This number depends on bus clock period also. For example, in VLPR mode bus clock is 4 MHz, which make clock period of 250 ns. In this case, minimum pulse width which will cause reset is 250 ns. For faster bus clock frequencies which have clock period less than 100 ns, the minimum pulse width not filtered will be 100 ns.

6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
7. When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
8. Measured at input V = V_{SS}
9. Measured at input V = V_{DD}

5.4 DC electrical specifications at 5.0 V Range

Table 12. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh}= (V_{DD} - 0.8 V)	5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	5	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = V_{DD} - 0.8 V	20	—	—	mA	3
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	20	—	—	mA	3
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	14.0	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	14.5	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh} = V_{DD} - 0.8 V	21	—	—	mA	4
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol}= 0.8 V	20.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					5
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	6
R_{PD}	Internal pulldown resistors	20		50	kΩ	7

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
4. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

6.2.4 Low Power Oscillator (LPO) electrical specifications

Table 21. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	113	128	139	kHz
$T_{startup}$	Startup Time	—	—	20	μs

6.2.5 SPLL electrical specifications

Table 22. SPLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPLL_REF} [1]	PLL Reference Frequency Range	8	—	16	MHz
F_{SPLL_Input} [2]	PLL Input Frequency	8	—	40	MHz
F_{VCO_CLK}	VCO output frequency	180	—	320	MHz
F_{SPLL_CLK}	PLL output frequency	90	—	160	MHz
J_{CYC_SPLL}	PLL Period Jitter (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	120	—	ps
	at F_{VCO_CLK} 320 MHz	—	75	—	ps
J_{ACC_SPLL}	PLL accumulated jitter over 1μs (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	1350	—	ps
	at F_{VCO_CLK} 320 MHz	—	600	—	ps
D_{UNL}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%
T_{SPLL_LOCK}	Lock detector detection time[4]	—	—	$150 \times 10^{-6} + 1075(1/F_{SPLL\_REF})$	s

1. F_{SPLL_REF} is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLLCFG register of Reference Manual.
2. F_{SPLL_Input} is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

6.3 Memory and memory interfaces

6.3.1 Flash memory module (FTFC) electrical specifications

This section describes the electrical characteristics of the flash memory module.

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
	setting (32-bit write complete, ready for next 32-bit write)	Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550	200	550	200	550		
$t_{quickwrClnup}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms	7

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2× the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 μs, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

Table 24. Flash command timing specifications for S32K11x

Symbol	Description[1]		S32K116		S32K118			
			Typ	Max	Typ	Max	Unit	Notes
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	0.36	—	0.36	ms	
		64 KB flash	—	—	—	—		
		128 KB flash	—	1.2	—	—		
		256 KB flash	—	—	—	2		
		512 KB flash	—	—	—	—		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	μs	
		4 KB flash	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	100	—	100	μs	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	μs	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	15	300	15	300	ms	2
		64 KB flash	—	—	—	—		
		128 KB flash	120	1100	—	—		
		256 KB flash	—	—	250	2125		
		512 KB flash	—	—	—	—		

Table continues on the next page...

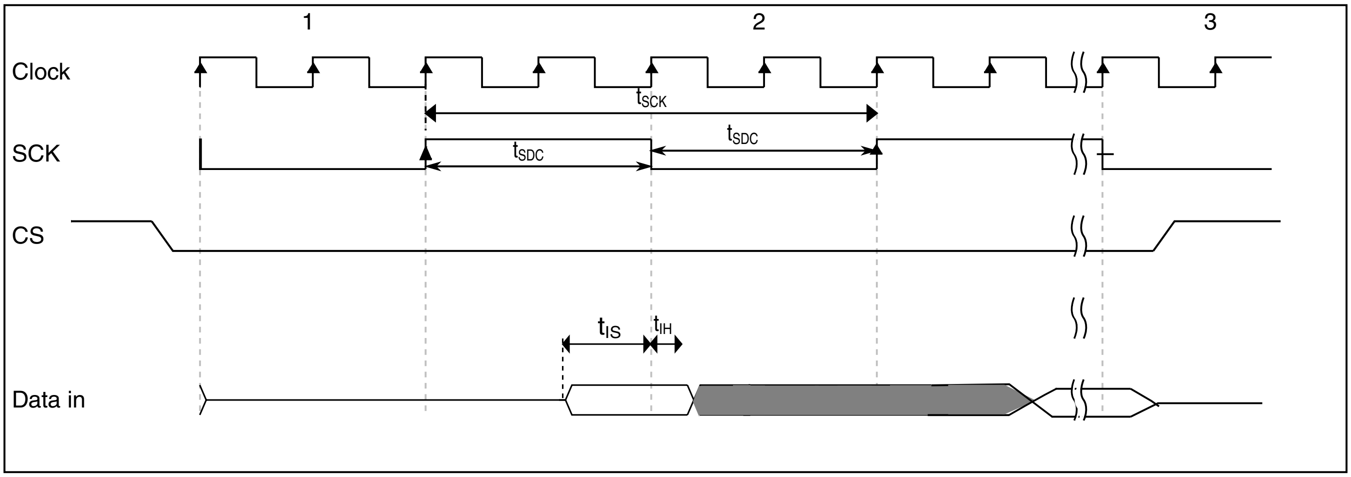


Figure 9. QuadSPI input timing (SDR mode) diagram

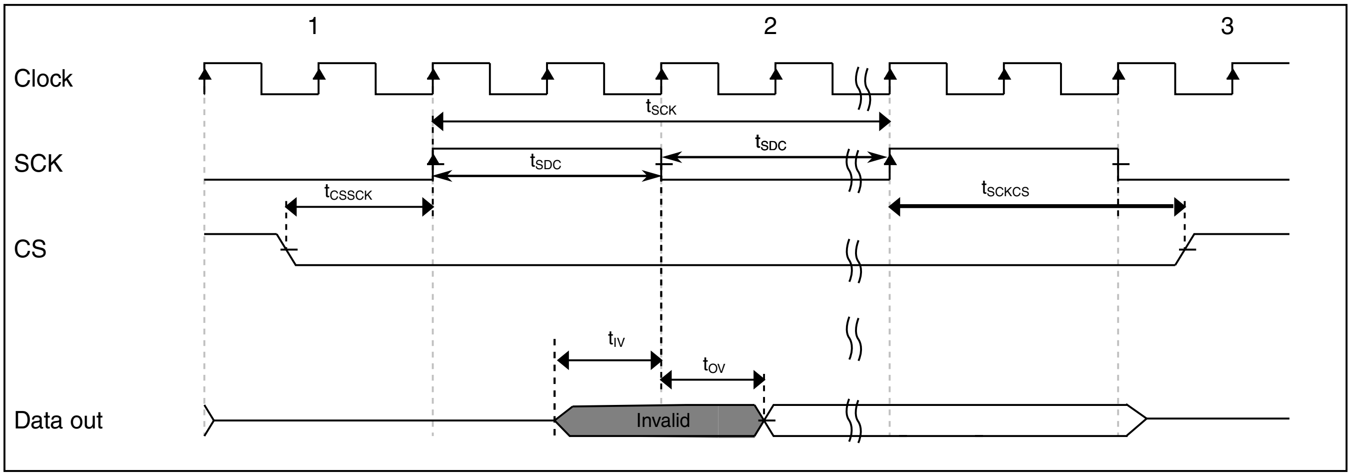
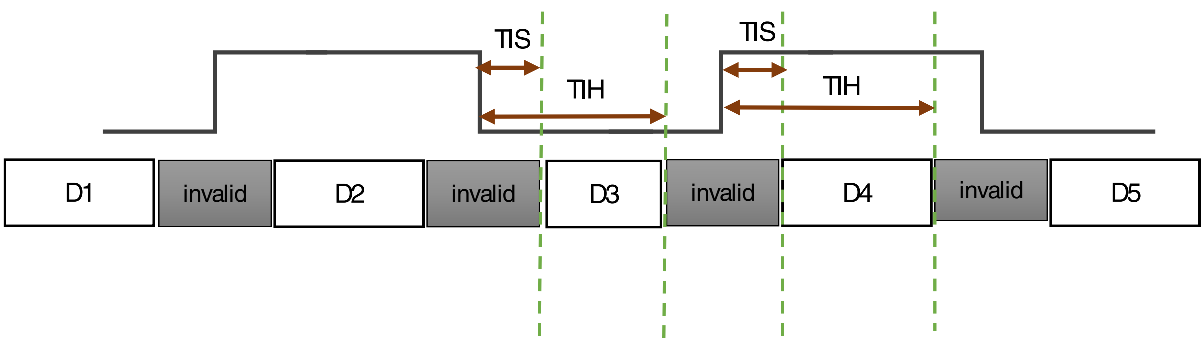


Figure 10. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time
TIH – Hold Time

Figure 11. QuadSPI input timing (HyperRAM mode) diagram

Table 27. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
f_{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	MHz	3, 4
f_{CONV}	ADC conversion frequency	No ADC hardware averaging.[5] Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	6, 7
		ADC hardware averaging set to 32. [5] Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	6, 7

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual* .
4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. Numbers based on the minimum sampling time of 275 ns.
7. For guidelines and examples of conversion rate calculation, see the *Reference Manual* section 'Calibration function'

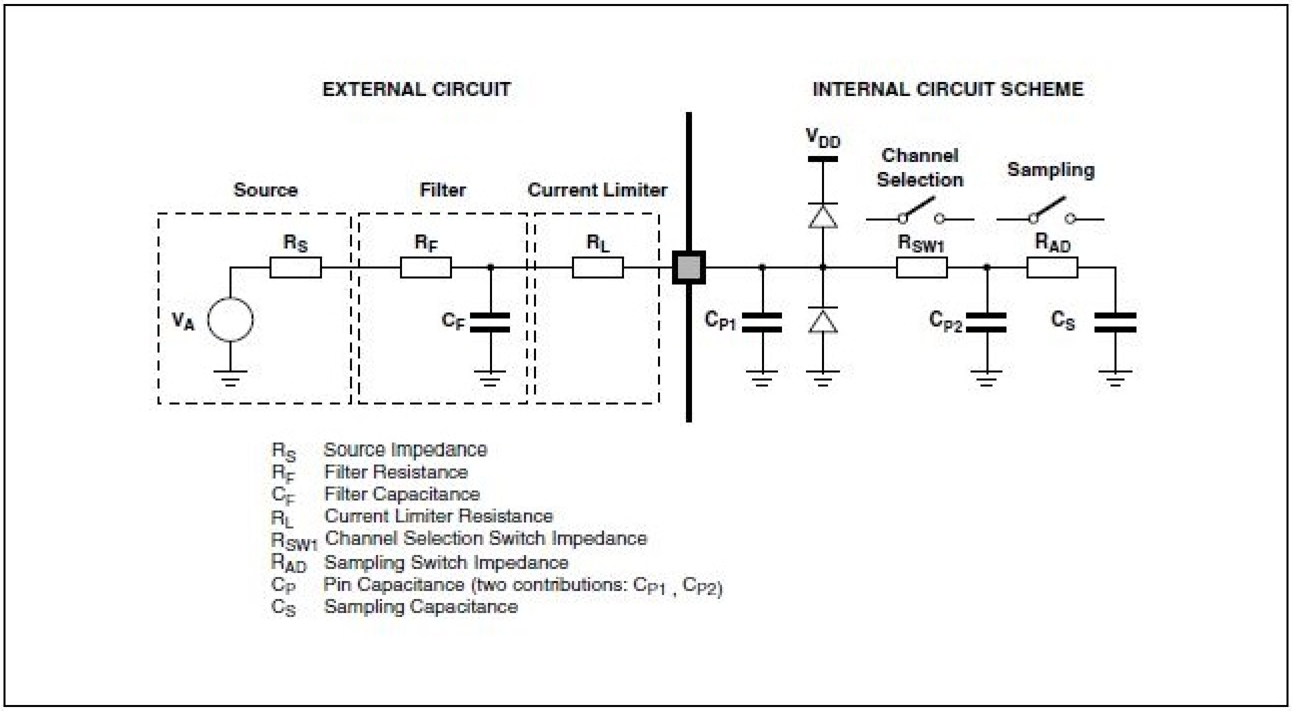


Figure 13. ADC input impedance equivalency diagram

Table 32. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
4	t_{Lag}[9]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	$(SCKPCS+1)*t_{periph} - 25$	-	$(SCKPCS+1)*t_{periph} - 25$	-	$(SCKPCS+1)*t_{periph} - 25$	-	$(SCKPCS+1)*t_{periph} - 25$	-	$(SCKPCS+1)*t_{periph} - 50$	-	$(SCKPCS+1)*t_{periph} - 50$	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													
5	t_{WSPSCK}[10]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	$t_{SPSCK}/2-3$	$t_{SPSCK}/2+3$	$t_{SPSCK}/2-3$	$t_{SPSCK}/2+3$	$t_{SPSCK}/2-3$	$t_{SPSCK}/2+3$	$t_{SPSCK}/2-3$	$t_{SPSCK}/2+3$	$t_{SPSCK}/2-5$	$t_{SPSCK}/2+5$	$t_{SPSCK}/2-5$	$t_{SPSCK}/2+5$	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow)[6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37[11] 32 [12]	-	72	-	78	-	
			Master Loopback[5]	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow)[6]	8	-	10	-	7	-	9	-	20	-	20	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow)[6]	3	-	3	-	3	-	3	-	12	-	12	-	

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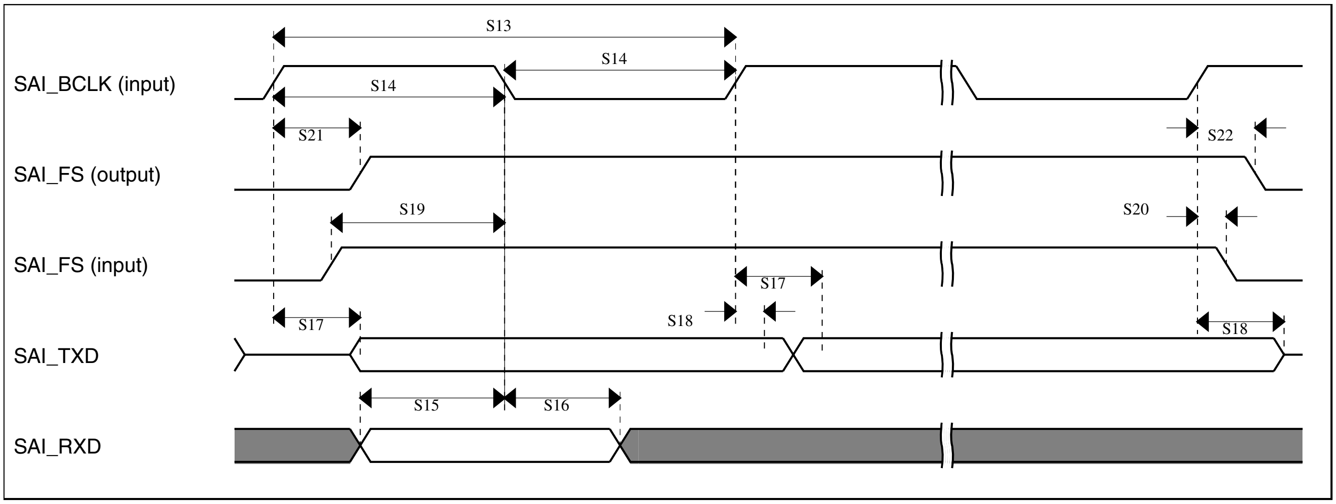

Figure 23. SAI Timing — Slave modes

6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 35. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

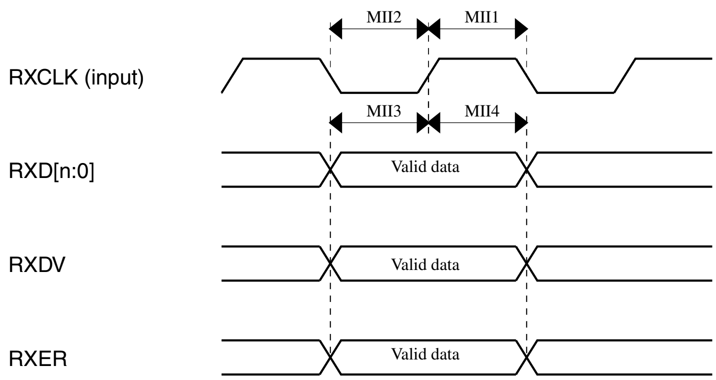

Figure 24. MII receive diagram

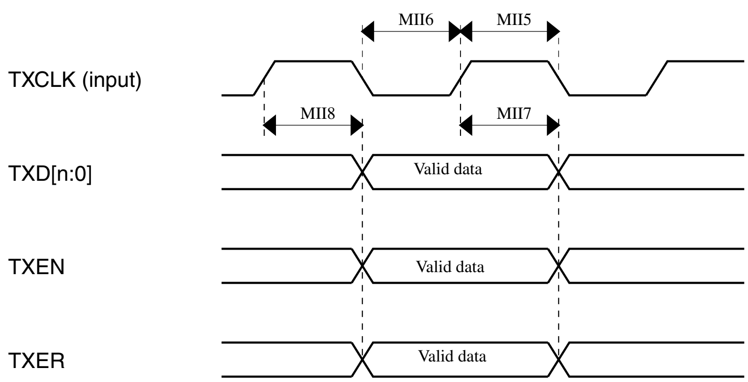

Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 37. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

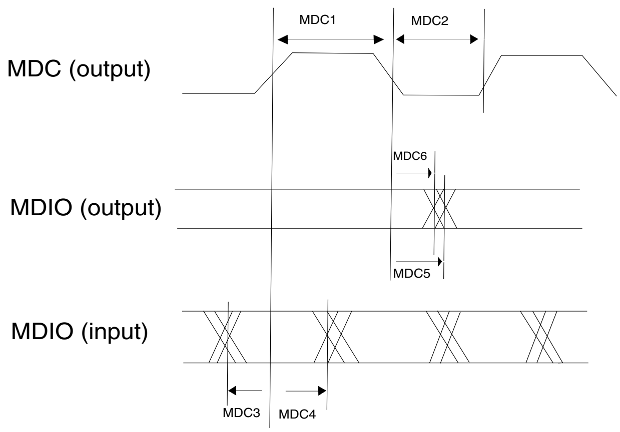

Figure 28. MII/RMII serial management channel timing diagram

6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specofications

Table 38. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

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