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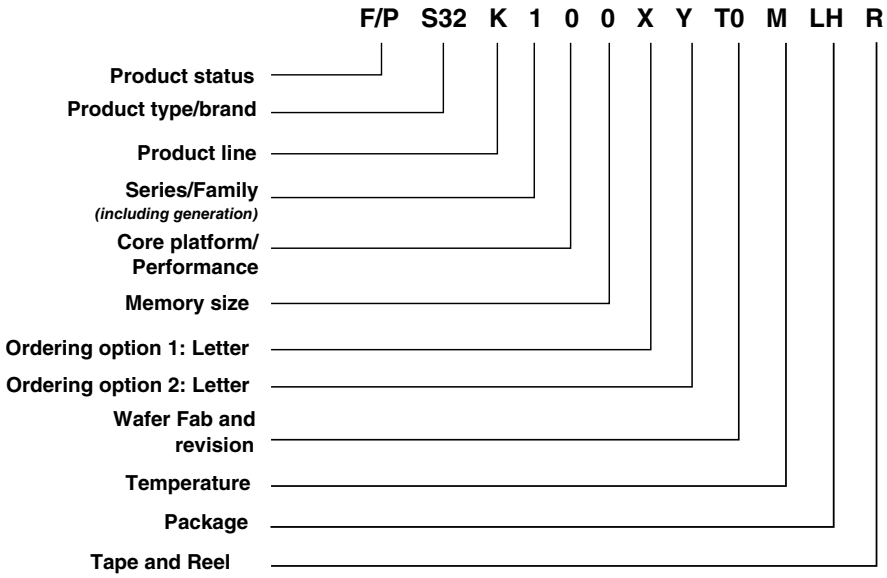
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	128
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b SAR; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k148hft0vlqt

3.2 Ordering information



Product status
P: Prototype
F: Qualified

Product type/brand
S32: Automotive 32-bit MCU

Product line
K: Arm Cortex MCUs

Series/Family
1: 1st product series
2: 2nd product series

Core platform/Performance
1: Arm Cortex M0+
4: Arm Cortex M4F

Memory size

	2	4	6	8
S32K11x			128K	256K
S32K14x	256K	512K	1M	2M

Ordering option
X: Speed
B: 48 MHz without DMA (S32K11x only)
L: 48 MHz with DMA (S32K11x only)
H: 80 MHz
U[1]: 112 MHz (Not valid with M temperature/125C)

Y: Optional feature
R: Base feature set
F: CAN FD, FlexIO
A[1]: CAN FD, FlexIO, Security
E: Ethernet, Serial Audio Interface (S32K148 only)
J[1]: Ethernet, Serial Audio Interface, CAN FD, FlexIO, Security (S32K148 only)

Wafer, Fab and revision
Fx: ATMC[2]
Tx: GF
XX: Flex #[2]

x0: 1st revision

Temperature
V: -40C to 105C
M: -40C to 125C
W: -40C to 150C[2]

Package

Pins	LQFP	QFN	BGA
32	-	FM	-
48	LF	-	-
64	LH	-	-
100	LL	-	MH
144	LQ	-	-
176	LU	-	-

Tape and Reel
T: Trays/Tubes
R: Tape and Reel

1. CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
2. Not supported yet
3. Part numbers no longer offered as standard include:
   Ordering Option X (M:64MHz); Ordering Option Y (N: limited RAM. 16KB for K142, 48KB for K144, 96KB for K146, 192KB for K148 S: Security); Temperature (C: -40C to 85C)

NOTE
Not all part number combinations are available. See S32K1xx_Orderable_Part_Number_List.xlsx attached with the Datasheet for list of standard orderable parts.

Figure 4. Ordering information

4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate and the ramp rate assumes that the S32K1xx HW design guidelines in AN5426 are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. T_J (Junction temperature)=135 °C. Assumes T_A=125 °C for RUN mode

   T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

   - Assumes maximum θJA for 2s2p board. See Thermal characteristics
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

Device functionality is guaranteed up to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.7 V

Table 2. Voltage and current operating requirements 1

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	4
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.

Table 7. Power consumption (Typicals unless stated otherwise) 1 (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (µA) [2]		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [3]		IDD/MHz (µA/MHz) [4]
			Peripherals disabled [5]	Peripherals enabled	Peripherals disabled [6]	Peripherals enabled use case 1[6]	Peripherals enabled use case 2[7]			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
		Max	1660	1736	3.48	3.55	NA	14.5	15.6	34.8	43.6	41.9	53.9	48.7	65.1	70.4	96.1	609
	105	Typ	560	577	2.49	2.54	4.03	10.9	11.9	29.8	37.8	37.6	47.5	45.2	61.5	63.8	89.1	565
		Max	2945	2970	4.40	4.47	NA	18.0	19.0	38.4	46.8	44.9	55.3	51.6	66.8	73.6	97.4	645
	125	Typ	NA	NA	NA	NA	4.85	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3990	4166	6.00	6.08	NA	23.4	24.5	44.3	52.5	50.9	61.3	57.5	71.6	NA		719

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and On-chip pulldown is enabled for all unused input pins.
2. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
3. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
4. Values mentioned for S32K14x devices are measured at RUN@80 MHz with peripherals disabled and values mentioned for S32K11x devices are measured at RUN@48 MHz with peripherals disabled.
5. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
6. Data collected using RAM
7. Numbers on limited samples size and data collected with Flash
8. The S32K148 data points assume that ENET/QuadSPI/SAI etc. are inactive.

Table 8. VLPS additional use-case power consumption at typical conditions

Use-case	Description	Temp.	Device						Unit
			S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
VLPS and RTC	• Clock source: LPO or RTC_CLKIN	25	TBD	TBD	30	30	30	40	µA
		85	TBD	TBD	110	170	180	240	µA
		105	TBD	TBD	230	330	350	490	µA
		125	TBD	TBD	570	680	810	1250	µA
VLPS and LPUART TX/RX	• Clock source: SIRC • Transmiting or receiving continuously using DMA • Baudrate: 19.2 kbps	25	TBD	TBD	230	230	250	250	µA
		85	TBD	TBD	320	400	410	490	µA
		105	TBD	TBD	490	550	600	850	µA
		125	TBD	TBD	890	1070	1250	1960	µA
VLPS and LPUART wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 19.2 kbps	25	TBD	TBD	100	100	110	110	µA
		85	TBD	TBD	170	240	280	350	µA
		105	TBD	TBD	260	400	480	600	µA
		125	TBD	TBD	530	580	1000	1280	µA
VLPS and LPI2C master	• Clock Source: SIRC • Transmit/receive using DMA • Baudrate: 100 kHz	25	TBD	TBD	670	690	820	900	µA
		85	TBD	TBD	880	960	1220	1370	µA
		105	TBD	TBD	1080	1250	1660	2060	µA
		125	TBD	TBD	1970	1980	2860	3690	µA
VLPS and LPI2C slave wake-up	• Clock source: SIRC • Wake-up address feature enabled • Baudrate: 100 kHz	25	TBD	TBD	250	250	270	280	µA
		85	TBD	TBD	340	340	410	510	µA
		105	TBD	TBD	430	430	610	810	µA
		125	TBD	TBD	740	760	1170	1540	µA
VLPS and LPSPI master	• Clock source: SIRC • Transmit/receive using DMA • Baudrate: 500 kHz	25	TBD	TBD	2.99	3.19	3.75	4.11	mA
		85	TBD	TBD	3.26	3.7	4.35	4.93	mA
		105	TBD	TBD	3.5	4.2	4.93	5.74	mA
		125	TBD	TBD	3.93	4.63	5.97	7.38	mA
VLPS and LPIT	• Clock source: SIRC • 1 channel enable • Mode: 32-bit periodic counter	25	TBD	TBD	100	100	120	130	µA
		85	TBD	TBD	190	250	260	320	µA
		105	TBD	TBD	310	410	440	570	µA
		125	TBD	TBD	640	750	910	1280	µA

5.3 DC electrical specifications at 3.3 V Range

NOTE

For details on the pad types defined in Table 11 and Table 12, see Reference Manual section *IO Signal Table* and IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Table 11. DC electrical specifications at 3.3 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	1
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	2
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.3 × V_{DD}	V	3
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{GPIO\text{-}HD\_DSE\_0}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	3.5	—	—	mA	
Iol_{GPIO} $Iol_{GPIO\text{-}HD\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	3	—	—	mA	
$Ioh_{GPIO\text{-}HD\_DSE\_1}$	I/O current source capability measured when pad V_{oh} = (V_{DD} – 0.8 V)	14	—	—	mA	4
$Iol_{GPIO\text{-}HD\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	12	—	—	mA	4
$Ioh_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	9.5	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_0}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	10	—	—	mA	5
$Ioh_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{oh}=V_{DD}-0.8 V	16	—	—	mA	5
$Iol_{GPIO\text{-}FAST\_DSE\_1}$	I/O current sink capability measured when pad V_{ol} = 0.8 V	15.5	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins [7]		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		60	kΩ	8
R_{PD}	Internal pulldown resistors	20		60	kΩ	9

1. S32K148 will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged S32K148 is guaranteed to operate from 2.97 V. All other S32K family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable
3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. For refernce only. Run simulations with the IBIS model and custom board for accurate results.

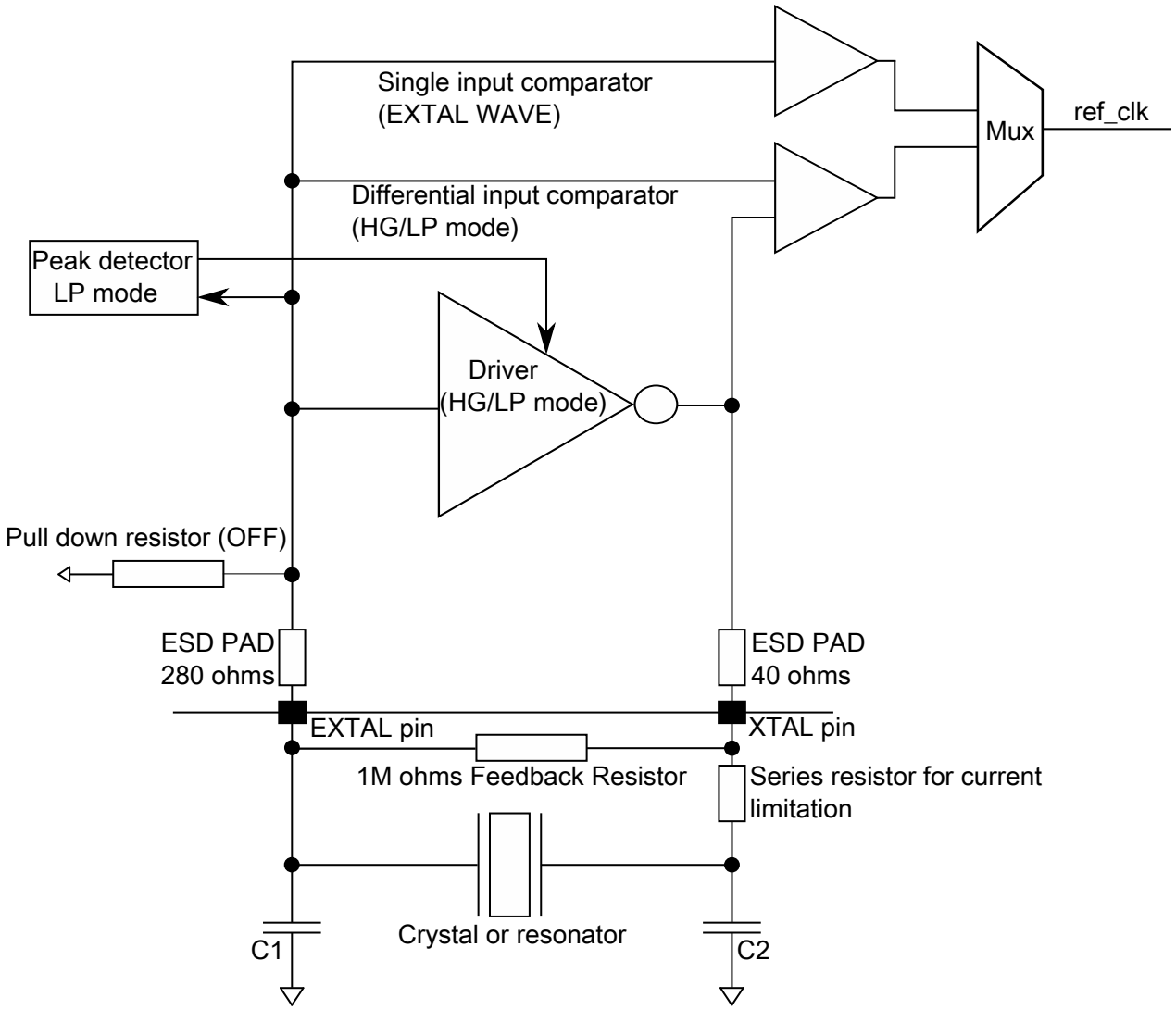


Figure 8. Oscillator connections scheme

Table 17. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	SCG_SOSCCFG[RANGE]=2'b10 for 4-8 MHz	2.2	—	13.7	mA/V	
	SCG_SOSCCFG[RANGE]=2'b11 for 8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	1.15	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

Table 17. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	µs	
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	µs	3,4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description[1]		S32K116		S32K118			
			Typ	Max	Typ	Max	Unit	Notes
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1 KB flash)	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	1.7	—	2.8	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	150	1500	230	2500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	150	1500	230	2500	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	71	—	71	—	ms	3
		64 KB EEPROM backup	—	—	—	—		
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2		
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	µs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	µs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	µs	

Table continues on the next page...

Table 25. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using FlexMemory feature : FlexRAM as Emulated EEPROM						
$t_{nvmretee}$	Data retention	5	—	—	years	4
$n_{nvmwree16}$	Write endurance • EEPROM backup to FlexRAM ratio = 16	100 K	—	—	writes	5, 6, 7
$n_{nvmwree256}$	• EEPROM backup to FlexRAM ratio = 256	1.6 M	—	—	writes	

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
3. Cycling endurance is per DFlash or PFlash Sector.
4. Data retention period per block begins upon initial user factory programming or after each subsequent erase. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.
5. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across product temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
6. For usage of any EEE driver other than the FlexMemory feature, the endurance spec will fall back to the specified endurance value of the D-Flash specification (1K).
7. FlexMemory calculator tool is available at NXP web site for help in estimation of the maximum write endurance achievable at specific EEPROM/FlexRAM ratios. The “In Spec” portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- QuadSPI trace length should be 3 inches.
- For non-Quad mode of operation if external device doesn’t have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

Table 37. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

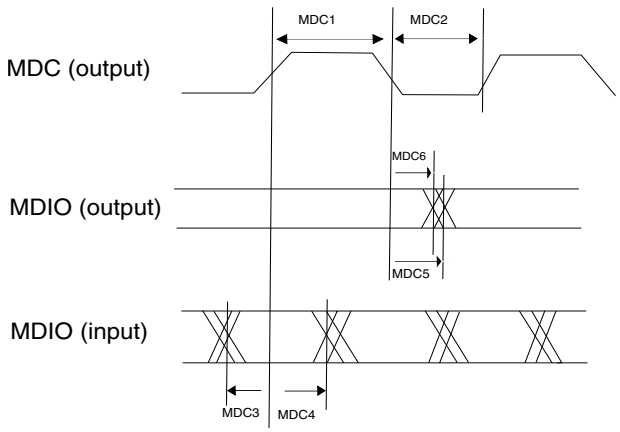


Figure 28. MII/RMII serial management channel timing diagram

6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specofications

Table 38. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

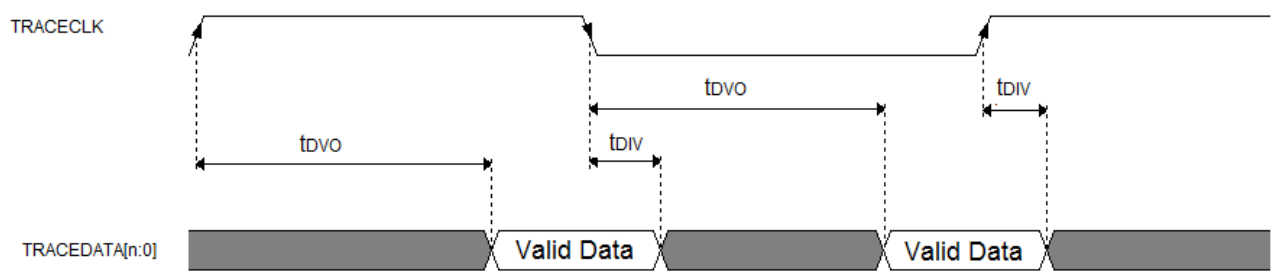


Figure 31. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

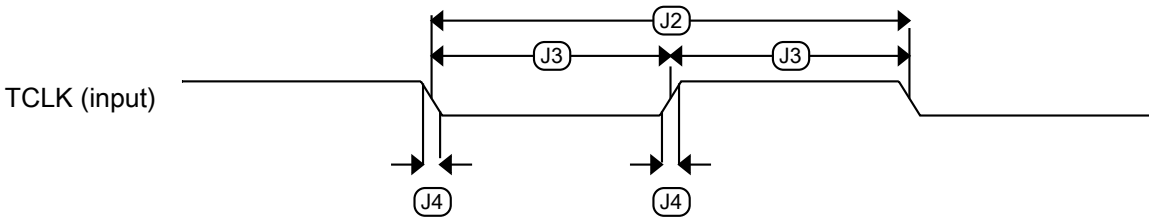


Figure 32. Test clock input timing

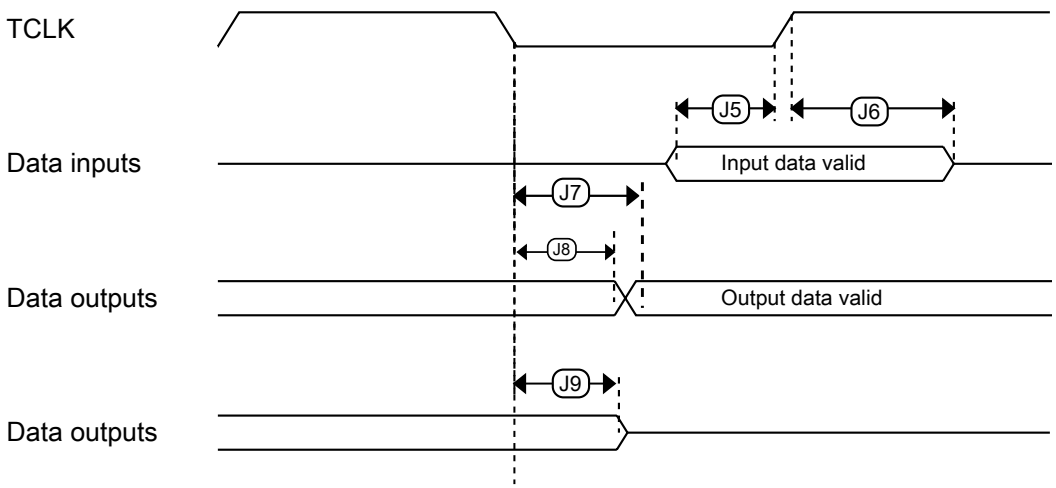


Figure 33. Boundary scan (JTAG) timing

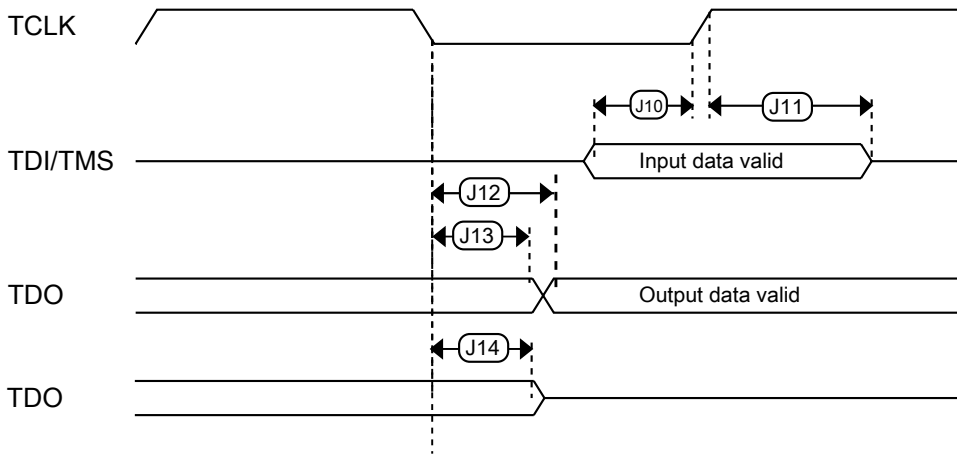


Figure 34. Test Access Port timing

7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

Table 42. Thermal characteristics for the 100 MAPBGA package

Rating	Conditions	Symbol	Values			Unit
			S32K146	S32K144	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) [1, 2]	Single layer board (1s)	$R_{\theta JA}$	57.2	61.0	52.5	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) [1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	32.1	35.6	27.5	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) [1, 2, 3]	Single layer board (1s)	$R_{\theta JMA}$	44.1	46.6	39.0	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Two layer board (2s2p)	$R_{\theta JMA}$	27.2	30.9	22.8	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	15.3	18.9	11.2	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	10.2	14.2	7.5	°C/W
Thermal resistance, Junction to Package Top outside center[6]	—	Ψ_{JT}	0.2	0.4	0.2	°C/W
Thermal resistance, Junction to Package Bottom outside center[7]	—	Ψ_{JB}	12.2	15.9	18.3	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release

2	03 March 2017	• Updated descpition of QSPI and Clock interfaces in Key Features section
		• Updated figure: High-level architecture diagram for the S32K1xx family
		• Updated figure: S32K1xx product series comparison
		• Added note in section Selecting orderable part number
		• Updated figure: Ordering information
		• In table: Absolute maximum ratings :
		  • Added footnote to I_{INJPAD_DC}
		  • Updated min and max value of I_{INJPAD_DC}
		  • Updated description, max and min values for I_{INJSUM}
		  • Updated $V_{IN\_TRANSIENT}$
		• In table: Voltage and current operating requirements :
		  • Renamed V_{SUP_OFF}
		  • Updated max value of V_{DD_OFF}
		  • Removed V_{INA} and V_{IN}
		  • Added V_{REFH} and V_{REFL}
		  • Updated footnote "Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V ...
		  • Removed I_{NJSUM_AF}
		• Updated footnotes in table Table 4
		• Updated section Power mode transition operating behaviors
		• In table: Power consumption
		  • Added footnote "With PMC_REGSC[CLKBIASDIS] ... "
		  • Updated conditions for VLPR
		  • Removed Idd/MHz for S32K144
		  • Updated numbers for S32K142 and S32K148
		  • Removed use case footnotes
		• In section Modes configuration :
		  • Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes _Master_configuration_sheet'
		• In table: DC electrical specifications at 3.3 V Range :
		  • Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		  • Added footnote to High drive port pins
		• In table: DC electrical specifications at 5.0 V Range :

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes

		• Added footnotes V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage
		• Updated table: AC electrical specifications at 3.3 V range
		• Updated table: AC electrical specifications at 5 V range
		• In table: Standard input pin capacitance
		  • Added footnote to Normal run mode (S32K14x series)
		• Removed note from 1M ohms Feedback Resistor in figure Oscillator connections scheme
		• In table: External System Oscillator electrical specifications
		  • Updated typical of I_{DDOSC} Supply current — low-gain mode (low-power mode) (HGO=0) 1 for 4 and 8 MHz
		  • Removed rows for I_{lk_ext} EXTAL/XTAL impedence High-frequency, low-gain mode (low-power mode) and high-frequency, high-gain mode and V_{EXTAL}
		  • Updated Typ. of R_S low-gain mode
		  • Updated description of R_F, R_S, and V_{PP}
		  • Removed footnote from R_F Feedback resistor
		  • Updated footnote for C_1 C_2 and R_F
		• In table: Table 18
		  • Removed mention of high-frequency
		  • Added HGO 0, 1 information
		• In table: Fast internal RC Oscillator electrical specifications
		  • Updated F_{FIRC}
		  • Updated description of ΔF
		  • Updated typ and max values of T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Added footnotes to T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles
		  • Updated naming convention of I_{DDFIRC} Supply current
		  • Added footnote to I_{DDFIRC} Supply current
		  • Added footnote to column Parameter
		• In table: Slow internal RC oscillator (SIRC) electrical specifications
		  • Removed V_{DD} Supply current in 2 MHz Mode
		  • Removed footnote and updated description of ΔF
		  • Updated footnote to F_{SIRC} and I_{DDSIRC}
		• In table: SPLL electrical specifications
		  • Added row for F_{SPLL_REF} PLL Reference
		  • Updated naming convention throughout the table
		  • Updated the max value of T_{SPLL_LOCK} Lock detector detection time
		• In table: Flash timing specifications — commands
		  • Added footnotes:
		  • All command times assumes ...
		  • For all EEPROM Emulation terms ...
		  • 'First time' EERAM writes after a POR ...
		  • Removed footnote 'Assumes 25 MHz or ...'
		  • Updated Max of $t_{eewr32bers}$
		  • Added parameters $t_{quickwr}$ and $t_{quickwrClnup}$
		• In table: Reliability specifications
		  • Removed Typ. values for all parameters
		  • Removed footnote 'Typical values represent ... '
		  • Added footnote 'Any other EEE driver usage ... '
		• Updated QuadSPI AC specifications
		• Removed topic: Reliability, Safety and Security modules
		• In table: 12-bit ADC operating conditions
		  • Updated V_{DDA}

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes
		• Updated specs for T_{JIT} Cycle-to-Cycle jitter to 300 ps • In QuadSPI AC specifications : • Updated specs for T_{iv} Data Output In-Valid Time • In figure 'QuadSPI output timing (SDR mode) diagram', marked Invalid area • In CMP with 8-bit DAC electrical specifications : • Removed '(VAIO)' from decription of V_{HYST0} • In LPSPI electrical specifications : • Added note 'Undefined' in figures 'LPSPI slave mode timing (CPHA = 0)' and 'LPSPI slave mode timing (CPHA = 1)'