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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	156
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b SAR; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k148hnt0vlur

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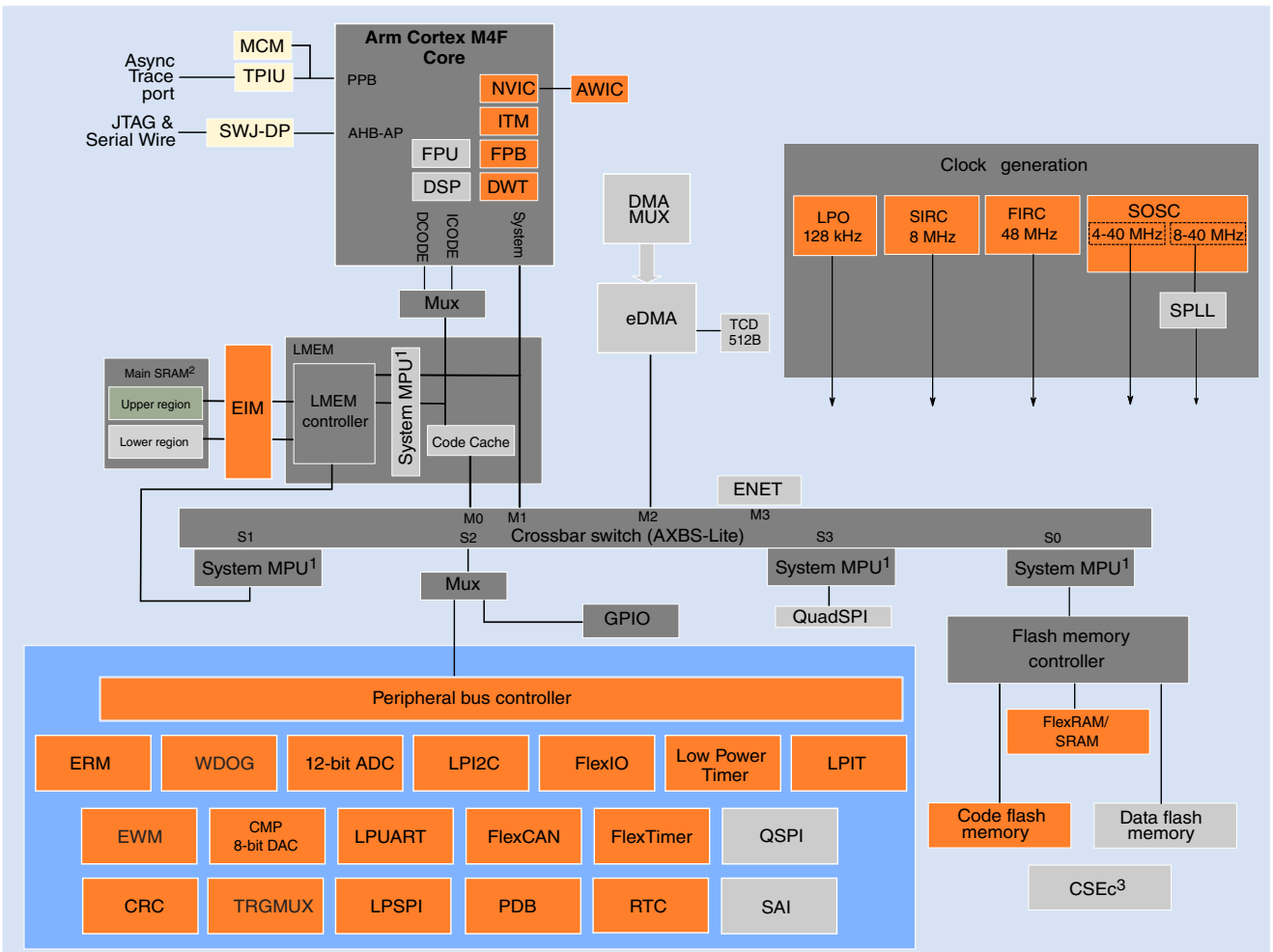
1 Block diagram

Following figures show superset high level architecture block diagrams of S32K14x series and S32K11x series respectively. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Each Crossbar master (Core, DMA, Ethernet) can be assigned different access rights to each protected memory region. The Arm M4 core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

3: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.

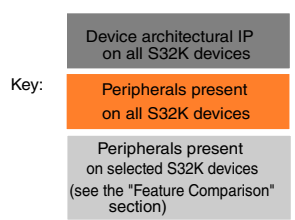
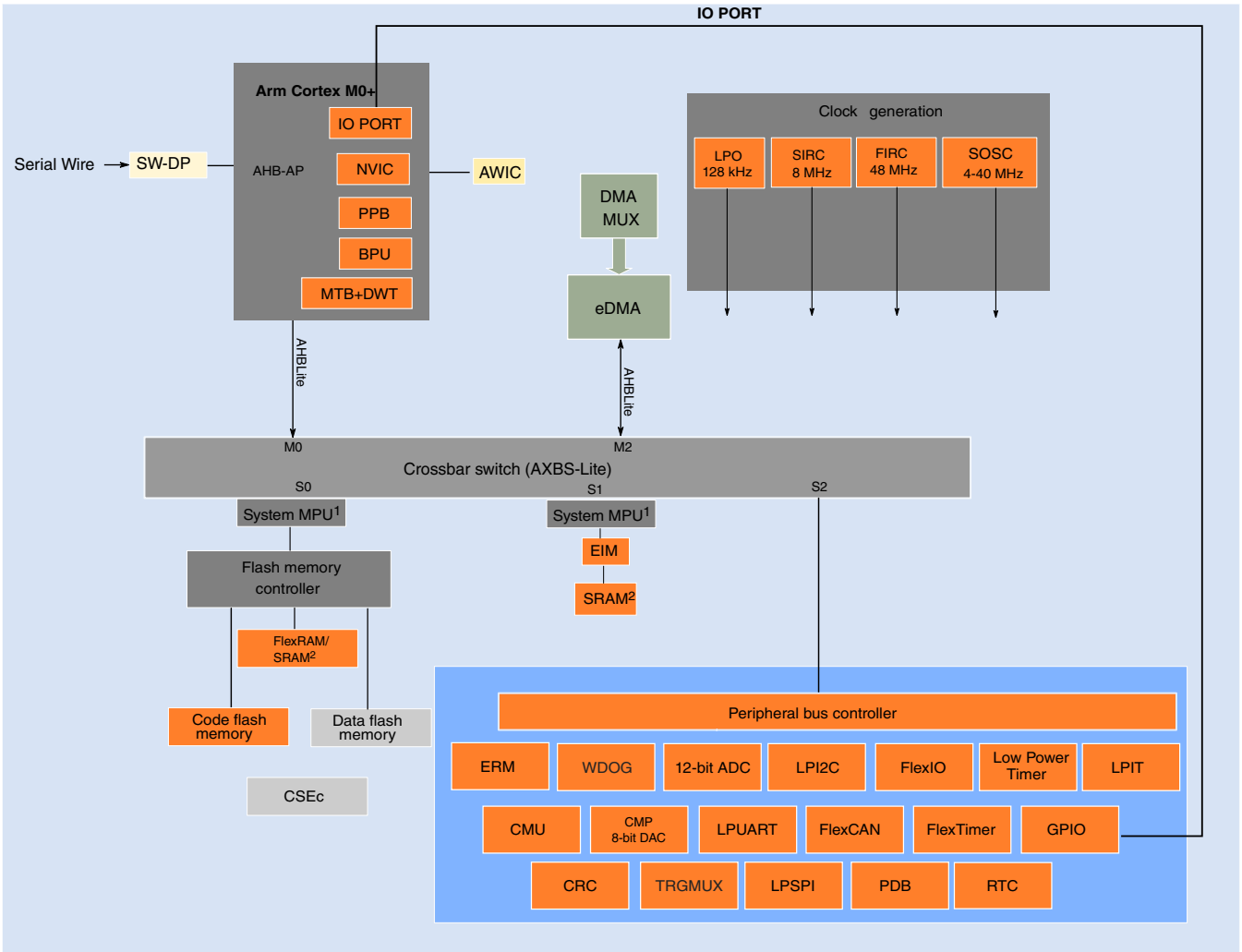


Figure 1. High-level architecture diagram for the S32K14x family



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Crossbar master (Core, DMA) can be assigned different access rights to each protected memory region. The Arm M0+ core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the S32K1xx Series Reference Manual.

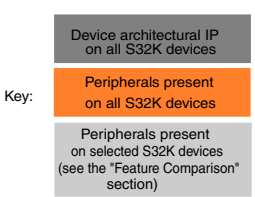


Figure 2. High-level architecture diagram for the S32K11x family

2 Feature comparison

The following figure summarizes the memory, peripherals and packaging options for the S32K1xx devices. All devices which share a common package are pin-to-pin compatible.

NOTE

Availability of peripherals depends on the pin availability in a particular package. For more information see *IO Signal*

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	µs
	STOP1 → RUN	0.07	0.075	0.08	µs
	STOP2 → RUN	0.07	0.075	0.08	µs
	VLPR → RUN	19	—	26	µs
	VLPR → VLPS	5.1	5.7	6.5	µs
	VLPS → VLPR	18.8	23	27.75	µs
	RUN → Compute operation	0.72	0.75	0.77	µs
	HSRUN → Compute operation	0.3	0.31	0.35	µs
	RUN → STOP1	0.35	0.38	0.4	µs
	RUN → STOP2	0.2	0.23	0.25	µs
	RUN → VLPS	0.3	0.35	0.4	µs
	RUN → VLPR	3.5	3.8	5	µs
	VLPS → Asynchronous DMA Wakeup	105	110	125	µs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	Pin reset → Code execution	—	214	—	µs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations. Attached *S32K1xx_Power_Modes _Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table Table 7. For full functionality refer to table: Module operation in available power modes of the *Reference Manual*.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input V = V_{SS}
7. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
tRF_{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
$tRF_{GPIO-HD}$	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
$tRF_{GPIO-FAST}$	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
tRF_{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
$tRF_{GPIO-HD}$	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

Table 14. AC electrical specifications at 5 V Range (continued)

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
		17.3	54.8	17.6	59.7	200
	1	1.1	4.6	1.1	5.0	25
		2.0	5.7	2.0	5.8	50
		5.4	16.0	5.0	16.0	200
$tRF_{GPIO-FAST}$	0	0.42	2.2	0.37	2.2	25
		2.0	5.0	1.9	5.2	50
		9.3	18.8	8.5	19.3	200
	1	0.37	0.9	0.35	0.9	25
		1.2	2.7	1.2	2.9	50
		6.0	11.8	6.0	12.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 15. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 16. Device clock specifications [1]

Symbol	Description	Min.	Max.	Unit
High Speed run mode[2]				
f_{SYS}	System and core clock	—	112	MHz
f_{BUS}	Bus clock	—	56	MHz
f_{FLASH}	Flash clock	—	28	MHz
Normal run mode (S32K11x series)				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	48	MHz

Table continues on the next page...

6.2.3 System Clock Generation (SCG) specifications

6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 19. Fast internal RC Oscillator electrical specifications

Symbol	Parameter[1]	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	$\%F_{FIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		3.4	5	µs[2]
T_{JIT}, [3]	Cycle-to-Cycle jitter	—	300	500	ps
T_{JIT}[3]	Long term jitter over 1000 cycles	—	0.04	0.1	$\%F_{FIRC}$

1. With FIRC regulator enable
2. Startup time is defined as the time between clock enablement and clock availability for system use.
3. FIRC as system clock

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 20. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	—	±3	$\%F_{SIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	—	±3.3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	9	12.5	µs[1]

1. Startup time is defined as the time between clock enablement and clock availability for system use.

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	µs	
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	µs	3,4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description[1]		S32K116		S32K118			
			Typ	Max	Typ	Max	Unit	Notes
t_{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	ms	2
$t_{pgmsec1k}$	Program Section execution time (1 KB flash)	—	5	—	5	—	ms	
t_{rd1all}	Read 1s All Block execution time	—	—	1.7	—	2.8	ms	
t_{rdonce}	Read Once execution time	—	—	30	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	150	1500	230	2500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	150	1500	230	2500	ms	2
$t_{pgmpart}$	Program Partition for EEPROM execution time	32 KB EEPROM backup	71	—	71	—	ms	3
		64 KB EEPROM backup	—	—	—	—		
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2		
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	µs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	µs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	µs	

Table continues on the next page...

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description[1]		S32K116		S32K118			
			Typ	Max	Typ	Max	Unit	Notes
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	µs	3,4
		48 KB EEPROM backup	—	—	—	—		
		64 KB EEPROM backup	—	—	—	—		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)	1st 32-bit write	200	550	200	550	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550		
		Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550		
$t_{quickwrClnup}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms	7

1. All command times assume 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 µs, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

6.3.1.2 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	—	—	years	1
$n_{nvmcycp}$	Cycling endurance	1 K	—	—	cycles	2, 3

Table continues on the next page...

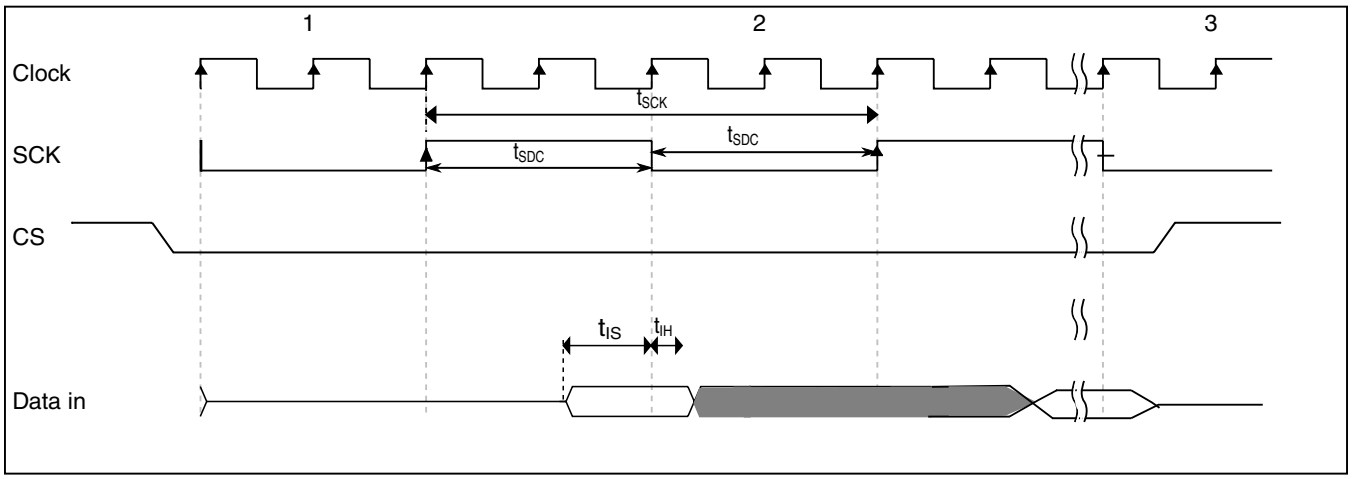


Figure 9. QuadSPI input timing (SDR mode) diagram

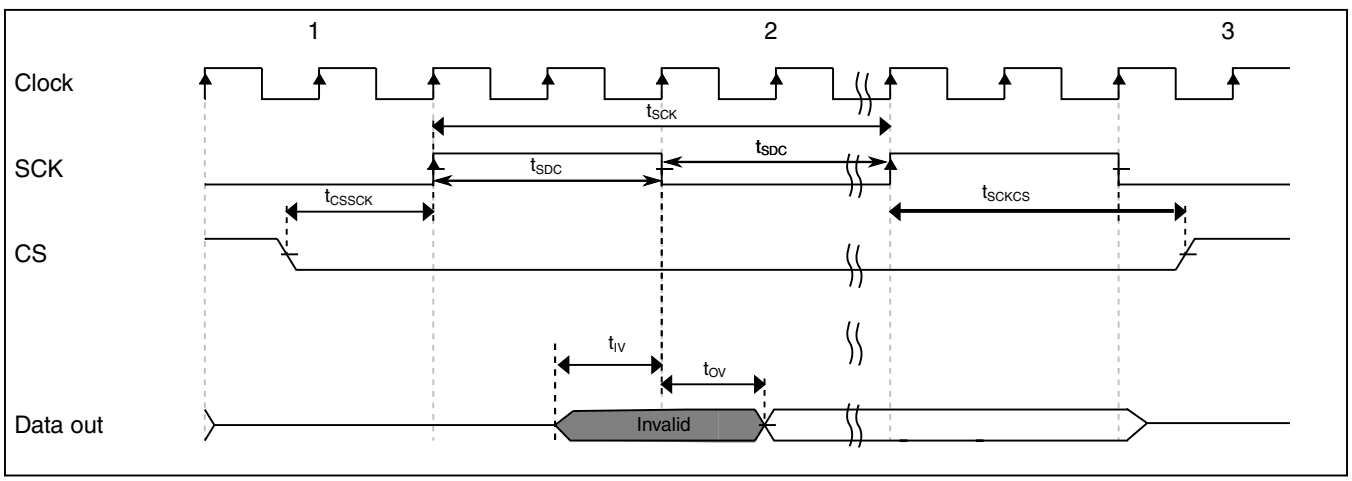
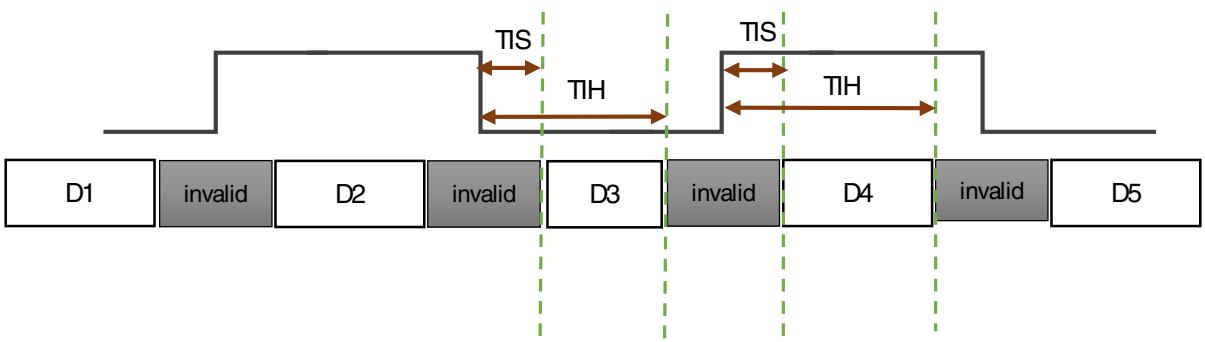


Figure 10. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time
TIH – Hold Time

Figure 11. QuadSPI input timing (HyperRAM mode) diagram

Table 27. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
f_{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	MHz	3, 4
f_{CONV}	ADC conversion frequency	No ADC hardware averaging.[5] Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	6, 7
		ADC hardware averaging set to 32. [5] Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	6, 7

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual* .
4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. Numbers based on the minimum sampling time of 275 ns.
7. For guidelines and examples of conversion rate calculation, see the *Reference Manual* section 'Calibration function'

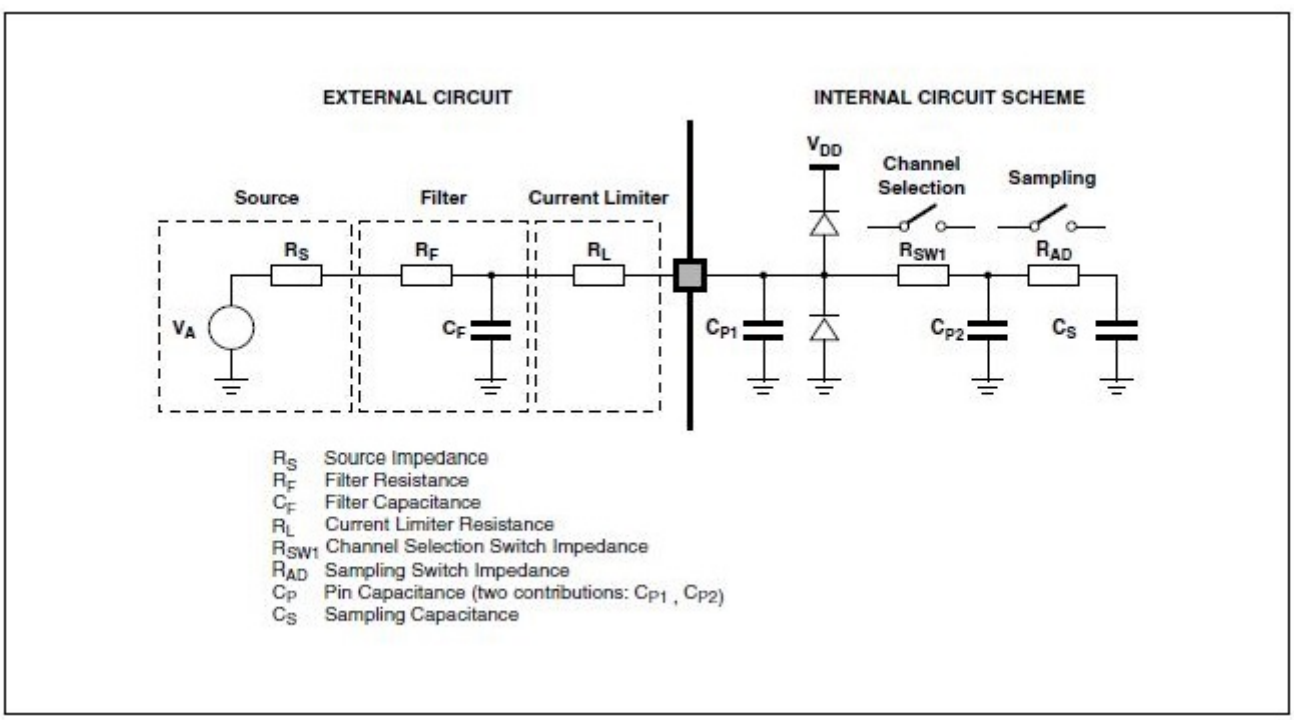


Figure 13. ADC input impedance equivalency diagram

Table 29. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS})

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	—	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

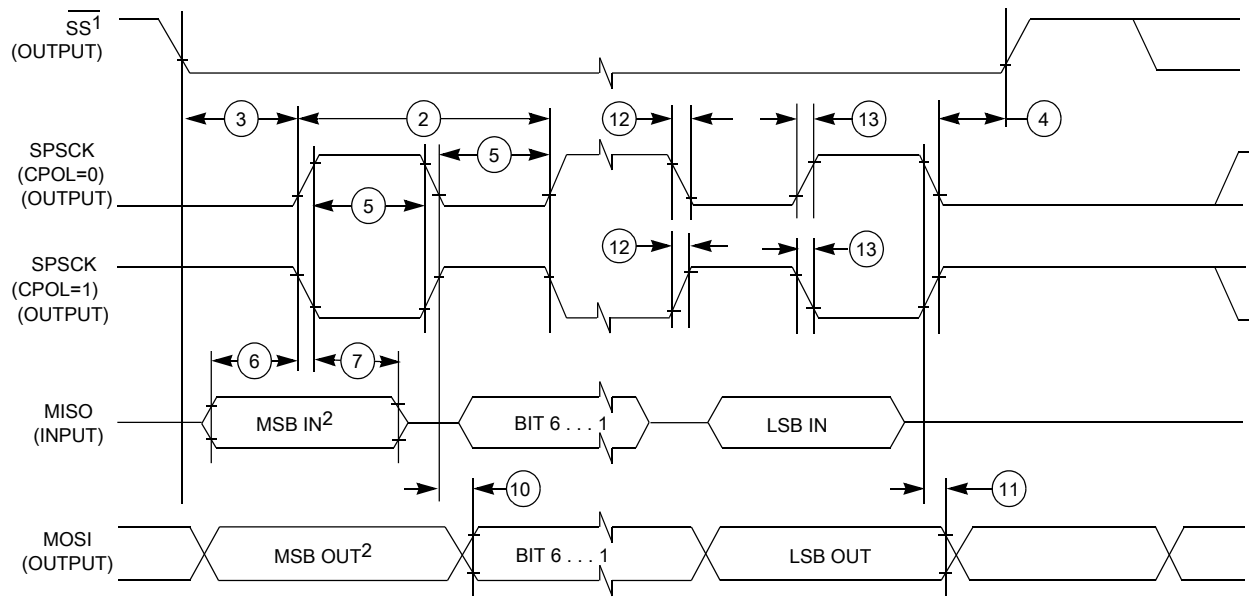
- Due to triple bonding in lower pin packages like 32-QFN, 48-LQFP, and 64-LQFP degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

Table 32. LPSPI electrical specifications[1] (continued)

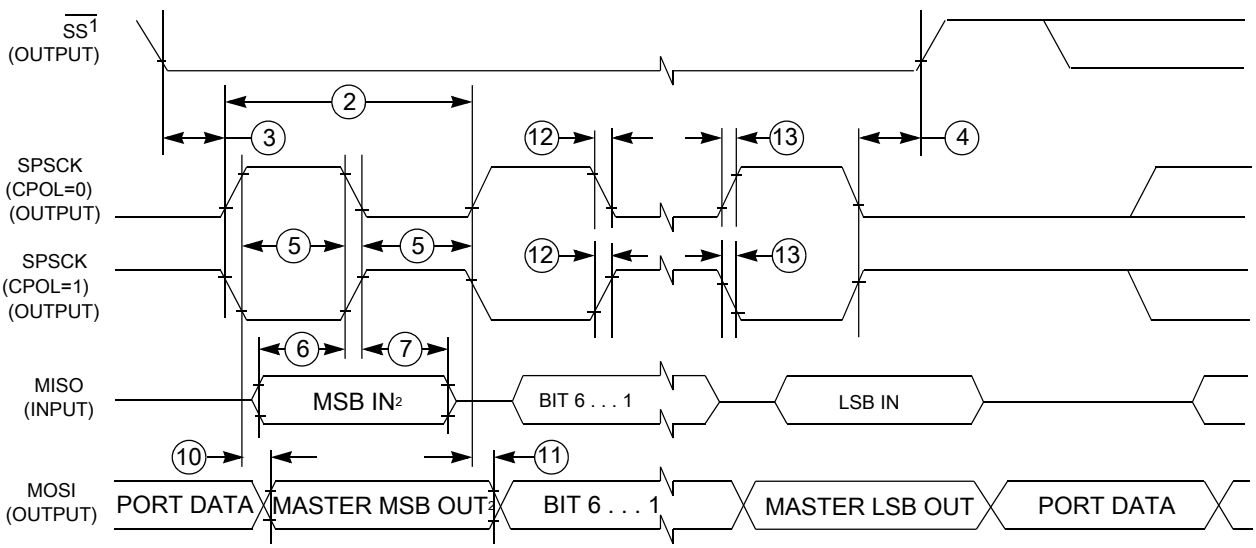
Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
4	t_{Lag}[9]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 25	-	(SCKPCS+1)*t_{periph}- 50	-	(SCKPCS+1)*t_{periph}- 50	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													
5	t_{WSPSCK}[10]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-3	t_{SPSCK}/2+3	t_{SPSCK}/2-5	t_{SPSCK}/2+5	t_{SPSCK}/2-5	t_{SPSCK}/2+5	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow)[6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37[11] 32[12]	-	72	-	78	-	
			Master Loopback[5]	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow)[6]	8	-	10	-	7	-	9	-	20	-	20	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow)[6]	3	-	3	-	3	-	3	-	12	-	12	-	

Table continues on the next page...



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. LPSPI master mode timing (CPHA = 1)

Table 36. RMII signal switching specifications (continued)

Symbol	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	2	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

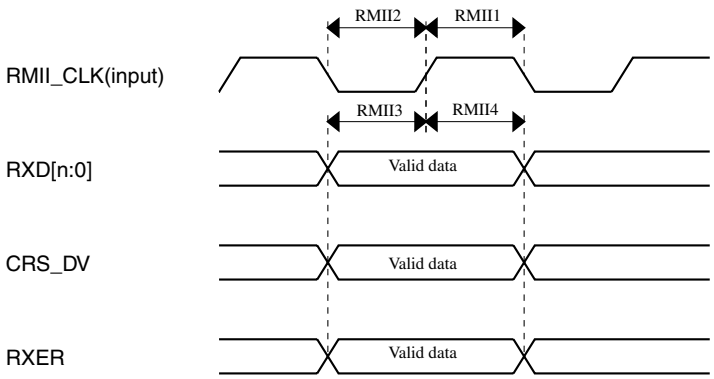


Figure 26. RMII receive diagram

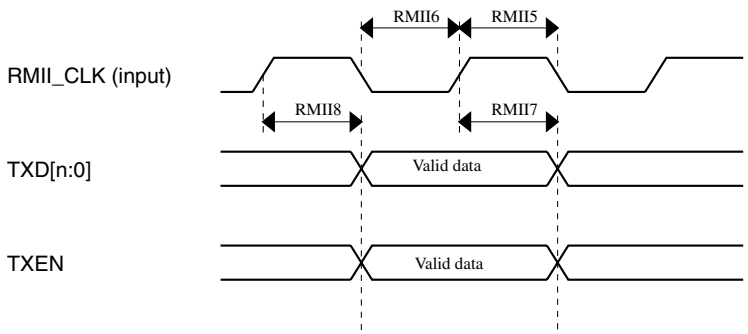


Figure 27. RMII transmit diagram

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- MDIO pin must have external Pull-up.

Table 37. MDIO timing specifications

Symbol	Description	Min.	Max.	Unit
—	MDC Clock Frequency	—	2.5	MHz

Table continues on the next page...

Table 40. JTAG electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
JI	TCLK frequency of operation													MHz
	Boundary Scan	-	20	-	20	-	20	-	20	-	10	-	10	
	JTAG	-	20	-	20	-	20	-	20	-	10	-	10	
J2	TCLK cycle period	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	ns
J3	TCLK clock pulse width													ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG													
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	5	-	5	-	15	-	15	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	5	-	5	-	8	-	8	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	3	-	3	-	15	-	15	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	2	-	2	-	8	-	8	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Package Top[7]	Natural Convection	Ψ_{JT}	32	1	NA	NA	NA	NA	NA	
			48	4	2	NA	NA	NA	NA	
			64	NA	2	2	2	2	NA	
			100	NA	NA	2	2	2	NA	
			144	NA	NA	NA	NA	2	1	
			176	NA	NA	NA	NA	NA	1	

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated values for V_{REFH} and V_{REFL} to add refernce to the section "voltage and current operating requirments" for Min and Max valaues • Updated footnote to Typ. • Removed footnote from RAS Analog source resistance • Updated figure: ADC input impedance equivalency diagram • In table: 12-bit ADC characteristics (2.7 V to 3 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS}) • Removed rows for V_{TEMP_S} and V_{TEMP25} • Updated footnote to Typ. • In table: 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS}) • Removed rows for V_{TEMP_S} and V_{TEMP25} • Removed number for TUE • Updated footnote to Typ. • In table: Comparator with 8-bit DAC electrical specifications • Updated Typ. of I_{DDLS} Supply current, Low-speed mode • Updated Typ. of t_{DLSB} Propagation delay, Low-speed mode • Updated Typ. of t_{DHSS} Propagation delay, High-speed mode • Updated t_{DLSS} Propagation delay • Added row for t_{DDAC} Initialization and switching settling time • Updated footnote • Updated section LPSPI electrical specifications • Added section: SAI electrical specifications • Updated section: Ethernet AC specifications • Added section: Clockout frequency • Added section: Trace electrical specifications • Updated table: Table 41 : Updated numbers for S32K142 and S32K148 • Updated table: Table 42 : Updated numbers for S32K148 • Updated Document number for 32-pin QFN in topic Obtaining package dimensions
3	14 March 2017	• In Table 2 • Updated min. value of V_{DD_OFF} • Added parameter I_{INJSUM_AF} • Updated Power mode transition operating behaviors • Updated Power consumption • Updated footnote to T_{SPLL_LOCK} in SPLL electrical specifications • In 12-bit ADC electrical characteristics • Updated table: 12-bit ADC characteristics (2.7 V to 3 V) (VREFH = VDDA, VREFL = VSS) • Added typ. value to I_{DDA_ADC}, TUE, DNL, and INL • Added min. value to SMPLTS • Removed footnote 'All the parameters in this table ... ' • Updated table: 12-bit ADC characteristics (3 V to 5.5 V) (VREFH = VDDA, VREFL = VSS) • Added typ. value to I_{DDA_ADC} • Removed footnote 'All the parameters in this table ... ' • In Flash timing specifications — commands updated Max. value of t_{vfykey} to 33 µs
4	02 June 2017	• In section: Block diagram, added block diagram for S32K11x series. • Updated figure: S32K1xx product series comparison. • In section: Selecting orderable part number , added reference to attachement *S32K_Part_Numbers.xlsx*. • In section: Ordering information • Updated figure: Ordering information. • In Table 1,

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes

		• Added footnote 'For S32K11x – FIRC/SOSC/FIRC/LPO; For S32K14x – FIRC/SOSC/FIRC/LPO/SPLL' to 'VLPS Mode: All clock sources disabled'
		• Updated numbers for:
		  • VLPR → VLPS
		  • VLPS → VLPR
		  • 'RUN → Compute operation'
		  • RUN → VLPS
		  • RUN → VLPR
		• In Power consumption :
		  • Updated specs for S32K142, S32K144, and S32K148
		  • Updated footnote 'Typical current numbers are indicative ...'
		  • Updated footnote 'The S32K148 data ...'
		  • Removed footnote 'Above S32K148 data is preliminary targets only'
		  • Added new table 'Power consumption at 3.3 V'
		• In General AC specifications :
		  • Updated max value and footnote of WFRST
		  • Updated symbol for not filtered pulse to 'WNFRST', updated min value, removed max. value, and added footnote
		• Fixed naming conventions to align with DS in DC electrical specifications at 3.3 V Range and DC electrical specifications at 5.0 V Range
		• Updated specs for AC electrical specifications at 3.3 V range and AC electrical specifications at 5 V range
		• In Device clock specifications :
		  • Updated f_{BUS} to 48 for 11x
		  • Added footnote to f_{BUS} for 14x
		• In External System Oscillator frequency specifications :
		  • Added specs for S32K11x
		  • Updated 't_{dc_extal}' for S32K14x
		  • Added footnote 'Frequecies below ... ' to 'f_{ec_extal}' and 't_{dc_extal}'
		• Splitted Flash timing specifications — commands for S32K14x and S32K11x
		• Updated Flash timing specifications — commands for S32K14x
		• In Reliability specifications :
		  • Added footnote 'Data retention period ... ' for 'tnvmretp1k' and 'tnvmretee'
		  • Minor update in footnote for 'nnvmwree16' 'nnvmwree256'
		• In QuadSPI AC specifications :
		  • Updated 'MCR[SCLKCFG[5]]' value to 0
		  • Updated 'Data Input Setup Time' HSRUN Internal DQS PAD Loopback value to 1.6
		  • Updated 'Data Input Setup Time' DDR External DQS min. value to 2
		  • Updated 'Data Input Hold Time' DDR External DQS min. value to 20
		  • Upadted figure 'QuadSPI output timing (SDR mode) diagram' and 'QuadSPI input timing (HyperRAM mode) diagram'
		• In 12-bit ADC electrical characteristics :
		  • Added note 'On reduced pin packages where ... '
		  • Removed max. value of 'I_{DDA_ADC}'
		  • Added note 'Due to triple ... '
		• In 12-bit ADC operating conditions, removed parameter 'ΔV_{DDA}'
		• In CMP with 8-bit DAC electrical specifications :
		  • Updated Typ. and Max. values of 'I_{DDLS}'
		  • Upadted Typ. value of 't_{DHSB}'
		  • Updated Typ. value of 'V_{HYST1}' , 'V_{HYST2}', and 'V_{HYST3}'
		• In LPSPI electrical specifications :
		  • Updated 'f_{periph}' and 'f_{op}', and 't_{SPSCK}'

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