Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, FlexIO, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	156
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b SAR; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k148hnt0vlut

- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
  - Up to one 10/100Mbps Ethernet with IEEE1588 support and two Synchronous Audio Interface (SAI) modules.
- Safety and Security
  - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
  - 128-bit Unique Identification (ID) number
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - System Memory Protection Unit (System MPU)
  - Cyclic Redundancy Check (CRC) module
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
- Timing and control
  - Up to eight independent 16-bit FlexTimers (FTM) modules, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- Package
  - 32-pin QFN, 48-pin LQFP, 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA, 144-pin LQFP, 176-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

3 Ordering information

3.1 Selecting orderable part number

Not all part number combinations are available. See the attachment *S32K1xx_Orderable_Part_Number_ List.xlsx* attached with the Datasheet for a list of standard orderable part numbers.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

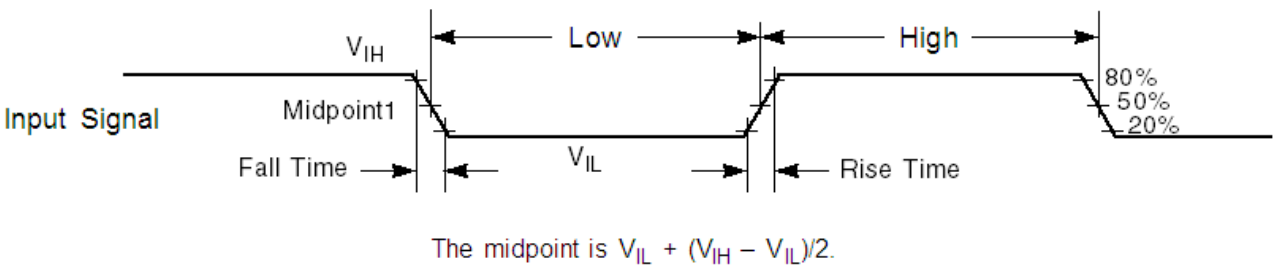


Figure 7. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	$\overline{\text{RESET}}$ input filtered pulse	—	10	ns	4
WNFRST	$\overline{\text{RESET}}$ input not filtered pulse	Maximum of (100 ns, bus clock period)	—	ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Maximum length of $\overline{\text{RESET}}$ pulse which will be filtered by internal filter.
5. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter. This number depends on bus clock period also. For example, in VLPR mode bus clock is 4 MHz, which make clock period of 250 ns. In this case, minimum pulse width which will cause reset is 250 ns. For faster bus clock frequencies which have clock period less than 100 ns, the minimum pulse width not filtered will be 100 ns.

Table 14. AC electrical specifications at 5 V Range (continued)

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
		17.3	54.8	17.6	59.7	200
	1	1.1	4.6	1.1	5.0	25
		2.0	5.7	2.0	5.8	50
		5.4	16.0	5.0	16.0	200
$tRF_{GPIO-FAST}$	0	0.42	2.2	0.37	2.2	25
		2.0	5.0	1.9	5.2	50
		9.3	18.8	8.5	19.3	200
	1	0.37	0.9	0.35	0.9	25
		1.2	2.7	1.2	2.9	50
		6.0	11.8	6.0	12.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 15. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 16. Device clock specifications [1]

Symbol	Description	Min.	Max.	Unit
High Speed run mode[2]				
f_{SYS}	System and core clock	—	112	MHz
f_{BUS}	Bus clock	—	56	MHz
f_{FLASH}	Flash clock	—	28	MHz
Normal run mode (S32K11x series)				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	48	MHz

Table continues on the next page...

Table 17. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Table 23. Flash command timing specifications for S32K14x (continued)

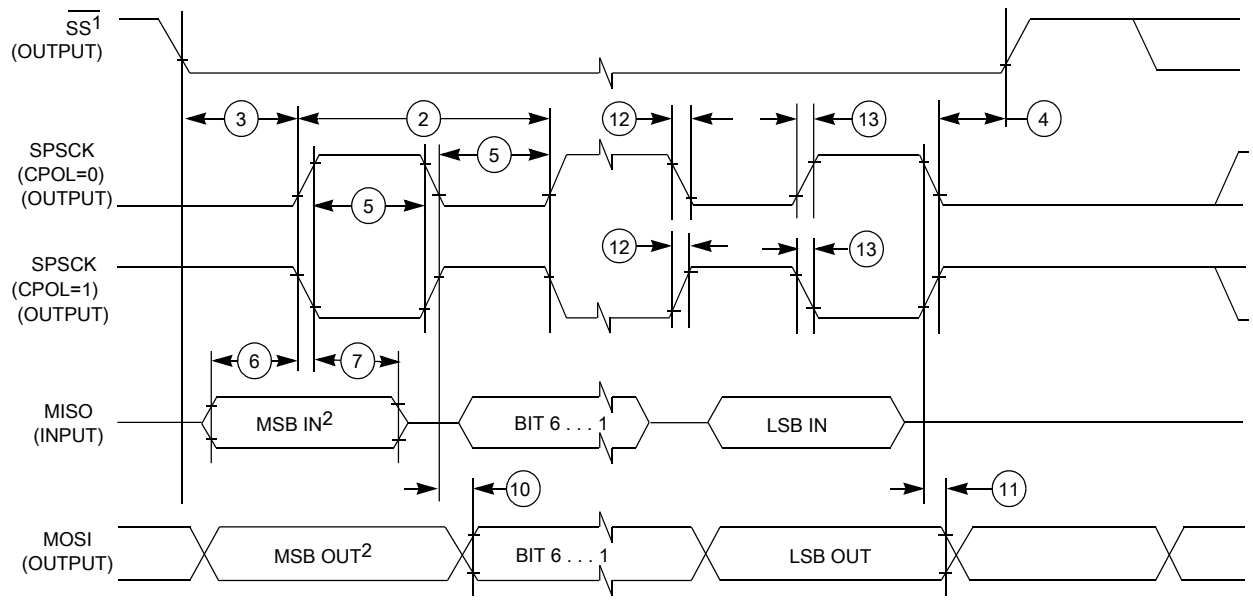
Symbol	Description[1]		S32K142		S32K144		S32K146		S32K148			
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Unit	Notes
t_{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	0.08	—	0.08	—	ms	3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2	0.8	1.2	—	—		
		48 KB EEPROM backup	1	1.5	1	1.5	1	1.5	—	—		
		64 KB EEPROM backup	1.3	1.9	1.3	1.9	1.3	1.9	1.3	1.9		
t_{eewr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr16b}$	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	385	1700	—	—	µs	3,4
		48 KB EEPROM backup	430	1850	430	1850	430	1850	—	—		
		64 KB EEPROM backup	475	2000	475	2000	475	2000	475	4000		
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	360	2000	360	2000	µs	
$t_{eewr32b}$	32-bit write to FlexRAM execution time	32 KB EEPROM backup	630	2000	630	2000	630	2000	—	—	µs	3,4
		48 KB EEPROM backup	720	2125	720	2125	720	2125	—	—		
		64 KB EEPROM backup	810	2250	810	2250	810	2250	810	4500		
$t_{quickwr}$	32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF	1st 32-bit write	200	550	200	550	200	550	200	1100	µs	4,5,6
		2nd through Next to Last (Nth-1) 32-bit write	150	550	150	550	150	550	150	550		

Table continues on the next page...

Table 32. LPSPI electrical specifications[1]

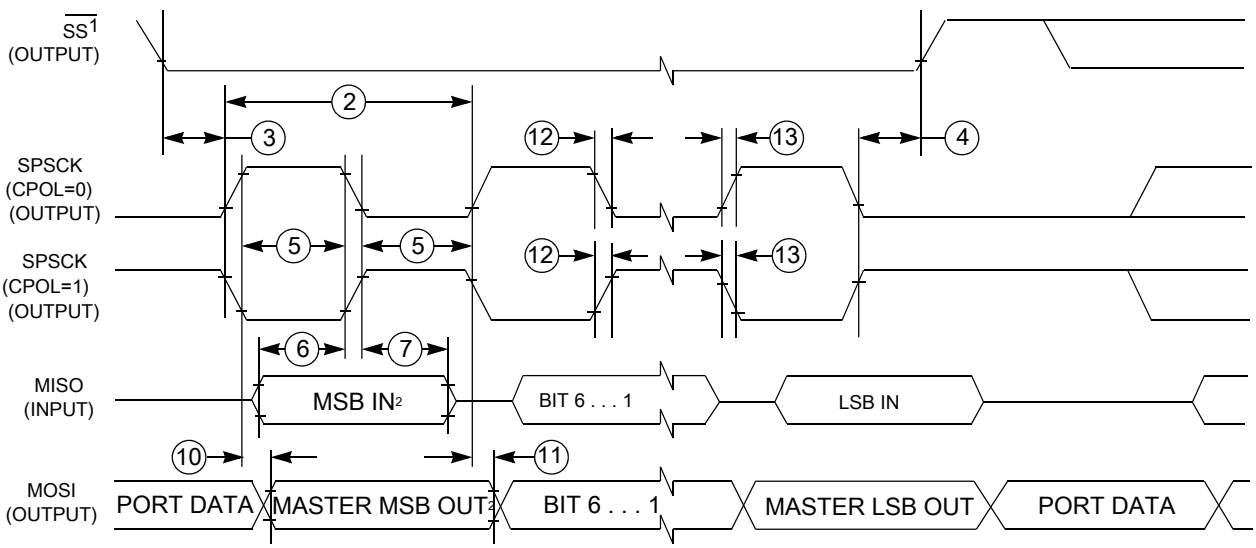
Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	f_{periph} [3, 4]	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	4	-	4	MHz
			Master	-	40	-	40	-	56	-	56	-	4	-	4	
			Master Loopback[5]	-	40	-	48	-	48	-	48	-	4	-	4	
			Master Loopback(slow)[6]	-	48	-	48	-	48	-	48	-	4	-	4	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14 [7]	-	2	-	2	MHz
			Master	-	10	-	10	-	14	-	14 [7]	-	2	-	2	
			Master Loopback[5]	-	20	-	12	-	24	-	12	-	2	-	2	
			Master Loopback(slow)[6]	-	12	-	12	-	12	-	12	-	2	-	2	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	500	-	500	-	ns
			Master	100	-	100	-	72	-	72	-	500	-	500	-	
			Master Loopback[5]	50	-	83	-	42	-	83	-	500	-	500	-	
			Master Loopback(slow)[6]	83	-	83	-	83	-	83	-	500	-	500	-	
3	t_{Lead}[8]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns
			Master	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-25	-	(PCSSCK+1)*t_{periph}-50	-	(PCSSCK+1)*t_{periph}-50	-	
			Master Loopback[5]													
			Master Loopback(slow)[6]													

Table continues on the next page...



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. LPSPI master mode timing (CPHA = 1)

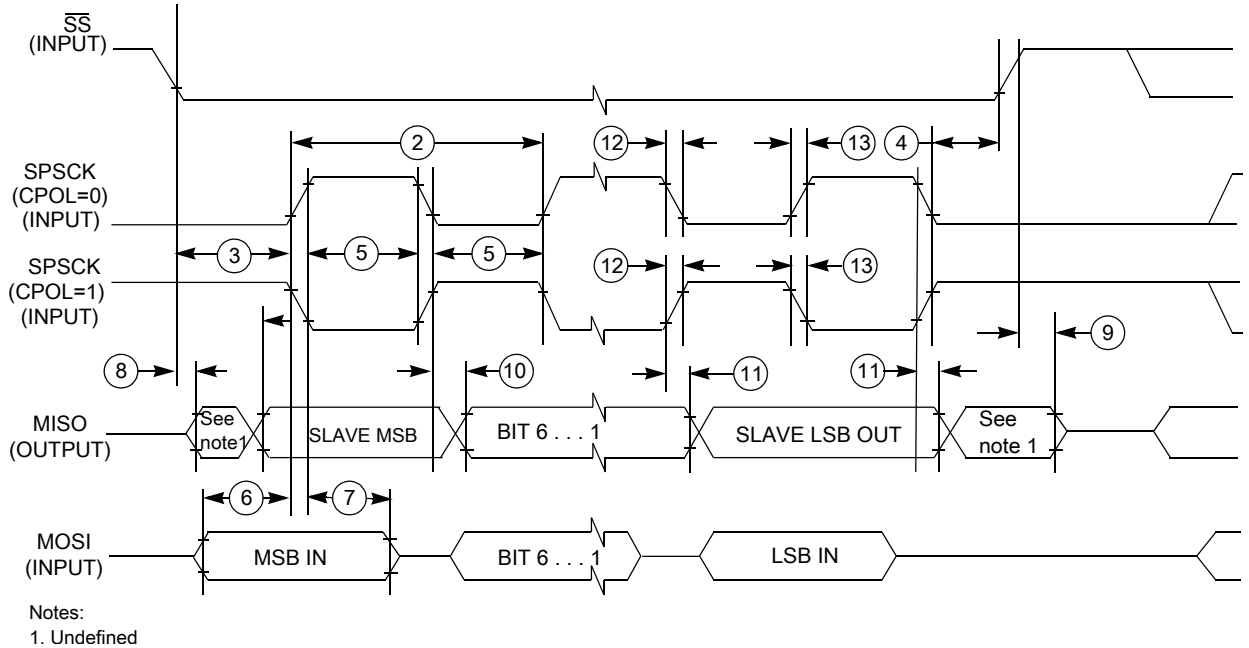


Figure 20. LPSPI slave mode timing (CPHA = 0)

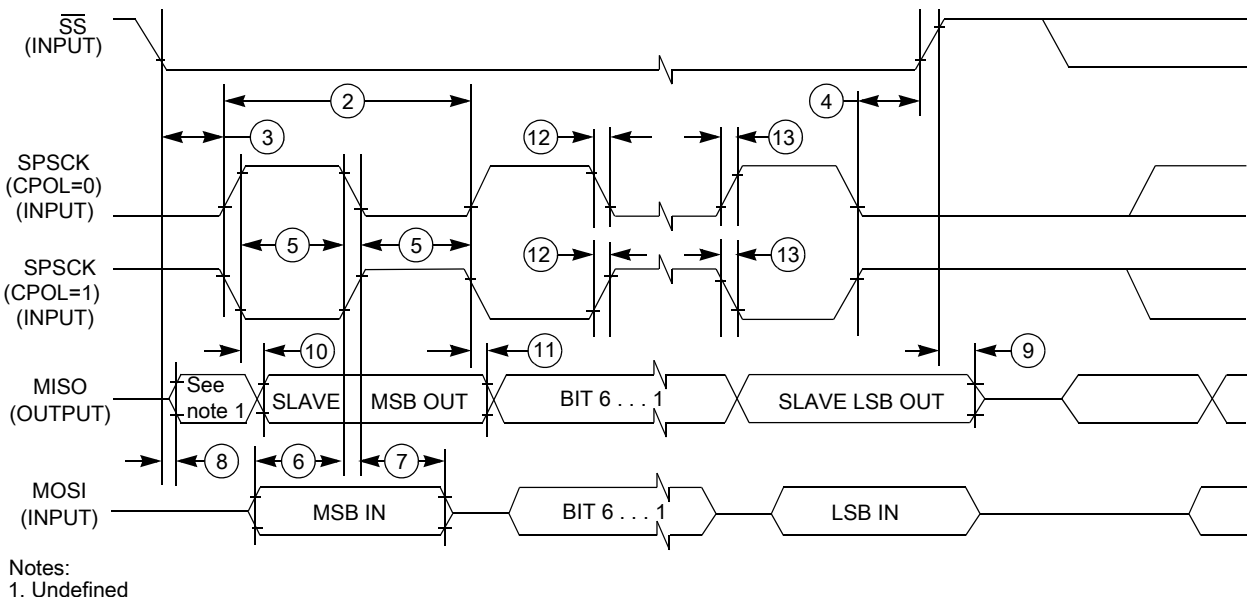


Figure 21. LPSPI slave mode timing (CPHA = 1)

6.5.3 LPI2C electrical specifications

See General AC specifications for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual.*

6.5.4 FlexCAN electical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

6.5.5 SAI electrical specifications

The following table describes the SAI electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 33. Master mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	—	ns
S4	SAI_BCLK pulse width high/low	45%	55%	BCLK period
S5	SAI_RXD input setup before SAI_BCLK	28	—	ns
S6	SAI_RXD input hold after SAI_BCLK	0	—	ns
S7	SAI_BCLK to SAI_TXD output valid	—	8	ns
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	ns
S9	SAI_FS input setup before SAI_BCLK	28	—	ns
S10	SAI_FS input hold after SAI_BCLK	0	—	ns
S11	SAI_BCLK to SAI_FS output valid	—	8	ns
S12	SAI_BCLK to SAI_FS output invalid	-2	—	ns

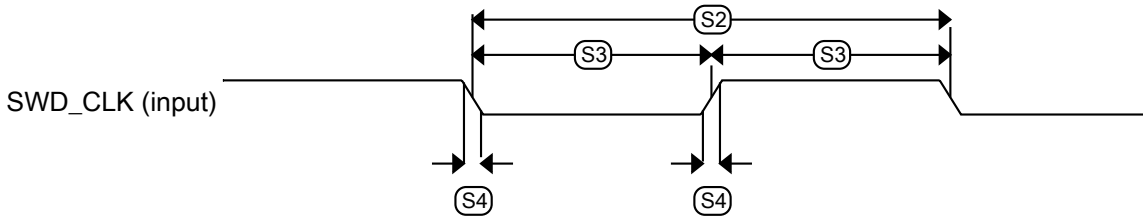


Figure 29. Serial wire clock input timing

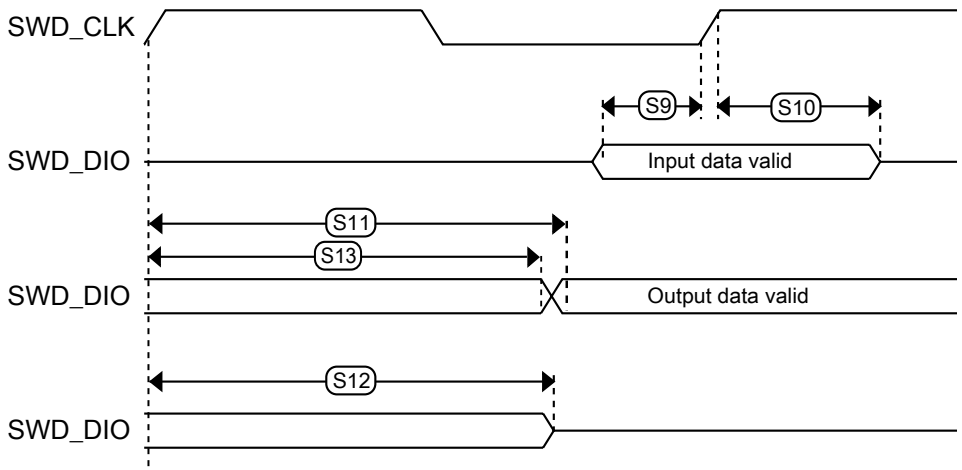


Figure 30. Serial wire data timing

6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 39. Trace specifications

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
—	Fsys	System frequency	80	48	40	112	80	4	MHz

Table continues on the next page...

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

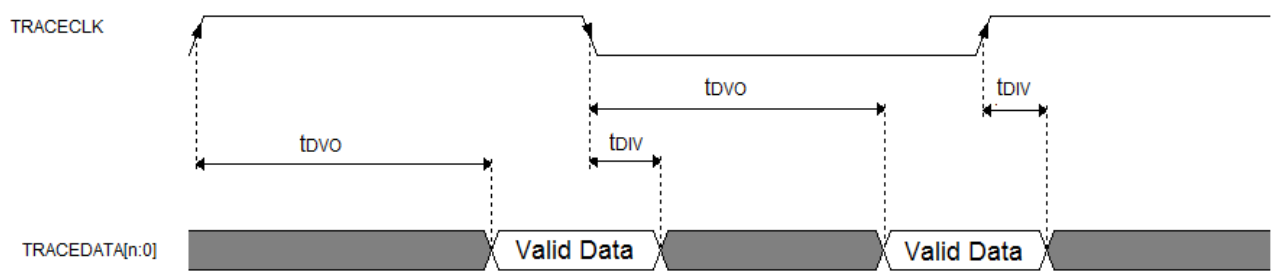


Figure 31. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

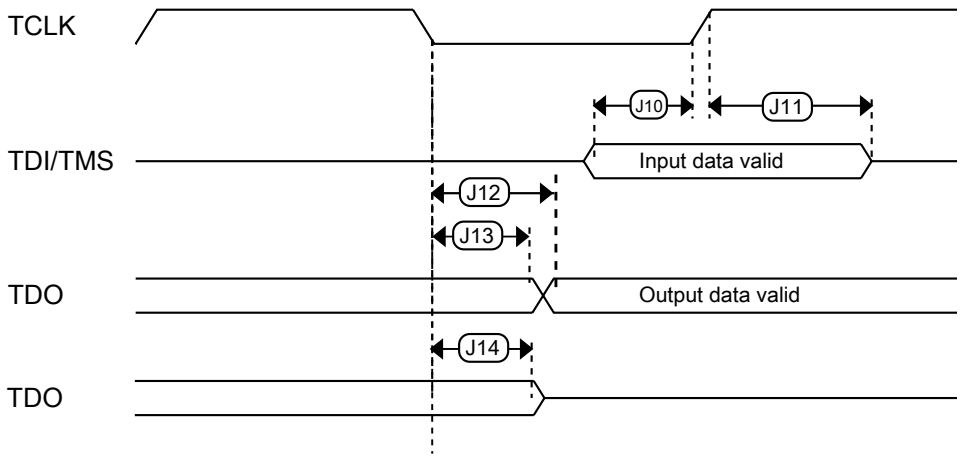


Figure 34. Test Access Port timing

7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	32	93	NA	NA	NA	NA	NA	°C/W
			48	79	71	NA	NA	NA	NA	
			64	NA	62	61	61	59	NA	
			100	NA	NA	53	52	51	NA	
			144	NA	NA	NA	NA	51	44	
			176	NA	NA	NA	NA	NA	42	
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Two layer board (1s1p)	$R_{\theta JA}$	32	50	NA	NA	NA	NA	NA	
			48	58	50	NA	NA	NA	NA	
			64	NA	46	45	45	44	NA	
			100	NA	NA	42	42	40	NA	
			144	NA	NA	NA	NA	44	37	
			176	NA	NA	NA	NA	NA	36	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	32	32	NA	NA	NA	NA	NA	
			48	55	47	NA	NA	NA	NA	
			64	NA	44	43	43	41	NA	
			100	NA	NA	40	40	39	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	35	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	32	77	NA	NA	NA	NA	NA	
			48	66	58	NA	NA	NA	NA	
			64	NA	50	49	49	48	NA	
			100	NA	NA	43	42	41	NA	
			144	NA	NA	NA	NA	42	36	
			176	NA	NA	NA	NA	NA	34	
Thermal resistance, Junction to Ambient (@200 ft/min)[1]	Two layer board (1s1p)	$R_{\theta JMA}$	32	43	NA	NA	NA	NA	NA	
			48	51	43	NA	NA	NA	NA	
			64	NA	39	38	38	37	NA	
			100	NA	NA	35	35	34	NA	

Table continues on the next page...

Table 41. Thermal characteristics for 32-pin QFN and 48/64/100/144/176-pin LQFP package (continued)

Rating	Conditions	Symbol	Package	Values						Unit
				S32K116	S32K118	S32K142	S32K144	S32K146	S32K148	
			144	NA	NA	NA	NA	37	31	
			176	NA	NA	NA	NA	NA	30	
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	32	26	NA	NA	NA	NA	NA	
			48	48	41	NA	NA	NA	NA	
			64	NA	37	36	36	35	NA	
			100	NA	NA	34	34	33	NA	
			144	NA	NA	NA	NA	36	30	
			176	NA	NA	NA	NA	NA	29	
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	32	11	NA	NA	NA	NA	NA	
			48	33	24	NA	NA	NA	NA	
			64	NA	26	25	25	23	NA	
			100	NA	NA	25	25	24	NA	
			144	NA	NA	NA	NA	30	24	
			176	NA	NA	NA	NA	NA	24	
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	32	NA	NA	NA	NA	NA	NA	
			48	23	19	NA	NA	NA	NA	
			64	NA	14	13	12	11	NA	
			100	NA	NA	13	12	11	NA	
			144	NA	NA	NA	NA	12	9	
			176	NA	NA	NA	NA	NA	9	
Thermal resistance, Junction to Case (Bottom) [6]	—	$R_{\theta JCBottom}$	32	1	NA					
			48	NA						
			64							
			100							
			144							
			176							

Table continues on the next page...

Table 42. Thermal characteristics for the 100 MAPBGA package

Rating	Conditions	Symbol	Values			Unit
			S32K146	S32K144	S32K148	
Thermal resistance, Junction to Ambient (Natural Convection) [1, 2]	Single layer board (1s)	$R_{\theta JA}$	57.2	61.0	52.5	°C/W
Thermal resistance, Junction to Ambient (Natural Convection) [1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	32.1	35.6	27.5	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min) [1, 2, 3]	Single layer board (1s)	$R_{\theta JMA}$	44.1	46.6	39.0	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Two layer board (2s2p)	$R_{\theta JMA}$	27.2	30.9	22.8	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	15.3	18.9	11.2	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	10.2	14.2	7.5	°C/W
Thermal resistance, Junction to Package Top outside center[6]	—	Ψ_{JT}	0.2	0.4	0.2	°C/W
Thermal resistance, Junction to Package Bottom outside center[7]	—	Ψ_{JB}	12.2	15.9	18.3	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number
32-pin QFN	SOT617-3 [1]
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W
100-pin MAPBGA	98ASA00802D
144-pin LQFP	98ASS23177W
176-pin LQFP	98ASS23479W

1. 5x5 mm package

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated note 'All the limits defined ... ' • Updated parameter '$I_{INJPAD\_DC\_ABS}$', 'V_{IN_DC}', $I_{INJSUM\_DC\_ABS}$. • In Table 2, • Updated parameter $I_{INJPAD\_DC\_OP}$ and $I_{INJSUM\_DC\_OP}$. • In Table 5, updated TBDs for V_{LVR_HYST}, V_{LVD_HYST}, and $_{VLVW\_HYST}$ • In Power mode transition operating behaviors, • Added VLPR → VLPS • Added VLPS → VLPR • Updated TBDs for VLPS → Asynchronous DMA Wakeup, STOP1 → Asynchronous DMA Wakeup, and STOP2 → Asynchronous DMA Wakeup • In Table 7, updated the specifications for S32K144. • Updated the attachment *S32K1xx_Power_Modes _Configuration.xlsx*. • In Table 15, removed C_{IN_A}. • In Table 17, • Updated specificatins for g_{mXOSC}. • Removed I_{DDOSC} • In Table 19, • Added parameter ΔF125. • Removed I_{DDFIRC} • In Table 20, • Added parameter ΔF125. • Removed I_{DDSIRC} • In Table 21, removed I_{LPO} • Updated section: Flash memory module (FTFC) electrical specifications • In section: 12-bit ADC operating conditions, • Updated TBDs for I_{DDA_ADC} and TUE in Table 28 • Updated TBDs for I_{DDA_ADC} and TUE in Table 29 • In section: QuadSPI AC specifications, updated figure 'QuadSPI output timing (HyperRAM mode) diagram'. • In section: 12-bit ADC operating conditions, updated Table 27. • In section: CMP with 8-bit DAC electrical specifications, added note 'For comparator IN signals adjacent ... ' • In table: Table 32, minor update in footnote 6. • In table: Table 41, updated specifications for S32K146.
5	06 Dec 2017	• Removed S32K148 from 'Caution' • Updated figure: S32K1xx product series comparison for • 'EEPROM emulated by FlexRAM' of S32K148 (Added content to footnote) • Added support for LIN protocol version 2.2 A • In Absolute maximum ratings : • Added note 'Unless otherwise ... ' • Added parameter 'Added note 'T_{ramp_MCU}' • Updated footnote for 'T_{ramp}' • In Voltage and current operating requirements : • Added footnote 'V_{DD} and V_{DDA} must be shorted ... ' against parameter 'V_{DD}– V_{DDA}' • Updated footnote 'V_{DD} and V_{DDA} must be shorted ...' • In Power and ground pins • Added diagrams for 32-QFN and 48-LQFP and footnote below the diagrams. • Updated footnote 'V_{DD} and V_{DDA} must be shorted ...' • In Power mode transition operating behaviors :

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes

		• Added footnote 'For S32K11x – FIRC/SOSC/FIRC/LPO; For S32K14x – FIRC/SOSC/FIRC/LPO/SPLL' to 'VLPS Mode: All clock sources disabled'
		• Updated numbers for:
		  • VLPR → VLPS
		  • VLPS → VLPR
		  • 'RUN → Compute operation'
		  • RUN → VLPS
		  • RUN → VLPR
		• In Power consumption :
		  • Updated specs for S32K142, S32K144, and S32K148
		  • Updated footnote 'Typical current numbers are indicative ...'
		  • Updated footnote 'The S32K148 data ...'
		  • Removed footnote 'Above S32K148 data is preliminary targets only'
		  • Added new table 'Power consumption at 3.3 V'
		• In General AC specifications :
		  • Updated max value and footnote of WFRST
		  • Updated symbol for not filtered pulse to 'WNFRST', updated min value, removed max. value, and added footnote
		• Fixed naming conventions to align with DS in DC electrical specifications at 3.3 V Range and DC electrical specifications at 5.0 V Range
		• Updated specs for AC electrical specifications at 3.3 V range and AC electrical specifications at 5 V range
		• In Device clock specifications :
		  • Updated f_{BUS} to 48 for 11x
		  • Added footnote to f_{BUS} for 14x
		• In External System Oscillator frequency specifications :
		  • Added specs for S32K11x
		  • Updated 't_{dc_extal}' for S32K14x
		  • Added footnote 'Frequecies below ... ' to 'f_{ec_extal}' and 't_{dc_extal}'
		• Splitted Flash timing specifications — commands for S32K14x and S32K11x
		• Updated Flash timing specifications — commands for S32K14x
		• In Reliability specifications :
		  • Added footnote 'Data retention period ... ' for 'tnvmretp1k' and 'tnvmretee'
		  • Minor update in footnote for 'nnvmwree16' 'nnvmwree256'
		• In QuadSPI AC specifications :
		  • Updated 'MCR[SCLKCFG[5]]' value to 0
		  • Updated 'Data Input Setup Time' HSRUN Internal DQS PAD Loopback value to 1.6
		  • Updated 'Data Input Setup Time' DDR External DQS min. value to 2
		  • Updated 'Data Input Hold Time' DDR External DQS min. value to 20
		  • Upadted figure 'QuadSPI output timing (SDR mode) diagram' and 'QuadSPI input timing (HyperRAM mode) diagram'
		• In 12-bit ADC electrical characteristics :
		  • Added note 'On reduced pin packages where ... '
		  • Removed max. value of 'I_{DDA_ADC}'
		  • Added note 'Due to triple ... '
		• In 12-bit ADC operating conditions, removed parameter 'ΔV_{DDA}'
		• In CMP with 8-bit DAC electrical specifications :
		  • Updated Typ. and Max. values of 'I_{DDLS}'
		  • Upadted Typ. value of 't_{DHSB}'
		  • Updated Typ. value of 'V_{HYST1}' , 'V_{HYST2}', and 'V_{HYST3}'
		• In LPSPI electrical specifications :
		  • Updated 'f_{periph}' and 'f_{op}', and 't_{SPSCK}'

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated 3.3 V numbers and added footnote against f_{op}, t_{SU}, ans t_V in HSRUN Mode • Added footnote to 't_{WSPSCK}' • Updated Thermal characteristics for S32K11x
6	31 Jan 2018	• Changed the representation of ARM trademark throughout. • Removed S32K142 from 'Caution' • In 'Key features', added the following note under 'Power management', 'Memory and memory interfaces', and 'Reliability, safety and security': • No write or erase access to ... • In High-level architecture diagram for the S32K14x family, added the following footnote: • No write or erase access to ... • In High-level architecture diagram for the S32K11x family : • Minor editorial update: Fixed the placement of SRAM, under 'Flash memory controller' block • Updated figure: S32K1xx product series comparison : • Updated footnote 1, and added against 'HSRUN' in addition to 'HW security module (CSEc)' and 'EEPROM emulated by FlexRAM'. • Updated 'System RAM (including FlexRAM and MTB)' row for S32K144, S32K146, and S32K148. • Updated channel count for S32K116 in row '12-bit SAR ADC (1 MSPS each)'. • Updated Ordering information • Updated Flash timing specifications — commands for S32K148, S32K142, S32K146, S32K116, and S32K118.
7	19 April 2018	• Changed Caution to Notes • Updated the wordings of Notes and removed S32K146 • Added 'Following two are the available ...' • In 'Key features' : • Editorial updates • Updated the note under Power management, Memory and memory interfaces, and Safety and security. • Updated FlexIO under Communications interfaces • Added ENET and SAI under Communications interfaces • Updated Cryptographic Services Engine (CSEc) under 'Safety and security' • In High-level architecture diagram for the S32K14x family : • Minor editorial updates • Updated note 3 • In High-level architecture diagram for the S32K11x family : • Minor editorial updates • In figure: S32K1xx product series comparison : • Editorial updates • Updated Frequency for S32K14x • Updated footnote 4 • Added footnote 5 • In Ordering information : • Renamed section, updated the starting paragraph • Updated the figure • In Voltage and current operating requirements, updated the note • In Power consumption : • Updated specs for S32K146 • Removed section 'Modes configuration', amd moved its content under the fisrt paragraph. • In 12-bit ADC operating conditions :

Table continues on the next page...