



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

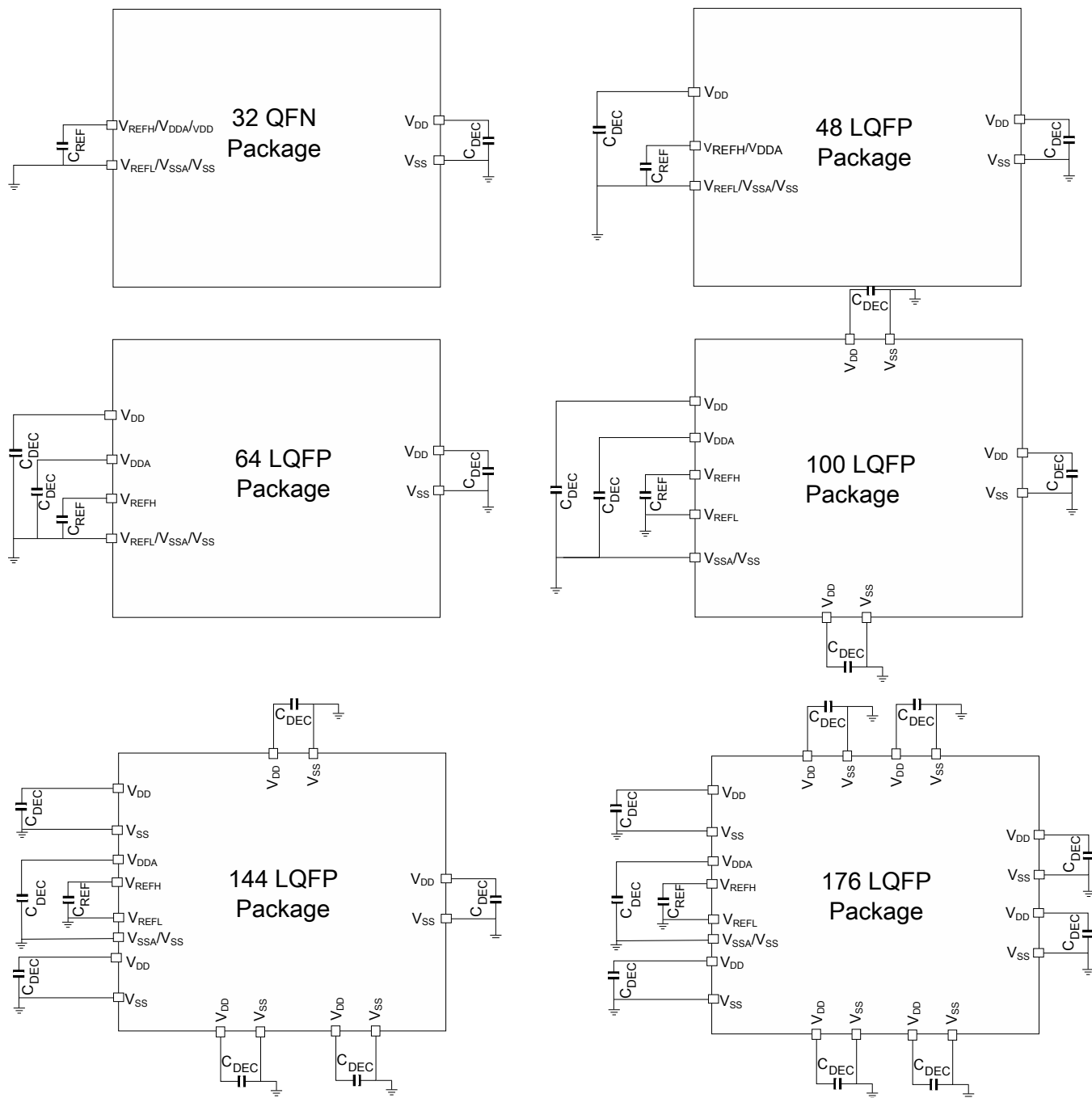
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	112MHz
Connectivity	CANbus, Ethernet, FlexIO, I ² C, LINbus, SPI, UART/USART
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	128
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b SAR; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/fs32k148ujt0vlqt

4.4 Power and ground pins



NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB

Figure 5. Pinout decoupling

Table 7. Power consumption (Typicals unless stated otherwise) ¹

Chip/Device	Ambient Temperature (°C)		VLPS (μA) ²		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) ³		IDD/MHz (μA/MHz) ⁴
			Peripherals disabled ⁵	Peripherals enabled	Peripherals disabled ⁶	Peripherals enabled use case 1 ⁶	Peripherals enabled use case 2 ⁷			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
S32K116	25	Typ	26	40	1.05	1.07	TBD	6.3	7.2	11.8	20.3	NA						245
	85	Typ	76	93	1.1	1.11	TBD	6.6	7.5	12	20.6							251
		Max	287	300	1.39	1.4	NA	8	8.9	13.4	22.1							279
	105	Typ	139	164	1.15	1.16	TBD	6.8	7.7	12.3	20.8							255
		Max	590	603	1.68	1.69	NA	9.2	10.1	14.5	23.1							302
	125	Typ	NA	NA	NA	NA	TBD	NA	NA	NA	NA							NA
		Max	891	904	2.02	2.04	NA	10.4	11.3	15.6	24.1							325
S32K118	25	Typ	26	38	1.9	2.5	TBD	7	12	TBD	TBD	NA						TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD							TBD
S32K142	25	Typ	29	40	1.17	1.21	2.19	6.4	7.4	17.3	24.6	24.5	31.3	28.8	37.5	40.5	52.2	360
	85	Typ	128	137	1.48	1.51	2.31	7	8	17.6	24.9	25	31.6	29.1	37.7	41.1	52.5	364
		Max	335	360	1.87	1.89	NA	8.6	9.4	22	28.2	26.9	33.5	32	40	44	55.6	400
	105	Typ	240	257	1.58	1.61	2.44	7.6	8.3	18.3	25.7	25.5	31.9	29.8	38	41.5	53.1	373
		Max	740	791	2.32	2.34	NA	9.9	10.9	23.1	30.2	27.8	35.3	33.8	40.7	44.9	57.4	423
	125	Typ	NA	NA	NA	NA	2.84	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA

Table continues on the next page...

Table 7. Power consumption (Typicals unless stated otherwise) 1 (continued)

Chip/Device	Ambient Temperature (°C)		VLPS (μA) ²		VLPR (mA)			STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) ³		IDD/MHz (μA/MHz) ⁴
			Peripherals disabled ⁵	Peripherals enabled	Peripherals disabled ⁶	Peripherals enabled use case 1 ⁶	Peripherals enabled use case 2 ⁷			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
		Max	1637	1694	3.1	3.21	NA	12.7	13.7	25	32.9	30.7	38.8	36	43.8	NA		450
S32K144	25	Typ	29.8	42	1.48	1.50	2.91	7	7.7	19.7	26.9	25.1	33.3	30.2	39.6	43.3	55.6	378
	85	Typ	150	159	1.72	1.85	3.08	7.2	8.1	20.4	27.1	26.1	33.5	30.5	40	43.9	56.1	381
		Max	359	384	2.60	2.65	NA	9.2	9.9	23.2	29.6	29.3	36.2	34.8	42.1	46.3	59.7	435
	105	Typ	256	273	1.80	2.10	3.23	7.8	8.5	20.6	27.4	26.6	33.8	31.2	40.5	44.8	57.1	390
		Max	850	900	2.65	2.70	NA	10.3	11.1	23.9	30.6	30.3	37.3	35.6	43.5	47.9	61.3	445
	125	Typ	NA	NA	NA	NA	3.65	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	1960	1998	3.18	3.25	NA	12.9	13.8	26.9	33.6	35	40.3	38.7	46.8	NA		484
S32K146	25	Typ	37	47	1.57	1.61	3.3	8	9.2	23.4	31.4	30.5	40.2	36.2	47.6	52	68.3	452
	85	Typ	207	209	1.79	1.83	3.54	8.9	10.1	24.4	32.4	31.5	41.3	37.2	48.7	53.3	69.8	465
		Max	974	981	3.32	3.38	NA	12.7	13.9	29.3	37.9	36.7	47	42.4	54.4	60.3	78	530
	105	Typ	419	422	1.99	2.04	3.78	9.8	11	25.3	33.4	32.5	42.2	38.1	49.6	54.4	70.8	477
		Max	2004	2017	4.06	4.13	NA	17.1	18.3	34.1	42.6	41.3	51.4	46.9	58.8	65.7	82.8	587
	125	Typ	NA	NA	NA	NA	4.44	NA	NA	NA	NA	NA	NA	NA	NA	NA		NA
		Max	3358	3380	5.28	5.38	NA	22.6	23.7	40.2	48.8	47.3	57.4	52.8	64.8	NA		660
S32K148 ⁸	25	Typ	38	54	2.17	2.20	3.45	8.5	9.6	27.6	34.9	35.5	45.3	42.1	57.7	60.3	83.3	526
	85	Typ	336	357	2.30	2.35	3.74	10.1	11.1	29.1	37.0	36.8	46.6	43.4	59.9	62.9	88.7	543

Table continues on the next page...

I/O parameters

- Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details see IO Signal Description Input Multiplexing sheet(s) attached with the *Reference Manual*.
- When using ENET and SAI on S32K148, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
- Measured at input $V = V_{SS}$
- Measured at input $V = V_{DD}$

5.4 DC electrical specifications at 5.0 V Range

Table 12. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	$0.65 \times V_{DD}$	—	$V_{DD} + 0.3$	V	1
V_{il}	Input Buffer Low Voltage	$V_{SS} - 0.3$	—	$0.35 \times V_{DD}$	V	2
V_{hys}	Input Buffer Hysteresis	$0.06 \times V_{DD}$	—	—	V	
I_{ohGPIO} $I_{ohGPIO-HD_DSE_0}$	I/O current source capability measured when pad $V_{oh} = (V_{DD} - 0.8 \text{ V})$	5	—	—	mA	
I_{olGPIO} $I_{olGPIO-HD_DSE_0}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	5	—	—	mA	
$I_{ohGPIO-HD_DSE_1}$	I/O current source capability measured when pad $V_{oh} = V_{DD} - 0.8 \text{ V}$	20	—	—	mA	3
$I_{olGPIO-HD_DSE_1}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	20	—	—	mA	3
$I_{ohGPIO-FAST_DSE_0}$	I/O current sink capability measured when pad $V_{oh} = V_{DD} - 0.8 \text{ V}$	14.0	—	—	mA	4
$I_{olGPIO-FAST_DSE_0}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	14.5	—	—	mA	4
$I_{ohGPIO-FAST_DSE_1}$	I/O current sink capability measured when pad $V_{oh} = V_{DD} - 0.8 \text{ V}$	21	—	—	mA	4
$I_{olGPIO-FAST_DSE_1}$	I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$	20.5	—	—	mA	4
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at $V_{DD} = 5.5 \text{ V}$					5
	All pins other than high drive port pins		0.005	0.5	μA	
	High drive port pins		0.010	0.5	μA	
R_{PU}	Internal pullup resistors	20		50	$k\Omega$	6
R_{PD}	Internal pulldown resistors	20		50	$k\Omega$	7

- For reset pads, same V_{ih} levels are applicable
- For reset pads, same V_{il} levels are applicable
- The strong pad I/O pin is capable of switching a 50 pF load up to 40 MHz.
- For reference only. Run simulations with the IBIS model and custom board for accurate results.

5. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *SK3K144_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
6. Measured at input $V = V_{SS}$
7. Measured at input $V = V_{DD}$

5.5 AC electrical specifications at 3.3 V range

Table 13. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max.	Min.	Max.	
tRF _{GPIO}	NA	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
tRF _{GPIO-HD}	0	3.2	14.5	3.4	15.7	25
		5.7	23.7	6.0	26.2	50
		20.0	80.0	20.8	88.4	200
	1	1.5	5.8	1.7	6.1	25
		2.4	8.0	2.6	8.3	50
		6.3	22.0	6.0	23.8	200
tRF _{GPIO-FAST}	0	0.6	2.8	0.5	2.8	25
		3.0	7.1	2.6	7.5	50
		12.0	27.0	10.3	26.8	200
	1	0.4	1.3	0.38	1.3	25
		1.5	3.8	1.4	3.9	50
		7.4	14.9	7.0	15.3	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 14. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS) ¹		Fall time (nS) ¹		Capacitance (pF) ²
		Min.	Max .	Min.	Max.	
tRF _{GPIO}	NA	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50
		17.3	54.8	17.6	59.7	200
tRF _{GPIO-HD}	0	2.8	9.4	2.9	10.7	25
		5.0	15.7	5.1	17.4	50

Table continues on the next page...

Table 16. Device clock specifications 1 (continued)

Symbol	Description	Min.	Max.	Unit
f _{FLASH}	Flash clock	—	24	MHz
Normal run mode (S32K14x series) ³				
f _{SYS}	System and core clock	—	80	MHz
f _{BUS}	Bus clock	—	40 ⁴	MHz
f _{FLASH}	Flash clock	—	26.67	MHz
VLPR mode ⁵				
f _{SYS}	System and core clock	—	4	MHz
f _{BUS}	Bus clock	—	4	MHz
f _{FLASH}	Flash clock	—	1	MHz
f _{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section [Feature comparison](#) for the availability of modes and other specifications.
2. Only available on some devices. See section [Feature comparison](#).
3. With SPLP as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

Table 18. External System Oscillator frequency specifications

Symbol	Description	Min.		Typ.		Max.		Unit	Notes
		S32K14x	S32K11x	S32K14x	S32K11x	S32K14x	S32K11x		
f _{osc_hi}	Oscillator crystal or resonator frequency	4		—		40		MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—		—		50	48	MHz	1
t _{dc_extal}	Input clock duty cycle (external clock mode)	48		50		52		%	1
t _{cst}	Crystal Start-up Time								
	8 MHz low-gain mode (HGO=0)	—		1.5		—		ms	2
	8 MHz high-gain mode (HGO=1)	—		2.5		—			
	40 MHz low-gain mode (HGO=0)	—		2		—			
	40 MHz high-gain mode (HGO=1)	—		2		—			

1. Frequencies below 40 MHz can be used for degraded duty cycle upto 40-60%
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 System Clock Generation (SCG) specifications

6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 19. Fast internal RC Oscillator electrical specifications

Symbol	Parameter ¹	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	% F_{FIRC}
ΔF_{125}	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	% F_{FIRC}
$T_{Startup}$	Startup time		3.4	5	μs ²
T_{JIT} ³	Cycle-to-Cycle jitter	—	300	500	ps
T_{JIT} ³	Long term jitter over 1000 cycles	—	0.04	0.1	% F_{FIRC}

1. With FIRC regulator enable

2. Startup time is defined as the time between clock enablement and clock availability for system use.

3. FIRC as system clock

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 20. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	—	±3	% F_{SIRC}
ΔF_{125}	Frequency deviation across process, voltage, and temperature < 125°C	—	—	±3.3	% F_{SIRC}
$T_{Startup}$	Startup time	—	9	12.5	μs ¹

1. Startup time is defined as the time between clock enablement and clock availability for system use.

Table 23. Flash command timing specifications for S32K14x (continued)

Symbol	Description ¹		S32K142		S32K144		S32K146		S32K148		Unit Notes	
			Typ	Max	Typ	Max	Typ	Max	Typ	Max		
	setting (32-bit write complete, ready for next 32-bit write)	Last (Nth) 32-bit write (time for write only, not cleanup)	200	550	200	550	200	550	200	550		
$t_{\text{quickwrClnup}}$	Quick Write Cleanup execution time	—	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	—	(# of Quick Writes) * 2.0	ms	7

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 μ s, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

Table 24. Flash command timing specifications for S32K11x

Symbol	Description ¹		S32K116		S32K118		Unit Notes	
			Typ	Max	Typ	Max		
t_{rd1blk}	Read 1 Block execution time	32 KB flash	—	0.36	—	0.36	ms	
		64 KB flash	—	—	—	—		
		128 KB flash	—	1.2	—	—		
		256 KB flash	—	—	—	2		
		512 KB flash	—	—	—	—		
t_{rd1sec}	Read 1 Section execution time	2 KB flash	—	75	—	75	μ s	
		4 KB flash	—	100	—	100		
t_{pgmchk}	Program Check execution time	—	—	100	—	100	μ s	
t_{pgm8}	Program Phrase execution time	—	90	225	90	225	μ s	
t_{ersblk}	Erase Flash Block execution time	32 KB flash	15	300	15	300	ms	2
		64 KB flash	—	—	—	—		
		128 KB flash	120	1100	—	—		
		256 KB flash	—	—	250	2125		
		512 KB flash	—	—	—	—		

Table continues on the next page...

Table 24. Flash command timing specifications for S32K11x (continued)

Symbol	Description ¹		S32K116		S32K118		Unit		Notes
			Typ	Max	Typ	Max			
t _{ersscr}	Erase Flash Sector execution time	—	12	130	12	130	ms		2
t _{pgmsec1k}	Program Section execution time (1 KB flash)	—	5	—	5	—	ms		
t _{rd1all}	Read 1s All Block execution time	—	—	1.7	—	2.8	ms		
t _{rdonce}	Read Once execution time	—	—	30	—	30	μs		
t _{pgmonce}	Program Once execution time	—	90	—	90	—	μs		
t _{ersall}	Erase All Blocks execution time	—	150	1500	230	2500	ms		2
t _{vfykey}	Verify Backdoor Access Key execution time	—	—	35	—	35	μs		
t _{ersallu}	Erase All Blocks Unsecure execution time	—	150	1500	230	2500	ms		2
t _{pgmpart}	Program Partition for EEPROM execution time	32 KB EEPROM backup	71	—	71	—	ms		3
		64 KB EEPROM backup	—	—	—	—			
t _{setram}	Set FlexRAM Function execution time	Control Code 0xFF	0.08	—	0.08	—	ms		3
		32 KB EEPROM backup	0.8	1.2	0.8	1.2			
		48 KB EEPROM backup	—	—	—	—			
		64 KB EEPROM backup	—	—	—	—			
t _{eevr8b}	Byte write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	μs		3-4
		48 KB EEPROM backup	—	—	—	—			
		64 KB EEPROM backup	—	—	—	—			
t _{eevr16b}	16-bit write to FlexRAM execution time	32 KB EEPROM backup	385	1700	385	1700	μs		3-4
		48 KB EEPROM backup	—	—	—	—			
		64 KB EEPROM backup	—	—	—	—			
t _{eevr32bers}	32-bit write to erased FlexRAM location execution time	—	360	2000	360	2000	μs		

Table continues on the next page...

Table 26. QuadSPI electrical specifications

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN ¹						HSRUN ¹						RUN/HSRUN ²			
QuadSPI Mode			SDR						SDR						SDR		DDR ³	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		External DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Register Settings																		
MCR[DDR_EN]		-	0		0		0		0		0		0		0		1	
MCR[DQS_EN]		-	0		1		1		0		1		1		0		1	
MCR[SCLKCFG[0]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[1]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[2]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[3]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[5]]		-	0		0		0		0		0		0		0		1	
SMPR[FSPHS]		-	0		1		0		0		1		0		0		0	
SMPR[FSDLY]		-	0		0		0		0		0		0		0		0	
SOCCR [SOCCFG[7:0]]			-		0		23		-		0		30		-		-	
SOCCR[SOCCFG[15:8]]		-	-		-		-		-		-		-		-		30	
FLSHCR[TDH]		-	0x00		0x00		0x00		0x00		0x00		0x00		0x00		0x01	
Timing Parameters																		
SCK Clock Frequency	f _{SCK}	MHz	-	38	-	64	-	48	-	40	-	80	-	50	-	20	-	20 ⁴
SCK Clock Period	t _{SCK}	ns	1/f _{SCK}	-	1/f _{SCK}	-	1/f _{SCK}	-	1/f _{SCK}	-	1/f _{SCK}	-	1/f _{SCK}	-	50.0	-	50.0 ⁴	-

Table continues on the next page...

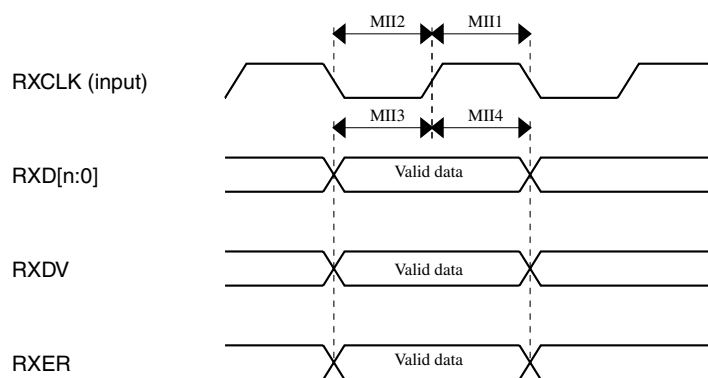


Figure 24. MII receive diagram

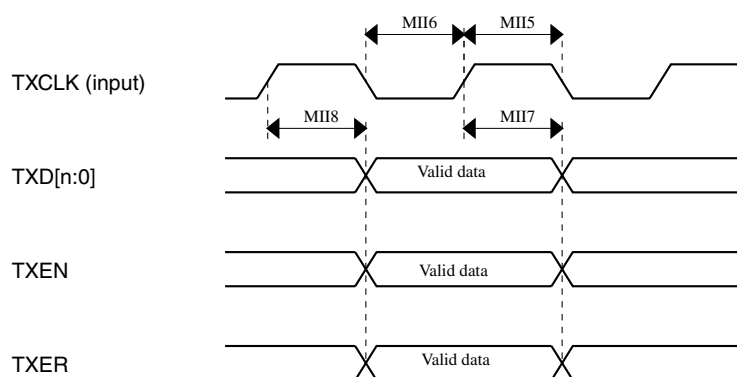


Figure 25. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

**Table 36. RMI signal switching specifications
(continued)**

Symbol	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	2	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

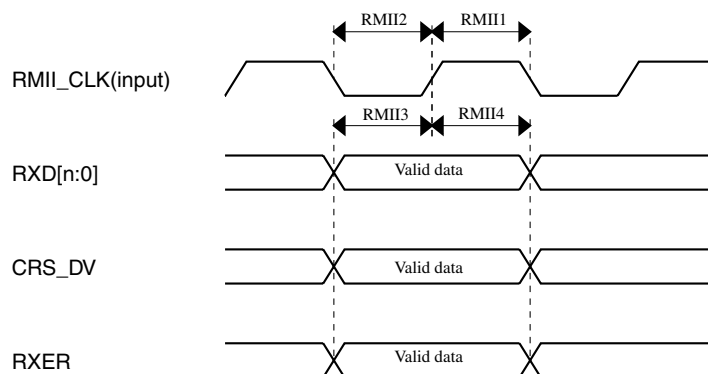


Figure 26. RMI receive diagram

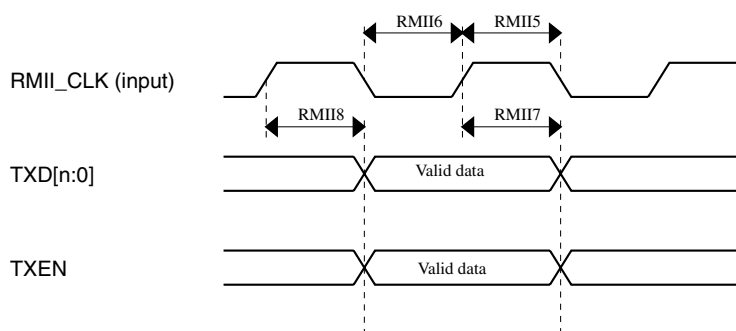


Figure 27. RMI transmit diagram

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- MDIO pin must have external Pull-up.

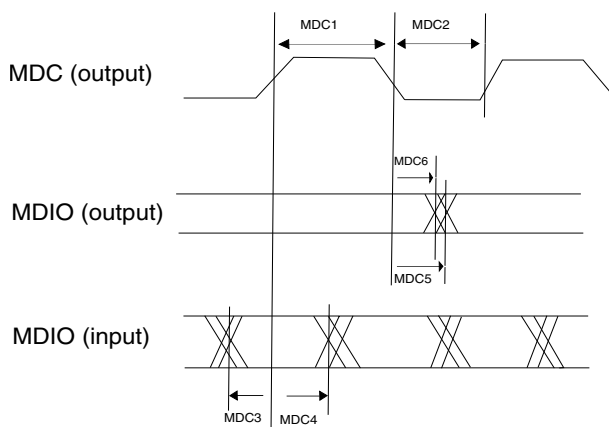
Table 37. MDIO timing specifications

Symbol	Description	Min.	Max.	Unit
—	MDC Clock Frequency	—	2.5	MHz

Table continues on the next page...

Table 37. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

**Figure 28. MII/RMII serial management channel timing diagram**

6.5.7 Clockout frequency

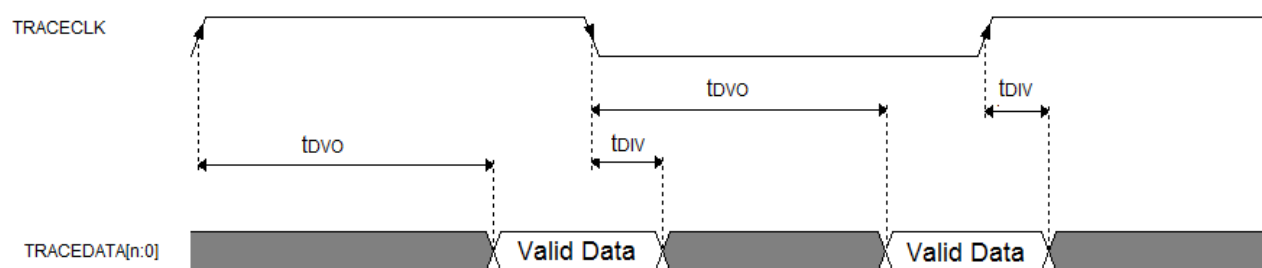
Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specifications

Table 39. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

**Figure 31. TRACE CLKOUT specifications**

6.6.3 JTAG electrical specifications

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 43. Revision History

Rev. No.	Date	Substantial Changes
1	12 Aug 2016	Initial release
2	03 March 2017	- Updated description of QSPI and Clock interfaces in Key Features section - Updated figure: High-level architecture diagram for the S32K1xx family - Updated figure: S32K1xx product series comparison - Added note in section Selecting orderable part number - Updated figure: Ordering information - In table: Absolute maximum ratings : - Added footnote to I_{INJPAD_DC} - Updated min and max value of I_{INJPAD_DC} - Updated description, max and min values for I_{INJSUM} - Updated $V_{IN_TRANSIENT}$ - In table: Voltage and current operating requirements : - Renamed V_{SUP_OFF} - Updated max value of V_{DD_OFF} - Removed V_{INA} and V_{IN} - Added V_{REFH} and V_{REFL} - Updated footnote "Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V ..." - Removed I_{NJSUM_AF} - Updated footnotes in table Table 4 - Updated section Power mode transition operating behaviors - In table: Power consumption - Added footnote "With PMC_REGSC[CLKBIASDIS] ..." - Updated conditions for VLPR - Removed I_{dd}/MHz for S32K144 - Updated numbers for S32K142 and S32K148 - Removed use case footnotes - In section Modes configuration : - Replaced table "Modes configuration" with spreadsheet attachment: 'S32K1xx_Power_Modes_Master_configuration_sheet' - In table: DC electrical specifications at 3.3 V Range : - Added footnotes to V_{ih} Input Buffer High Voltage and V_{ih} Input Buffer Low Voltage - Added footnote to High drive port pins - In table: DC electrical specifications at 5.0 V Range :

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes
		- Added footnotes V_{ih} Input Buffer High Voltage and V_{il} Input Buffer Low Voltage - Updated table: AC electrical specifications at 3.3 V range - Updated table: AC electrical specifications at 5 V range - In table: Standard input pin capacitance - Added footnote to Normal run mode (S32K14x series) - Removed note from 1M ohms Feedback Resistor in figure Oscillator connections scheme - In table: External System Oscillator electrical specifications - Updated typical of I_{DDOSC} Supply current — low-gain mode (low-power mode) (HGO=0) 1 for 4 and 8 MHz - Removed rows for I_{lk_ext} EXTAL/XTAL impedance High-frequency, low-gain mode (low-power mode) and high-frequency, high-gain mode and V_{EXTAL} - Updated Typ. of R_S low-gain mode - Updated description of R_F, R_S, and V_{PP} - Removed footnote from R_F Feedback resistor - Updated footnote for C_1 C_2 and R_F - In table: Table 18 - Removed mention of high-frequency - Added HGO 0, 1 information - In table: Fast internal RC Oscillator electrical specifications - Updated F_{FIRC} - Updated description of ΔF - Updated typ and max values of T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles - Added footnotes to T_{JIT} cycle-to-cycle jitter and T_{JIT} Long term jitter over 1000 cycles - Updated naming convention of I_{DDFIRC} Supply current - Added footnote to I_{DDFIRC} Supply current - Added footnote to column Parameter - In table: Slow internal RC oscillator (SIRC) electrical specifications - Removed V_{DD} Supply current in 2 MHz Mode - Removed footnote and updated description of ΔF - Updated footnote to F_{SIRC} and I_{DDSIRC} - In table: SPLL electrical specifications - Added row for F_{SPLL_REF} PLL Reference - Updated naming convention throughout the table - Updated the max value of T_{SPLL_LOCK} Lock detector detection time - In table: Flash timing specifications — commands - Added footnotes: - All command times assumes ... - For all EEPROM Emulation terms ... 'First time' EERAM writes after a POR ... - Removed footnote 'Assumes 25 MHz or ...' - Updated Max of $t_{ewr32bers}$ - Added parameters $t_{quickwr}$ and $t_{quickwrCinup}$ - In table: Reliability specifications - Removed Typ. values for all parameters - Removed footnote 'Typical values represent ...' - Added footnote 'Any other EEE driver usage ...' - Updated QuadSPI AC specifications - Removed topic: Reliability, Safety and Security modules - In table: 12-bit ADC operating conditions - Updated V_{DDA}

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated values for V_{REFH} and V_{REFL} to add reference to the section "voltage and current operating requirements" for Min and Max values - Updated footnote to Typ. - Removed footnote from RAS Analog source resistance - Updated figure: ADC input impedance equivalency diagram - In table: 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Removed rows for V_{TEMP_S} and V_{TEMP25} - Updated footnote to Typ. - In table: 12-bit ADC characteristics (3 V to 5.5 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Removed rows for V_{TEMP_S} and V_{TEMP25} - Removed number for TUE - Updated footnote to Typ. - In table: Comparator with 8-bit DAC electrical specifications - Updated Typ. of I_{DDL5} Supply current, Low-speed mode - Updated Typ. of t_{DLSB} Propagation delay, Low-speed mode - Updated Typ. of t_{DHSS} Propagation delay, High-speed mode - Updated t_{DLSS} Propagation delay - Added row for t_{DDAC} Initialization and switching settling time - Updated footnote - Updated section LPSPi electrical specifications - Added section: SAI electrical specifications - Updated section: Ethernet AC specifications - Added section: Clockout frequency - Added section: Trace electrical specifications - Updated table: Table 41 : Updated numbers for S32K142 and S32K148 - Updated table: Table 42 : Updated numbers for S32K148 - Updated Document number for 32-pin QFN in topic Obtaining package dimensions
3	14 March 2017	- In Table 2 - Updated min. value of V_{DD_OFF} - Added parameter I_{INJSUM_AF} - Updated Power mode transition operating behaviors - Updated Power consumption - Updated footnote to T_{SPLL_LOCK} in SPLL electrical specifications - In 12-bit ADC electrical characteristics - Updated table: 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Added typ. value to I_{DDA_ADC}, TUE, DNL, and INL - Added min. value to SMPLTS - Removed footnote 'All the parameters in this table ... ' - Updated table: 12-bit ADC characteristics (3 V to 5.5 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$) - Added typ. value to I_{DDA_ADC} - Removed footnote 'All the parameters in this table ... ' - In Flash timing specifications — commands updated Max. value of t_{Vfykey} to 33 μs
4	02 June 2017	- In section: Block diagram, added block diagram for S32K11x series. - Updated figure: S32K1xx product series comparison. - In section: Selecting orderable part number , added reference to attachment S32K_Part_Numbers.xlsx. - In section: Ordering information - Updated figure: Ordering information. - In Table 1,

Table continues on the next page...

Table 43. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated note 'All the limits defined ...' - Updated parameter 'I_{INJPAD_DC_ABS}', 'V_{IN_DC}', I_{INJSUM_DC_ABS}. - In Table 2, - Updated parameter I_{INJPAD_DC_OP} and I_{INJSUM_DC_OP}. - In Table 5, updated TBDs for V_{LVR_HYST}, V_{LVD_HYST}, and V_{LVW_HYST} - In Power mode transition operating behaviors, - Added VLPR → VLPS - Added VLPS → VLPR - Updated TBDs for VLPS → Asynchronous DMA Wakeup, STOP1 → Asynchronous DMA Wakeup, and STOP2 → Asynchronous DMA Wakeup - In Table 7, updated the specifications for S32K144. - Updated the attachment <i>S32K1xx_Power_Modes_Configuration.xlsx</i>. - In Table 15, removed C_{IN_A}. - In Table 17, - Updated specificatins for g_{mXOSC}. - Removed I_{DDOSC} - In Table 19, - Added parameter ΔF125. - Removed I_{DDFIRC} - In Table 20, - Added parameter ΔF125. - Removed I_{DDSIRC} - In Table 21, removed I_{LPO} - Updated section: Flash memory module (FTFC) electrical specifications - In section: 12-bit ADC operating conditions, - Updated TBDs for I_{DDA_ADC} and TUE in Table 28 - Updated TBDs for I_{DDA_ADC} and TUE in Table 29 - In section: QuadSPI AC specifications, updated figure 'QuadSPI output timing (HyperRAM mode) diagram'. - In section: 12-bit ADC operating conditions, updated Table 27. - In section: CMP with 8-bit DAC electrical specifications, added note 'For comparator IN signals adjacent ...' - In table: Table 32, minor update in footnote 6. - In table: Table 41, updated specifications for S32K146.
5	06 Dec 2017	- Removed S32K148 from 'Caution' - Updated figure: S32K1xx product series comparison for 'EEPROM emulated by FlexRAM' of S32K148 (Added content to footnote) - Added support for LIN protocol version 2.2 A - In Absolute maximum ratings : - Added note 'Unless otherwise ...' - Added parameter 'Added note 'T_{ramp_MCU}' - Updated footnote for 'T_{ramp}' - In Voltage and current operating requirements : - Added footnote 'V_{DD} and V_{DDA} must be shorted ...' against parameter 'V_{DD}—V_{DDA}' - Updated footnote 'V_{DD} and V_{DDA} must be shorted ...' - In Power and ground pins - Added diagrams for 32-QFN and 48-LQFP and footnote below the diagrams. - Updated footnote 'V_{DD} and V_{DDA} must be shorted ...' - In Power mode transition operating behaviors :

Table continues on the next page...

Table 43. Revision History

Rev. No.	Date	Substantial Changes
		- Updated specs for T_{JIT} Cycle-to-Cycle jitter to 300 ps - In QuadSPI AC specifications : - Updated specs for T_{iv} Data Output In-Valid Time - In figure 'QuadSPI output timing (SDR mode) diagram', marked Invalid area - In CMP with 8-bit DAC electrical specifications : - Removed '(VAIO)' from decription of V_{HYST0} - In LPSPi electrical specifications : - Added note 'Undefined' in figures 'LPSPi slave mode timing (CPHA = 0)' and 'LPSPi slave mode timing (CPHA = 1)'