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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	352-BBGA
Supplier Device Package	352-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9315-cbz

Processor Core - ARM920T

The ARM920T is a Harvard architecture processor with separate 16-kbyte instruction and data caches with an 8-word line length but a unified memory. The processor utilizes a five-stage pipeline consisting of fetch, decode, execute, memory, and write stages. Key features include:

- ARM (32-bit) and Thumb (16-bit compressed) Instruction Sets
- 32-bit Advanced Micro-Controller Bus Architecture (AMBA)
- 16-kbyte Instruction Cache with Lockdown
- 16-kbyte Data Cache (programmable write-through or write-back) with Lockdown
- MMU for Linux®, Microsoft® Windows® CE and Other Operating Systems
- Translation Look Aside Buffers with 64 Data and 64 Instruction Entries
- Programmable Page Sizes of 1 Mbyte, 64 kbyte, 4 kbyte, and 1 kbyte
- Independent Lockdown of TLB Entries

MaverickCrunch™ Math Engine

The MaverickCrunch Engine is a mixed-mode coprocessor designed primarily to accelerate the math processing required to rapidly encode digital audio formats. It accelerates single and double precision integer and floating point operations plus an integer multiply-accumulate (MAC) instruction that is considerably faster than the ARM920T's native MAC instruction. The ARM920T coprocessor interface is utilized thereby sharing its memory interface and instruction stream. Hardware forwarding and interlock allows the ARM to handle looping and addressing while MaverickCrunch handles computation. Features include:

- IEEE-754 single and double precision floating point
- 32 / 64-bit integer
- Add / multiply / compare
- Integer MAC 32-bit input with 72-bit accumulate
- Integer Shifts
- Floating point to/from integer conversion
- Sixteen 64-bit register files
- Four 72-bit accumulators

MaverickKey™ Unique ID

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

Both a specific 32-bit ID as well as a 128-bit random ID is programmed into the EP9315 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device the EP9315 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by also matching device IDs to server IDs. MaverickKey IDs provide a level of hardware security required for today's Internet appliances.

General Purpose Memory Interface (SDRAM, SRAM, ROM, FLASH)

The EP9315 features a unified memory address model where all memory devices are accessed over a common address/data bus. A separate internal port is dedicated to the read-only Raster/LCD refresh engine, while the rest of the memory accesses are performed via the Processor bus. The SRAM memory controller supports 8, 16 and 32-bit devices and accommodates an internal boot ROM concurrently with 32-bit SDRAM memory.

- 1-4 banks of 32-bit 66 or 100 MHz SDRAM
- One internal port dedicated to the Raster/LCD Refresh Engine (Read Only)
- Address and data bus shared between SDRAM, SRAM, ROM, and FLASH memory
- NOR FLASH memory supported

Table B. General Purpose Memory Interface Pin Assignments

Pin Mnemonic	Pin Description
SDCLK	SDRAM Clock
SDCLKEN	SDRAM Clock Enable
SDCSn[3:0]	SDRAM Chip Selects 3-0
RASn	SDRAM RAS
CASn	SDRAM CAS
SDWEn	SDRAM Write Enable
CSn[7:6] and CSn[3:0]	Chip Selects 7, 6, 3, 2, 1, 0
AD[25:0]	Address Bus 25-0
DA[31:0]	Data Bus 31-0
DQMn[3:0]	SDRAM Output Enables / Data Masks
WRn	SRAM Write Strobe
RDn	SRAM Read / OE Strobe
WAITn	SRAM Wait Input

- Timing and interface signals for digital LCD and TFT displays
- Full programmability for either non-interlaced or dual-scan color and grayscale flat panel displays
- Dedicated data path to SDRAM controller for improved system performance
- Pixel depths of 4, 8, 16, or 24 bits per pixel or 256 levels of grayscale
- Hardware Cursor up to 64 x 64 pixels
- 256 x 18 Color Lookup Table
- Hardware Blinking
- 8-bit interface to low-end panel

Table F. LCD Interface Pin Assignments

Pin Mnemonic	Pin Description
SPCLK	Pixel Clock
P[17:0]	Pixel Data Bus [17:0]
HSYNC / LP	Horizontal Synchronization / Line Pulse
VCSYNC / FP	Vertical or Composite Synchronization / Frame Pulse
BLANK	Composite Blank
BRIGHT	Pulse Width Modulated Brightness

Graphics Accelerator

The EP9315 contains a hardware graphics acceleration engine that improves graphic performance by handling block copy, block fill and hardware line draw operations. The Graphics Accelerator is used in the system to off-load graphics operations from the processor.

Pixel depths supported by the Graphics Accelerator are 4, 8, 16, or 24 bits per pixel. The 24 bits per pixel mode can be operated as packed (4 pixels every 3 words) or unpacked (1 pixel per word with the high byte unused.)

The block copy operations of the Graphics Accelerator are similar to a DMA (Direct Memory Access) transfer that understands pixel organization, block width, transparency, and transformation from 1bpp to higher 4, 8, 16, or 24bpp.

The line draw operations also allow for solid lines or dashed lines. The colors for line drawing can be either foreground color and background color or foreground color with the background being transparent.

Touch Screen Interface with 12-bit Analog-to-digital Converter (ADC)

The touch screen interface performs all sampling, averaging, ADC range checking, and control for a wide variety of analog resistive touch screens. This controller only interrupts the processor when a meaningful change occurs. The touch screen hardware may be disabled and the switch matrix and ADC controlled directly if desired. Features include:

- Support for 4-, 5-, 7-, or 8-wire analog resistive touch screens.
- Flexibility - unused lines may be used for temperature sensing or other functions.
- Touch screen interrupt function.

Table G. Touch Screen Interface with 12-bit Analog-to-Digital Converter Pin Assignments

Pin Mnemonic	Pin Description
Xp, Xm	Touch screen ADC X Axis
Yp, Ym	Touch screen ADC Y Axis
SXp, SXm	Touch screen ADC X Axis Voltage Feedback
SYp, SYm	Touch screen ADC Y Axis Voltage Feedback

64-Key Keypad Interface

The keypad circuitry scans an 8 x 8 array of 64 normally open, single-pole switches. Any one or two keys depressed will be de-bounced and decoded. An interrupt is generated whenever a stable set of depressed keys is detected. If the keypad is not utilized, the 16 column/row pins may be used as general purpose I/O. The Keypad interface:

- Provides scanning, debounce, and decoding for a 64-key switch array.
- Scans an 8-row by 8-column matrix.
- May decode 2 keys at once.
- Generates an interrupt when a new stable key is determined.
- Also generates a 3-key reset interrupt.

Table H. 64-Key Keypad Interface Pin Assignments

Pin Mnemonic	Pin Description	Alternative Usage
COL[7:0]	Key Matrix Column Inputs	General Purpose I/O
ROW[7:0]	Key Matrix Row Inputs	General Purpose I/O

Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	- - - -	3.96 2.16 2.16 3.96	V V V V
Total Power Dissipation	(Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)			-	±10	mA
Output current per pin, DC			-	±50	mA
Digital Input voltage	(Note 2)		-0.3	RVDD+0.3	V
Storage temperature			-40	+125	°C

Note: 1. Includes all power generated due to AC and/or DC output loading.
2. The power supply pins are at recommended maximum values.

Caution: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	3.0 1.71 1.71 3.0	3.3 1.80 1.80 3.3	3.6 1.94 1.94 3.6	V V V V
Operating Ambient Temperature - Commercial	(Note 3)	T_A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	(Note 4)	T_A	-40	+25	+85	°C
Processor Clock Speed - Commercial		FCLK	-	-	200	MHz
Processor Clock Speed - Industrial		FCLK	-	-	184	MHz
System Clock Speed - Commercial		HCLK	-	-	100	MHz
System Clock Speed - Industrial		HCLK	-	-	92	MHz

Note: 3. The device is capable of operating up to 70° C ambient under typical operating conditions with power consumption less than 1.5W.
4. The device is capable of operating up to 85° C ambient under typical operating conditions with power consumption less than 1.5W.

DC Characteristics

(T_A = 0 to 70° C; CVDD = VDD_PLL = 1.8; RVDD = 3.3 V;
All grounds = 0 V; all voltages with respect to 0 V unless otherwise noted)

Parameter			Symbol	Min	Max	Unit
High level output voltage	Iout = -4 mA	(Note 5)	V_{oh}	0.85 × RVDD	-	V
Low level output voltage	Iout = 4 mA		V_{ol}	-	0.15 × RVDD	V
High level input voltage		(Note 6)	V_{ih}	0.65 × RVDD	VDD + 0.3	V
Low level input voltage		(Note 6)	V_{il}	-0.3	0.35 × RVDD	V
High level leakage current	Vin = 3.3 V	(Note 6)	I_{ih}	-	10	µA
Low level leakage current	Vin = 0	(Note 6)	I_{il}	-	-10	µA

Parameter		Min	Typ	Max	Unit
Power Supply Pins (Outputs Unloaded), 25° C					
Power Supply Current:	CVDD / VDD_PLL Total RVDD	- -	190 45	240 80	mA mA
Low-Power Mode Supply Current	CVDD / VDD_PLL Total RVDD	- -	2 1	3.5 2	mA mA

Note: 5. For open drain pins, high level output voltage is dependent on the external load.
6. All inputs that do not include internal pull-ups or pull-downs, must be externally driven for proper operation (See Table S on page 60). If an input is not driven, it should be tied to power or ground, depending on the particular function. If an I/O pin is not driven and programmed as an input, it should be tied to power or ground through its own resistor.

SDRAM Burst Write Cycle

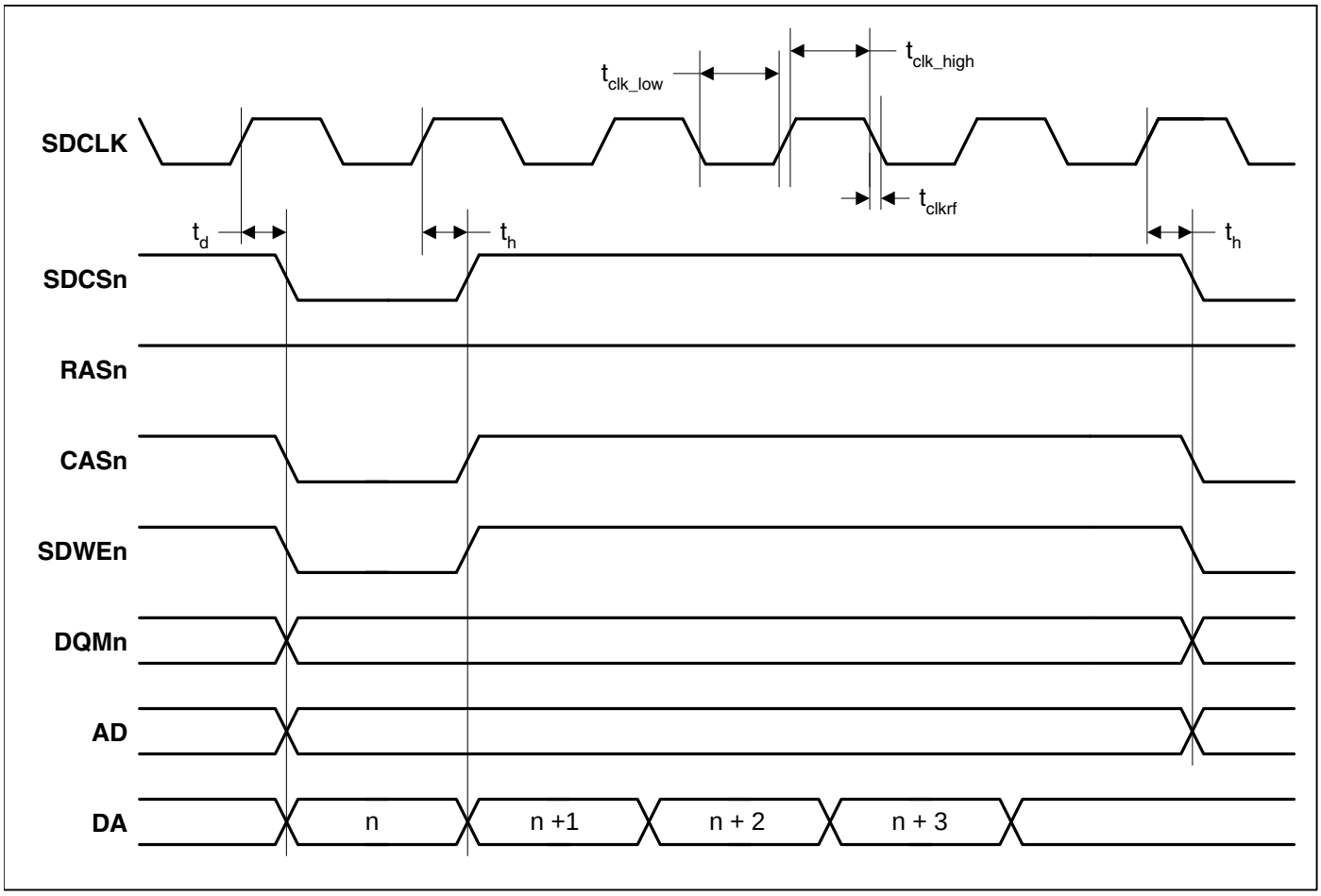


Figure 4. SDRAM Burst Write Cycle Timing Measurement

Static Memory Single Word Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	0	-	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpw}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to RDn deassert time	t_{DAs}	$t_{HCLK} + 12$	-	-	ns
DA hold from RDn deassert time	t_{DAh}	0	-	-	ns

See “Timing Conditions” on page 14 for definition of HCLK.

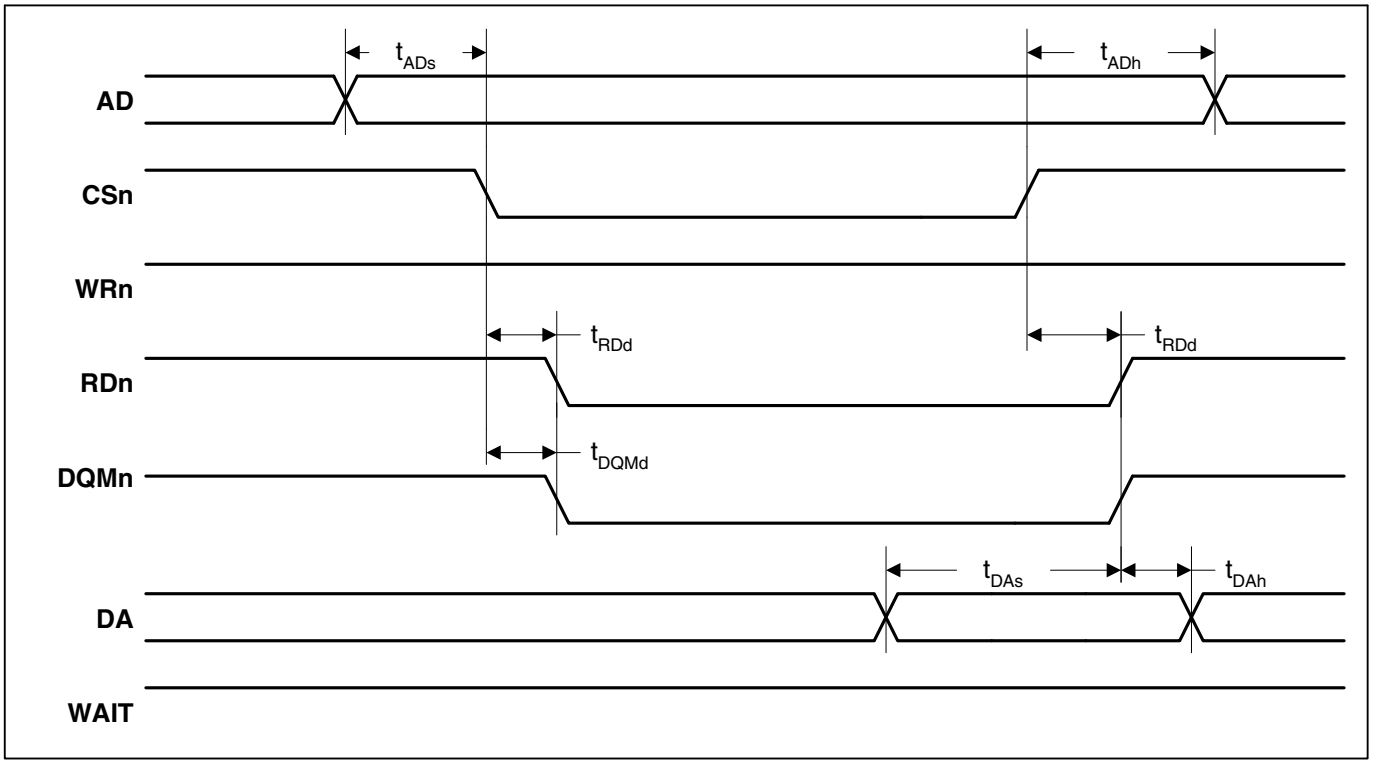


Figure 6. Static Memory Single Word Read Cycle Timing Measurement

Static Memory 32-bit Write on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	-	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh1}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

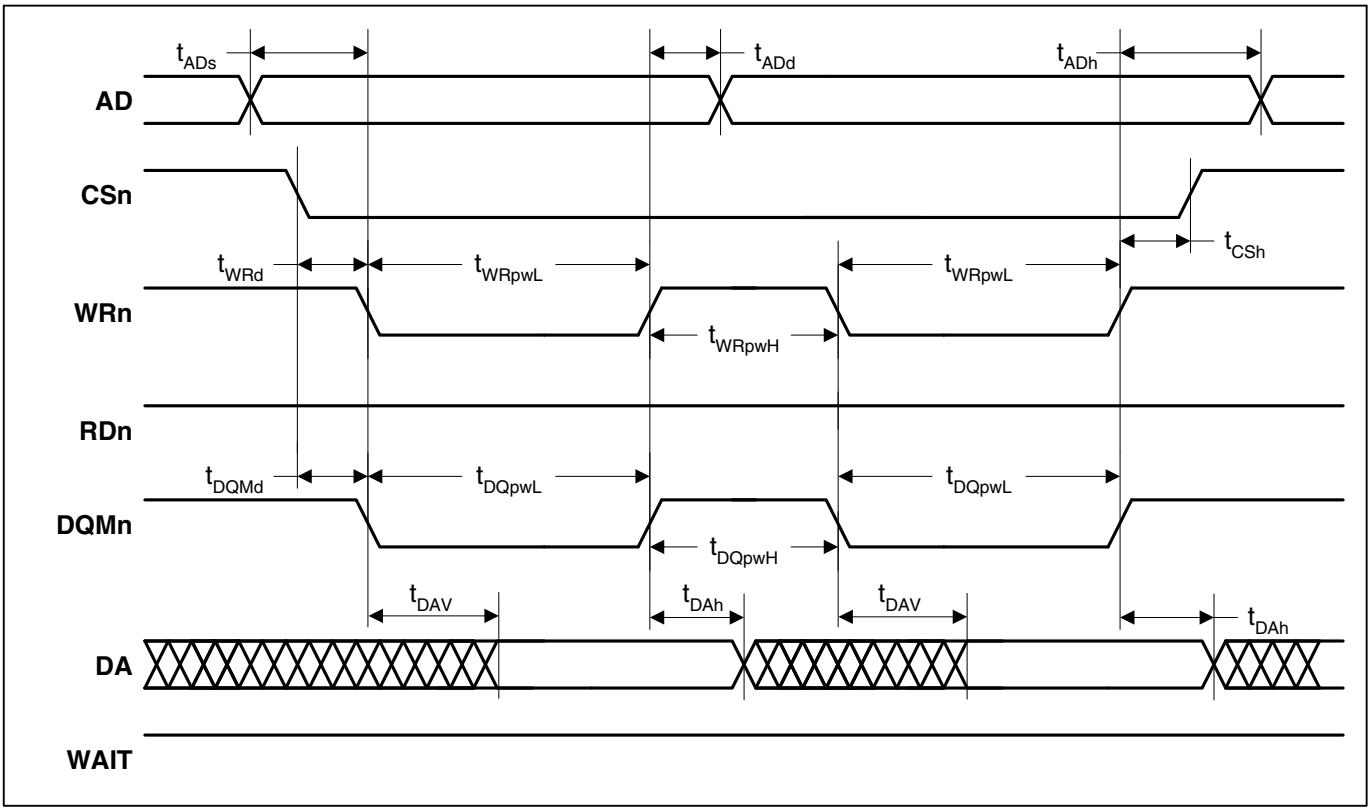


Figure 11. Static Memory Multiple Word Write 16-bit Cycle Timing Measurement

PCMCIA Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to signal transition time	t_{ADs}	0	-	-	ns
MCDIR hold time	t_{MCDh}	0	-	-	ns
MCEHn/MCELn/MCREGn hold time	t_{MCEh}	0	-	-	ns
DATA invalid delay time	t_{DAfo}	0	-	-	ns
Wait Time[1]	t_W	-	-	t_A-[2 × t_{HCLK}]	ns
Attribute Mode Timing					
Attribute access time	t_A	[(AA + 1) × t_{HCLK}] - 14	(AA + 1) × t_{HCLK}	-	ns
Attribute hold time	t_H	[(HA + 1) × t_{HCLK}] - 3	(HA + 1) × t_{HCLK}	-	ns
Attribute space pre-charge delay time	t_p	(PA + 1) × t_{HCLK}	(PA + 1) × t_{HCLK}	-	ns
Common Mode Timing					
Common access time	t_A	[(AC + 1) × t_{HCLK}] - 14	(AC + 1) × t_{HCLK}	-	ns
Common hold time	t_H	[(HC + 1) × t_{HCLK}] - 3	(HC + 1) × t_{HCLK}	-	ns
Common space pre-charge delay time	t_p	(PC + 1) × t_{HCLK}	(PC + 1) × t_{HCLK}	-	ns
I/O Mode Timing					
I/O access time	t_A	[(AI + 1) × t_{HCLK}] - 14	(AI + 1) × t_{HCLK}	-	ns
I/O hold time	t_H	[(HI + 1) × t_{HCLK}] - 3	(HI + 1) × t_{HCLK}	-	ns
I/O space pre-charge delay time	t_p	(PI + 1) × t_{HCLK}	(PI + 1) × t_{HCLK}	-	ns

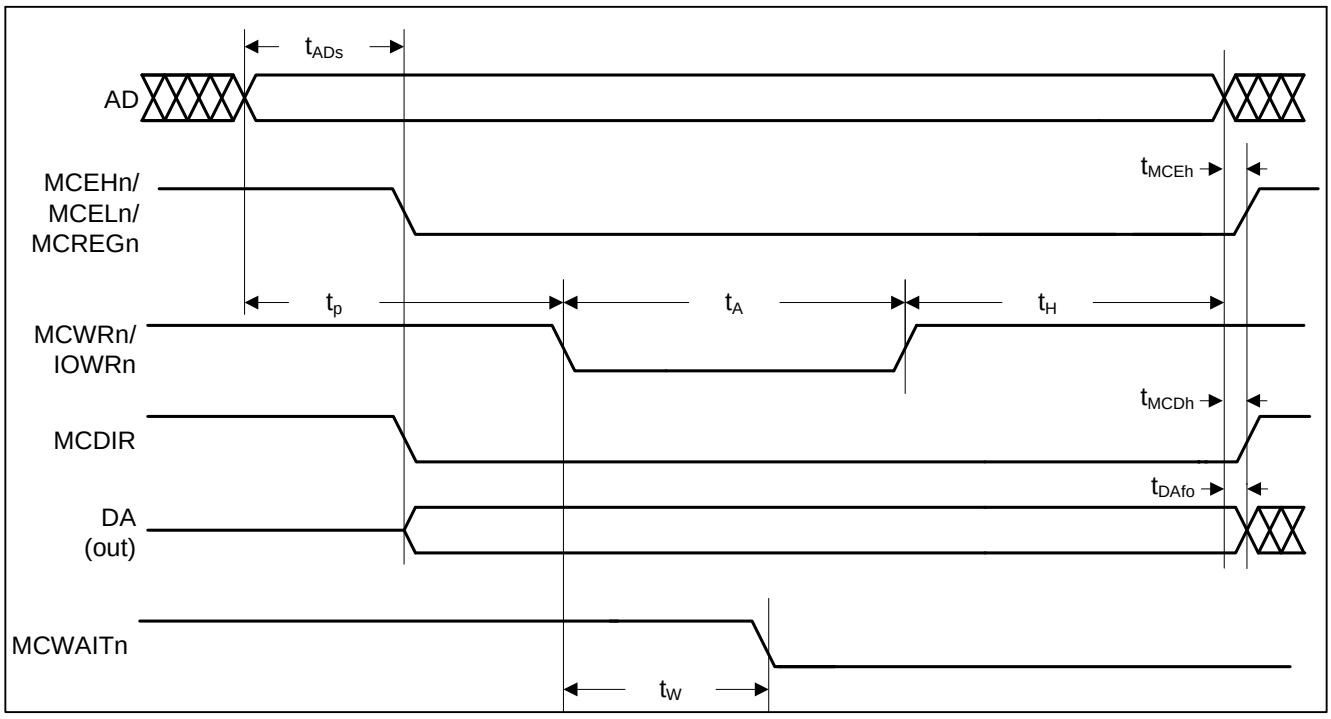


Figure 18. PCMCIA Write Cycle Timing Measurement

Note: MCWAITn asserted will extend the MCWR / IOWR strobe time.

IDE Interface

Register Transfers

Parameter			Symbol	Mode 0 (in ns)	Mode 1 (in ns)	Mode 2 (in ns)	Mode 3 (in ns)	Mode 4 (in ns)
Cycle time	(min)	(Notes 1, 4, 5)	t_0	600	383	330	180	120
Address valid to DIORn / DIOWn setup	(min)	(Note 4)	t_1	70	50	30	30	25
DIORn / DIOWn pulse width 8-bit	(min)	(Note 1, 4)	t_2	290	290	290	80	70
DIORn / DIOWn recovery time	(min)	(Note 1, 4)	t_{2i}	-	-	-	70	25
DIOWn data setup	(min)	(Note 4)	t_3	60	45	30	30	20
DIOWn data hold	(min)		t_4	0	0	0	0	0
DIORn data setup	(min)		t_5	20	20	20	20	20
DIORn data hold	(min)		t_6	0	0	0	0	0
DIORn data high impedance state	(max)	(Note 2, 4)	t_{6z}	30	30	30	30	30
DIORn / DIOWn to address valid hold	(min)	(Note 4)	t_9	20	15	10	10	10
Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	(Note 4)	t_{RD}	0	0	0	0	0
IORDY Setup time		(Note 3, 4)	t_A	35	35	35	35	35
IORDY Pulse Width	(max)	(Note 4)	t_B	1250	1250	1250	1250	1250
IORDY assertion to release	(max)		t_C	5	5	5	5	5
DIOWn assert to data valid	(max)		t_{DDV}	10	10	10	10	10

Note: 1. t_0 is the minimum total cycle time, t_2 is the minimum DIORn / DIOWn assertion time, and t_{2i} is the minimum DIORn / DIOWn negation time. A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2. This parameter specifies the time from the negation edge of DIORn to the time that the data bus is released by the device.

3. The delay from the activation of DIORn or DIOWn until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIORn or DIOWn, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIORn or DIOWn, then t_{RD} shall be met and t_5 is not applicable.

4. Timings based upon software control. See User's Guide.

5. ATA / ATAPI standards prior to ATA / ATAPI-5 inadvertently specified an incorrect value for mode 2 time t_0 by utilizing the 16-bit PIO value.

6. All IDE timing is based upon HCLK = 100 MHz.

PIO Data Transfers

Parameter			Symbol	Mode 0 (in ns)	Mode 1 (in ns)	Mode 2 (in ns)	Mode 3 (in ns)	Mode 4 (in ns)
Cycle time	(min)	(Note 1, 4)	t_0	600	383	240	180	120
Address valid to DIORn / DIOWn setup	(min)	(Note 4)	t_1	70	50	30	30	25
DIORn / DIOWn 16-bit	(min)	(Note 1, 4)	t_2	165	125	100	80	70
DIORn / DIOWn recovery time	(min)	(Note 1, 4)	t_{2i}	-	-	-	70	25
DIOWn data setup	(min)	(Note 4)	t_3	60	45	30	30	20
DIOWn data hold	(min)		t_4	0	0	0	0	0
DIORn data setup	(min)		t_5	20	20	20	20	20
DIORn data hold	(min)		t_6	0	0	0	0	0
DIORn data high impedance state	(max)	(Note 2, 4)	t_{6z}	30	30	30	30	30
DIORn / DIOWn to address valid hold	(min)	(Note 4)	t_9	20	15	10	10	10
Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	(Note 4)	t_{RD}	0	0	0	0	0
IORDY Setup time		(Note 3, 4)	t_A	35	35	35	35	35
IORDY Pulse Width	(max)	(Note 4)	t_B	1250	1250	1250	1250	1250
IORDY assertion to release	(max)		t_C	5	5	5	5	5
DIOWn assert to data valid	(max)		t_{DDV}	10	10	10	10	10

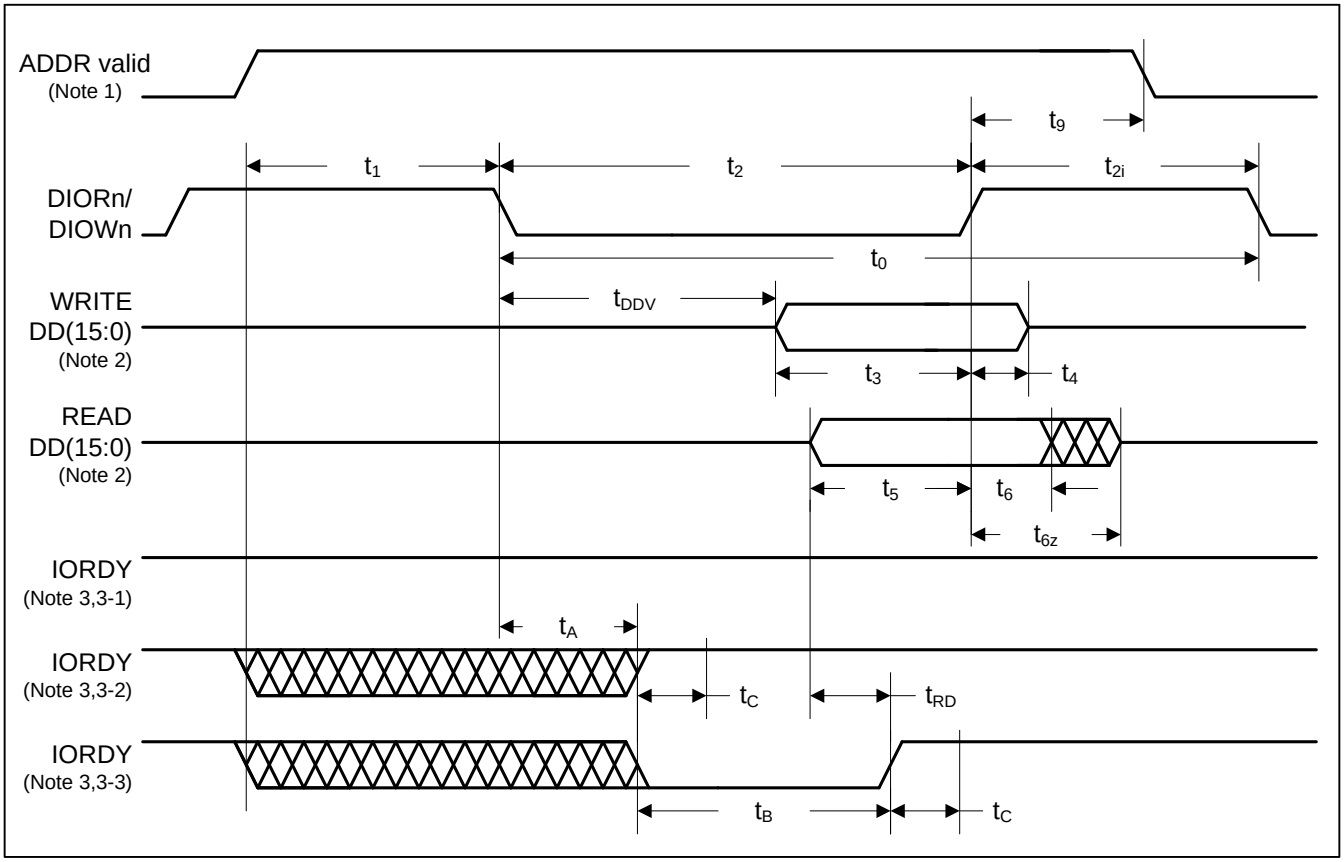
Note: 1. t_0 is the minimum total cycle time, t_2 is the minimum DIORn / DIOWn assertion time, and t_{2i} is the minimum DIORn / DIOWn negation time. A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2. This parameter specifies the time from the negation edge of DIORn to the time that the data bus is released by the device.

3. The delay from the activation of DIORn or DIOWn until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIORn or DIOWn, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIORn or DIOWn, then t_{RD} shall be met and t_5 is not applicable.

4. Timings based upon software control. See User's Guide.

5. All IDE timing is based upon HCLK = 100 MHz.



Note: 1. Device address consists of signals IDECS0n, IDECS1n and IDEDA (2:0)

2. Data consists of DD (15:0)

3. The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIORn or DIOWn. The assertion and negation or IORDY are described in the following three cases:

3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.

3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than t_C before release: no wait generated.

3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than t_C before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIORn is asserted, the device shall place read data on DD (15:0) for t_{RD} before asserting IORDY.

Figure 20. PIO Data Transfer to/from Device

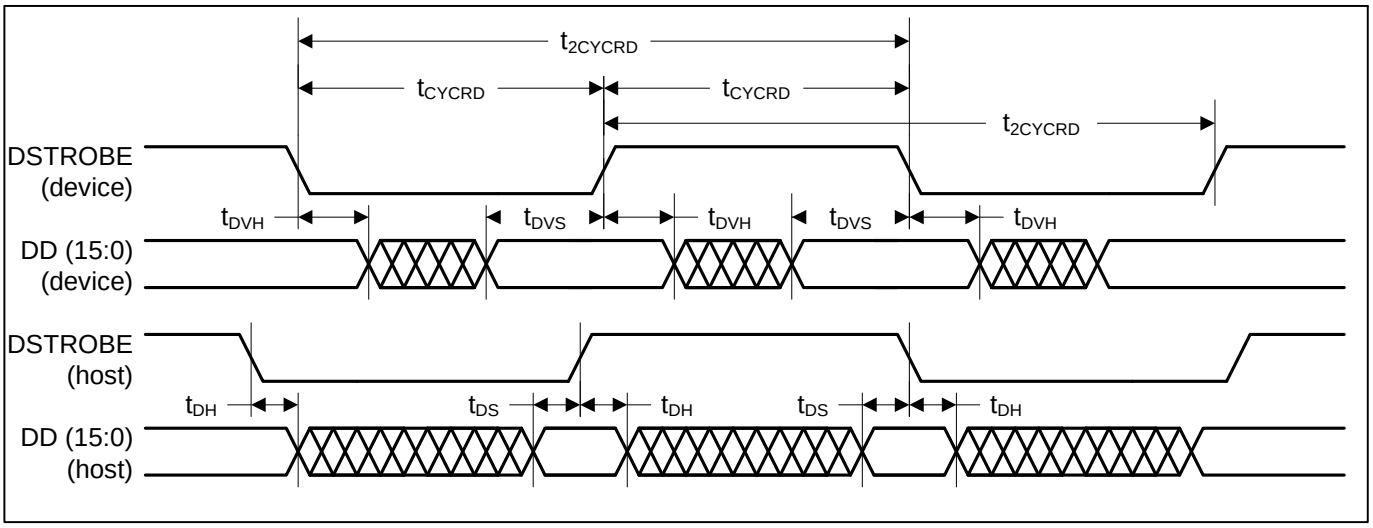
Ultra DMA Data Transfer

Figure 21 through Figure 30 define the timings associated with all phases of Ultra DMA bursts. The following table contains the values for the timings for each of the Ultra DMA modes.

Timing reference levels = 1.5 V

Parameter	Symbol	Mode 0 (in ns)		Mode 1 (in ns)		Mode 2 (in ns)		Mode 3 (in ns)	
		min	max	min	max	min	max	min	max
Cycle time allowing for asymmetry and clock variations (from DSTROBE edge to DSTROBE edge)	t_{CYCRD}	112	-	73	-	54	-	39	-
Two-cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of DSTROBE)	t_{2CYCRD}	230	-	154	-	115	-	86	-
Cycle time allowing for asymmetry and clock variations (from HSTROBE edge to HSTROBE edge)	t_{CYCWR}	230	-	170	-	130	-	100	-
Two-cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of HSTROBE)	t_{2CYCWR}	460	-	340	-	260	-	200	-
Data setup time at recipient (Read)	t_{DS}	15	-	10	-	7	-	7	-
Data hold time at recipient (Read)	t_{DH}	8	-	8	-	8	-	8	-
Data valid setup time at sender (Write) (Note 2) (from data valid until STROBE edge)	t_{DVS}	70	-	48	-	30	-	20	-
Data valid hold time at sender (Write) (Note 2) (from STROBE edge until data may become invalid)	t_{DVH}	6	-	6	-	6	-	6	-
First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	t_{FS}	0	230	0	200	0	170	0	130
Limited interlock time (Note 3)	t_{LI}	0	150	0	150	0	150	0	100
Interlock time with minimum (Note 3)	t_{MLI}	20	-	20	-	20	-	20	-
Unlimited interlock time (Note 3)	t_{UI}	0	-	0	-	0	-	0	-
Maximum time allowed for output drivers to release (from asserted or negated)	t_{AZ}	-	10	-	10	-	10	-	10
Minimum delay time required for output	t_{ZAH}	20	-	20	-	20	-	20	-
Drivers to assert or negate (from released)	t_{ZAD}	0	-	0	-	0	-	0	-
Envelope time (from DMACKn to STOP and HDMARDYn during data in burst initiation and from DMACKn to STOP during data out burst initiation)	t_{ENV}	20	70	20	70	20	70	20	55
Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDYn)	t_{RFS}	-	75	-	70	-	60	-	60
Ready-to-pause time (that recipient shall wait to pause after negating DMARDYn)	t_{RP}	160	-	125	-	100	-	100	-
Maximum time before releasing IORDY	t_{IORDYZ}	-	20	-	20	-	20	-	20
Minimum time before driving STROBE (Note 4)	t_{ZIORDY}	0	-	0	-	0	-	0	-
Setup and hold times for DMACKn (before assertion or negation)	t_{ACK}	20	-	20	-	20	-	20	-
Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	t_{SS}	50	-	50	-	50	-	50	-

Note: 1. Timing parameters shall be measured at the connector of the sender or receiver to which the parameter applies.
2. The test load for t_{DVS} and t_{DVH} shall be a lumped capacitor load with no cable or receivers. Timing for t_{DVS} and t_{DVH} shall be met for all capacitive loads from 15 to 40 pf where all signals have the same capacitive load value.
3. t_{UI}, t_{MLI} and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., either sender or recipient is waiting for the other to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
4. t_{ZIORDY} may be greater than t_{ENV} since the device has a pull up on IORDYn giving it a known state when released.
5. All IDE timing is based upon HCLK = 100 MHz.



Note: DD (15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 22. Sustained Ultra DMA data-in Burst

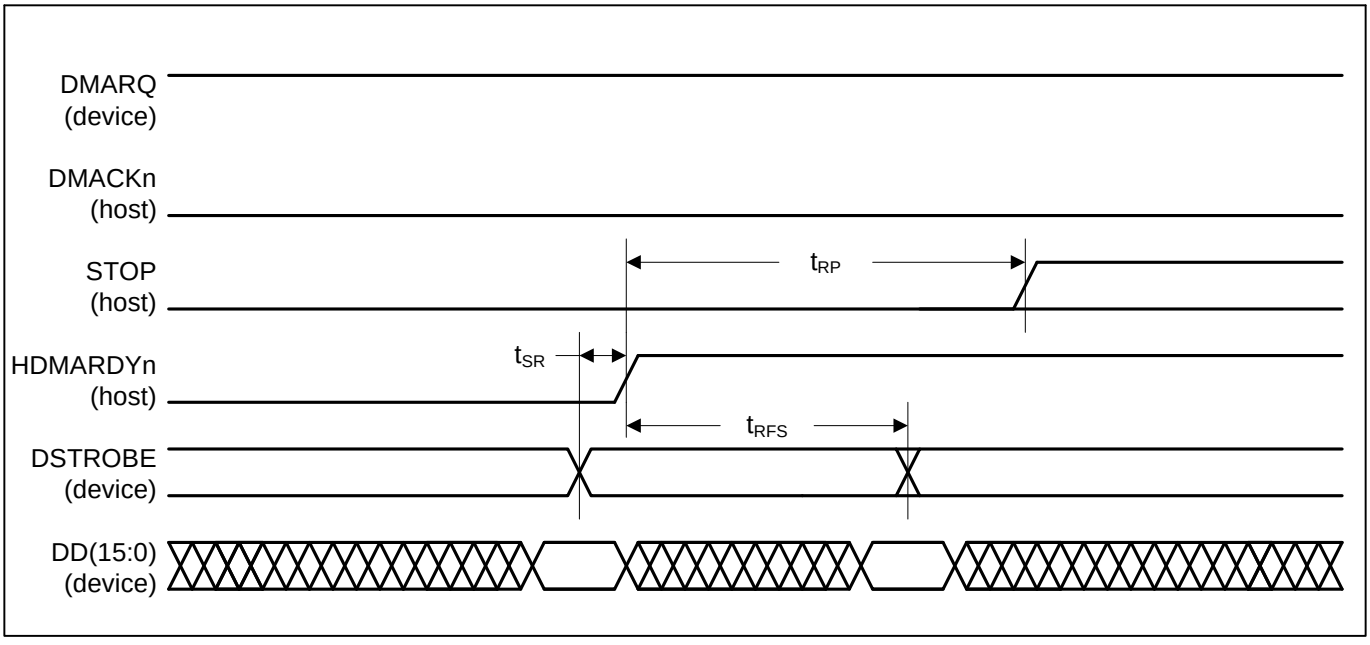
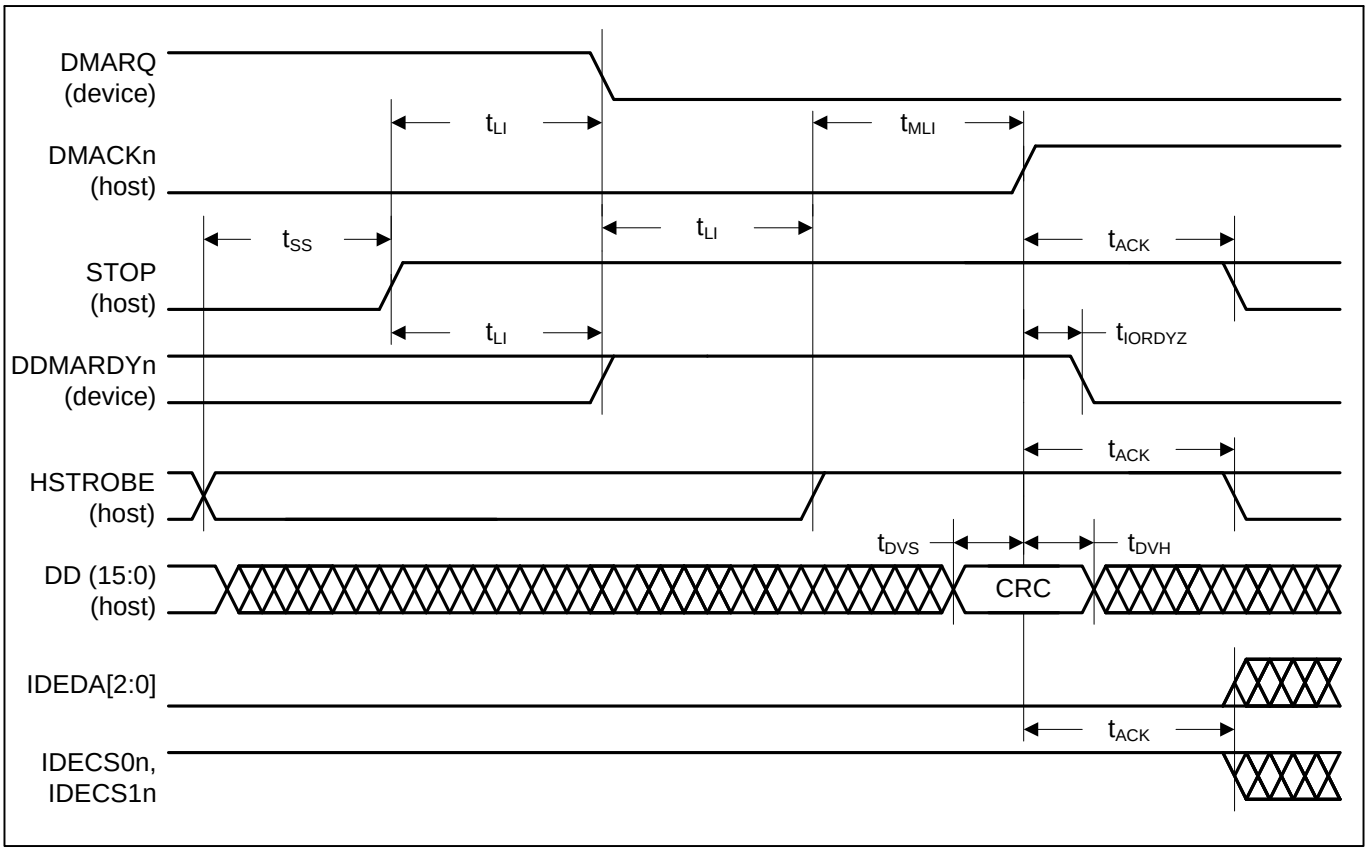


Figure 23. Host Pausing an Ultra DMA data-in Burst



Note: The definitions for the DIOWn:STOP, IORDY:DDMARDYn:DSTROBE and DIORn:HDMARDYn:HSTROBE signal lines are no longer in effect after DMARQ and DMACKn are negated.

Figure 29. Host Terminating an Ultra DMA data-out Burst

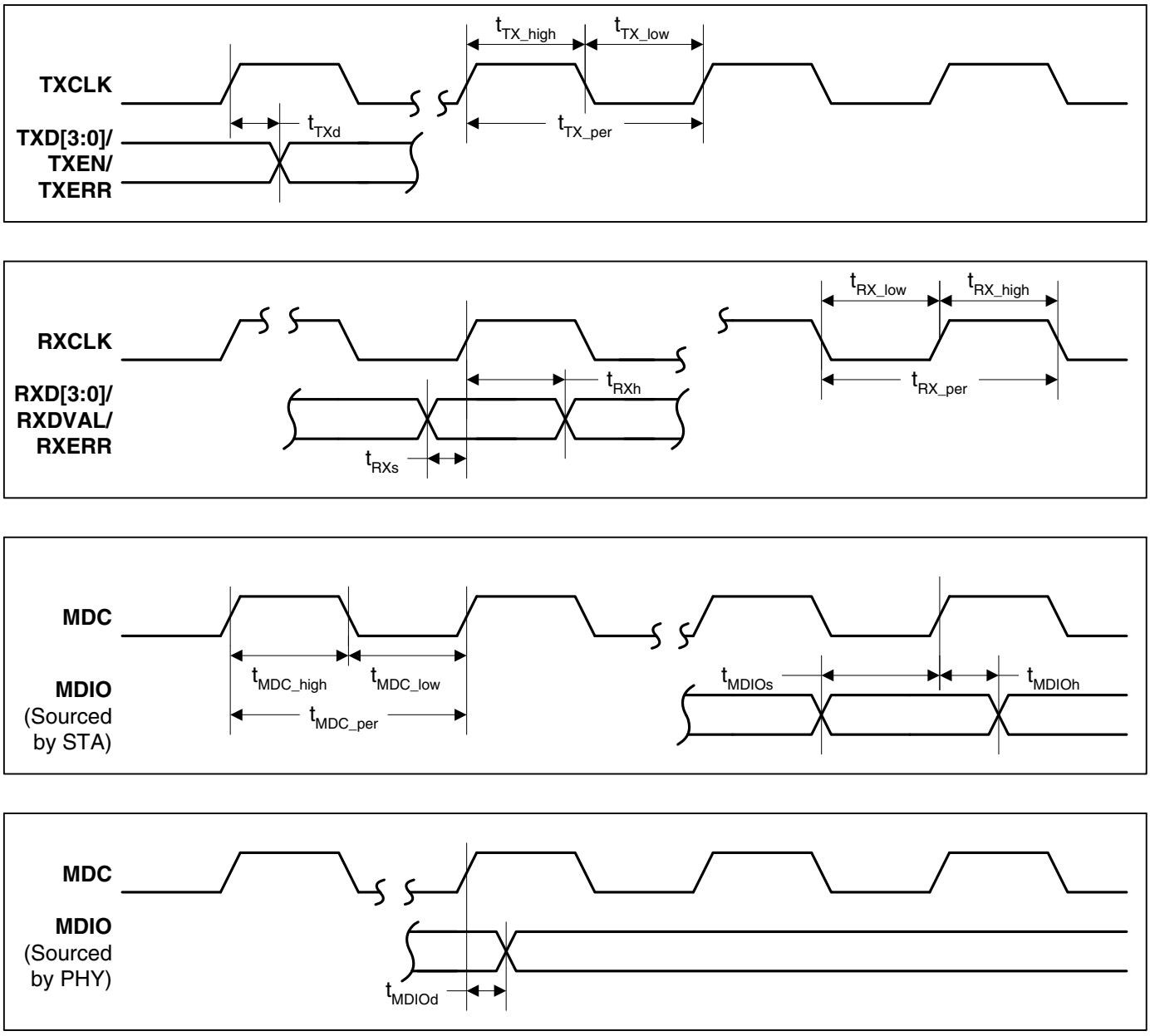


Figure 31. Ethernet MAC Timing Measurement

LCD Interface

Parameter	Symbol	Min	Typ	Max	Unit
SPCLK rise/fall time	t_{clkr}	2	-	8	ns
SPCLK rising edge to control signal transition time	t_{CD}	-	-	3	ns
SPCLK rising edge to data transition time	t_{DD}	-	-	10	ns
Data valid time	t_{Dv}	t_{SPCLK}	-	-	ns

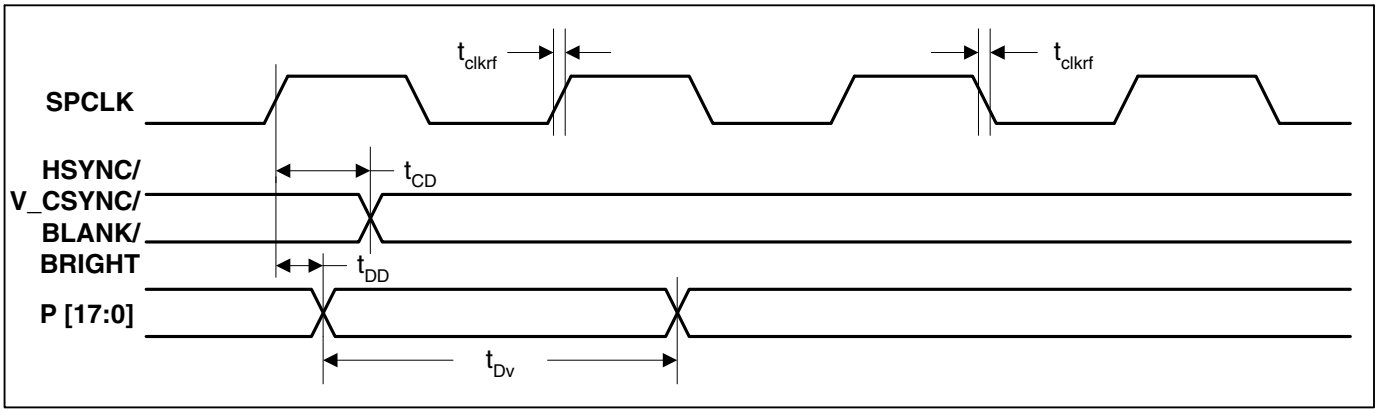
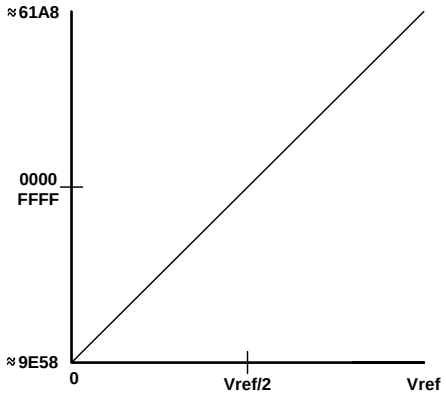


Figure 37. LCD Timing Measurement

ADC

Parameter	Comment	Value	Units
Resolution	No missing codes Range of 0 to 3.3 V	50K counts (approximate)	
Integral non-linearity		0.01%	
Offset error		±15	mV
Full scale error		0.2%	
Maximum sample rate	ADIV = 0 ADIV = 1	3750 925	Samples per second Samples per second
Channel switch settling time	ADIV = 0 ADIV = 1	500 2	µs ms
Noise (RMS) - typical		120	µV

Note: ADIV refers to bit 16 in the KeyTchClkDiv register.
ADIV = 0 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 4.
ADIV = 1 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 16.



A/D Converter Transfer Function
(approximately ±25,000 counts)

Figure 38. ADC Transfer Function

Using the ADC:

This ADC has a state-machine based conversion engine that automates the conversion process. The initiator for a conversion is the read access of the TSXYResult register by the CPU. The data returned from reading this register contains the result as well as the status bit indicating the state of the ADC. However, this peripheral requires a delay between each successful conversion and the issue of the next conversion command, or else the returned value of successive samples may not reflect the analog input. Since the state of the ADC state machine is returned through the same channel used to initiate the conversion process, there must be a delay inserted after every complete conversion. Note that reading TSXYResult during a conversion will not affect the result of the ongoing process.

The following is a recommended procedure for safely polling the ADC from software:

1. Read the TSXYResult register into a local variable to initiate a conversion.
2. If the value of bit 31 of the local variable is '0' then repeat step 1.
3. Delay long enough to meet the maximum sample rate as shown above.
4. Mask the local variable with 0xFFFF to remove extraneous data.
5. If signed mode is used, do a sign extend of the lower halfword.
6. Return the sampled value.

Table S. Pin Descriptions *(Continued)*

Pin Name	Block	Pad Type	Pull Type	Description
MDIO	EMAC	4ma	PU	Management data input/output
RXCLK	EMAC	I	PD	Receive clock in
MIIRXD[3:0]	EMAC	I	PD	Receive data in
RXDVAL	EMAC	I	PD	Receive data valid
RXERR	EMAC	I	PD	Receive data error
TXCLK	EMAC	I	PU	Transmit clock in
MIITXD[3:0]	EMAC	I	PD	Transmit data out
TXEN	EMAC	4ma	PD	Transmit enable
TXERR	EMAC	4ma	PD	Transmit error
CRS	EMAC	I	PD	Carrier sense
CLD	EMAC	I	PU	Collision detect
GRLED	LED	12ma		Green LED
RDLED	LED	12ma		Red LED
EECLK	EEPROM	4ma	PU	EEPROM / Two-wire Interface clock
EEDAT	EEPROM	4ma	PU	EEPROM / Two-wire Interface data
ABITCLK	AC97	8ma	PD	AC97 bit clock
ASYNC	AC97	8ma	PD	AC97 frame sync
ASDI	AC97	I	PD	AC97 Primary input
ASDO	AC97	8ma	PU	AC97 output
ARSTn	AC97	8ma		AC97 reset
SCLK1	SPI1	8ma	PD	SPI bit clock
SFRM1	SPI1	8ma	PD	SPI Frame Clock
SSPRX1	SPI1	I	PD	SPI input
SSPTX1	SPI1	8ma		SPI output
INT[3:0]	INT	I	PD	External interrupts
PRSTn	Syscon	I	PU	Power on reset
RSTOn	Syscon	4ma		User Reset in out - open drain
SLA[1:0]	EEPROM	4ma		Flash programming voltage control
VS1	PCMCIA	I	PU	Voltage sense
VS2	PCMCIA	I	PU	Voltage sense
MCD1	PCMCIA	I	PU	Card detect
MCD2	PCMCIA	I	PU	Card detect
MCBVD1	PCMCIA	I	PU	Voltage detection / status change
MCBVD2	PCMCIA	I	PU	Voltage detection
MCDIR	PCMCIA	4ma		Data transceiver direction control
MCDAENn	PCMCIA	4ma		Data bus transceiver enable
MCADENn	PCMCIA	4ma		Address bus transceiver enable
MCREGn	PCMCIA	4ma	PU	Memory card register
MCEHn	PCMCIA	4ma	PU	Memory card high byte select
MCELn	PCMCIA	4ma	PU	Memory card low byte select
IORDn	PCMCIA	4ma	PU	I/O card read
IOWRn	PCMCIA	4ma	PU	I/O card write
MCRDn	PCMCIA	4ma	PU	Memory card read
MCWRn	PCMCIA	4ma	PU	Memory card write
READY	PCMCIA	I	PU	Ready / interrupt
WP	PCMCIA	I	PU	Write protect
MCWAITn	PCMCIA	I	PU	Wait Input
MCRESETn	PCMCIA	4ma		Card reset

Table S. Pin Descriptions *(Continued)*

Pin Name	Block	Pad Type	Pull Type	Description
EGPIO[15:0]	GPIO	I/O, 4 ma	PU	Enhanced GPIO
DD[15:8]	IDE	8ma	PU	IDE data bus
DD7	IDE	8ma	PD	IDE data bus
DD[6:0]	IDE	8ma	PU	IDE data bus
IDEDA[2:0]	IDE	8ma		IDE Device address output
IDECS0n	IDE	8ma		IDE Chip Select 0 output
IDECS1n	IDE	8ma		IDE Chip Select 1 output
DIORn	IDE	8ma		IDE Read strobe output
DIOWn	IDE	8ma		IDE Write strobe output
DMACKn	IDE	8ma		IDE DMA acknowledge output
IORDY	IDE	I	PU	IDE ready input
CVDD	Power	P		Digital power, 1.8V
RVDD	Power	P		Digital power, 3.3V
CGND	Ground	G		Digital ground
RGND	Ground	G		Digital ground

Table T illustrates the pin signal multiplexing and configuration options.

Table T. Pin Multiplex Usage Information

Physical Pin Name	Description	Multiplex signal name
COL[7:0]	GPIO	GPIO Port D[7:0]
ROW[7:0]	GPIO	GPIO Port C[7:0]
EGPIO[0]	Ring Indicator Input	RI
EGPIO[1]	1Hz clock monitor	CLK1HZ
EGPIO[2]	IDE DMA request	DMARQ
EGPIO[3]	Transmit Enable output / HDLC clocks	TENn / HDLCCLK1 / HDLCCLK3
EGPIO[4]	I2S Transmit Data 1	SDO1
EGPIO[5]	I2S Receive Data 1	SDI1
EGPIO[6]	I2S Transmit Data 2	SDO2
EGPIO[7]	DMA Request 0	DREQ0
EGPIO[8]	DMA Acknowledge 0	DACK0
EGPIO[9]	DMA EOT 0	DEOT0
EGPIO[10]	DMA Request 1	DREQ1
EGPIO[11]	DMA Acknowledge 1	DACK1
EGPIO[12]	DMA EOT 1	DEOT1
EGPIO[13]	I2S Receive Data 2	SDI2
EGPIO[14]	PWM 1 output	PWMOUT1
EGPIO[15]	IDE Device active / present	DASP
ABITCLK	I2S Serial clock	SCLK
ASYNC	I2S Frame Clock	LRCK
ASDO	I2S Transmit Data 0	SDO0
ASDI	I2S Receive Data 0	SDI0
ARSTn	I2S Master clock	MCLK
SCLK1	I2S Serial clock	SCLK
SFRM1	I2S Frame Clock	LRCK
SSPTX1	I2S Transmit Data 0	SDO0
SSPRX1	I2S Receive Data 0	SDI0
IDEDA[2:0]	GPIO	GPIO Port E[7:5]
IDECS0n	GPIO	GPIO Port E[4]
IDECS1n	GPIO	GPIO Port E[3]
DIORn	GPIO	GPIO Port E[2]
GRLED	LED	GPIO Port E[1]
RDLED	LED	GPIO Port E[0]
DD[7:0]	GPIO	GPIO Port H[7:0]
DD[15:12]	GPIO	GPIO Port G[7:4]
SLA[1:0]	GPIO	GPIO Port G[3:2]
EEDAT	GPIO	GPIO Port G[1]
EECLK	GPIO	GPIO Port G[0]
FGPIO[7]	GPIO	VS2
FGPIO[6]	GPIO	READY
FGPIO[5]	GPIO	VS1
FGPIO[4]	GPIO	MCBVD2
FGPIO[3]	GPIO	MCBVD1
FGPIO[2]	GPIO	MCD2
FGPIO[1]	GPIO	MCD1
FGPIO[0]	GPIO	WP

Acronyms and Abbreviations

The following tables list abbreviations and acronyms used in this data sheet.

Term	Definition
ADC	Analog-to-Digital Converter
ALT	Alternative
AMBA	Advanced Micro-controller Bus Architecture
ATAPI	ATA Packet Interface
CODEC	COder / DECoder
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	Direct-Memory Access
EBUS	External Memory Bus
EEPROM	Electronically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
FIFO	First In / First Out
FIQ	Fast Interrupt Request
FLASH	Flash memory
GPIO	General Purpose I/O
HDLC	High-level Data Link Control
I/F	Interface
I^2S	Inter-IC Sound
IC	Integrated Circuit
ICE	In-Circuit Emulator
IDE	Integrated Drive Electronics
IEEE	Institute of Electronics and Electrical Engineers
IrDA	Infrared Data Association
IRQ	Standard Interrupt Request
ISO	International Standards Organization
JTAG	Joint Test Action Group
LFSR	Linear Feedback Shift Register
MII	Media Independent Interface
MMU	Memory Management Unit
OHCI	Open Host Controller Interface
PHY	Ethernet PHYsical layer interface
PIO	Programmed I/O
RISC	Reduced Instruction Set Computer
SDMI	Secure Digital Music Initiative
SDRAM	Synchronous Dynamic RAM
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STA	Station - Any device that contains an IEEE 802.11 conforming Medium Access Control (MAC) and physical layer (PHY) interface to the wireless medium
TFT	Thin Film Transistor
TLB	Translation Lookaside Buffer
USB	Universal Serial Bus

Units of Measurement

Symbol	Unit of Measure
$^{\circ}C$	degree Celsius
Hz	Hertz = cycle per second
Kbps	Kilobits per second
kbyte	Kilobyte
kHz	KiloHertz = 1000 Hz
Mbps	Megabits per second
MHz	MegaHertz = 1,000 kHz
µA	microAmpere = 10^{-6} Ampere
µs	microsecond = 1,000 nanoseconds = 10^{-6} seconds
mA	milliAmpere = 10^{-3} Ampere
ms	millisecond = 1,000 microseconds = 10^{-3} seconds
mW	milliWatt = 10^{-3} Watts
ns	nanosecond = 10^{-9} seconds
pF	picoFarad = 10^{-12} Farads
V	Volt
W	Watt