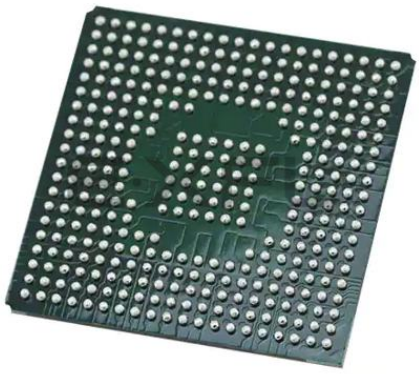

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Math Engine; MaverickCrunch™
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	352-BBGA
Supplier Device Package	352-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9315-ibz

OVERVIEW

The EP9315 is an ARM920T-based system-on-a-chip design with a large peripheral set targeted to a variety of applications:

- Thin Client Computers for Business and Home
- Internet Radio
- Internet Access Devices
- Industrial Computers
- Specialized Terminals
- Point-of-sale Terminals
- Test and Measurement Equipment

The ARM920T microprocessor core with separate 16-kbyte, 64-way set-associative instruction and data caches is augmented by the MaverickCrunch™ co-processor, enabling high-speed floating point calculations.

MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100-Mbps Ethernet media access controller (EMAC) is included along with external interfaces to SPI, I^2S audio, Raster/LCD, IDE storage peripherals, keypad, and touchscreen. A three-port USB 2.0 Full Speed Host (OHCI) (12 Mbits per second) and three UARTs are included as well.

The EP9315 is a high-performance, low-power, RISC-based, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 200 MHz (184 MHz for industrial conditions). The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 mW and 750 mW (dependent on speed).

Table A. Revision History

Revision	Date	Changes
PP1	January 2004	Initial Release.
PP2	July 2004	Update AC data. Add ADC data.
PP3	Febuary 2005	Update electrical characteristics based upon more complete characterization data.
PP4	March 2005	Minor correction to block diagram on page 1..
PP5	October 2007	Updated PCMCIA timing descriptions on pages 30 and 31.
F1	February 2010	Removed “Preliminary Data” statement from legal disclaimer. Removed lead-containing device part numbers. Increased minimum CVDD & VDD_PLL voltages from 1.65 V min. to 1.71 V min. Changed operating temperatures to 0 to 60°C commercial, -40 to 70°C industrial.
F2	March 2010	Added note restricting power dissipationat temperature. Increased commercial/industrial temperatures to 70/85 deg. C max.

List of Figures

IDE Interface

The IDE Interface provides an industry-standard connection to two AT Advanced Packet Interface (ATAPI) compliant devices. The IDE port will attach to a master and a slave device. The internal DMA controller performs all data transfers using the Ultra DMA modes. The interface supports the following operating modes:

- PIO Mode 0 thru 4
- Ultra DMA Modes 0 thru 3

Table C. IDE Interface Pin Assignments

Pin Mnemonic	Pin Description
DD[15-0]	IDE Data bus
IDEDA[2-0]	IDE Device address
IDECSn[0,1]	IDE Chip Select 0 and 1
DIORn	IDE Read Strobe
DIOWn	IDE Write Strobe
DMACKn	IDE DMA acknowledge

Ethernet Media Access Controller (MAC)

The MAC subsystem is compliant with the ISO/TEC 802.3 topology for a single shared medium with several stations. Multiple MII-compliant PHYs are supported. Features include:

- Supports 1/10/100 Mbps transfer rates for home / small-business / large-business applications
- Interfaces to an off-chip PHY through industry standard Media Independent Interface (MII)

Table D. Ethernet Media Access Controller Pin Assignments

Pin Mnemonic	Pin Description
MDC	Management Data Clock
MDIO	Management Data I/O
RXCLK	Receive Clock
MIIRXD[3:0]	Receive Data
RXDVAL	Receive Data Valid
RXERR	Receive Data Error
TXCLK	Transmit Clock
MIITXD[3:0]	Transmit Data
TXEN	Transmit Enable
TXERR	Transmit Error
CRS	Carrier Sense
CLD	Collision Detect

Serial Interfaces (SPI, I^{2}S and AC ’97)

The SPI port can be configured as a master or a slave, supporting the National Semiconductor®, Motorola® and Texas Instruments® signaling protocols.

The AC'97 port supports multiple codecs for multichannel audio output with a single stereo input. Three I^{2}S ports can be configured to support six channel 24-bit audio.

These ports are multiplexed so that I^{2}S port 0 will take over either the AC'97 pins or the SPI pins. The second and third I2S ports' serial input and serial output pins are multiplexed with EGPIO[4,5,6,13]. The clocks supplied in the first I2S port are also used for the second and third I2S ports.

- Normal Mode: One SPI Port and one AC’97 Port
- I^{2}S on SSP Mode: One AC’97 Port and up to three I^{2}S Ports
- I^{2}S on AC’97 Mode: One SPI Port and up to three I^{2}S Ports

Table E. Audio Interfaces Pin Assignment

Pin Name	Normal Mode	I2S on SSP Mode	I2S on AC'97 Mode
	Pin Description	Pin Description	Pin Description
SCLK1	SPI Bit Clock	I2S Serial Clock	SPI Bit Clock
SFRM1	SPI Frame Clock	I2S Frame Clock	SPI Frame Clock
SSPRX1	SPI Serial Input	I2S Serial Input	SPI Serial Input
SSPTX1	SPI Serial Output	I2S Serial Output	SPI Serial Output
		(No I2S Master Clock)	
ARSTn	AC'97 Reset	AC'97 Reset	I2S Master Clock
ABITCLK	AC'97 Bit Clock	AC'97 Bit Clock	I2S Serial Clock
ASYNC	AC'97 Frame Clock	AC'97 Frame Clock	I2S Frame Clock
ASDI	AC'97 Serial Input	AC'97 Serial Input	I2S Serial Input
ASDO	AC'97 Serial Output	AC'97 Serial Output	I2S Serial Output

Raster / LCD Interface

The Raster / LCD interface provides data and interface signals for a variety of display types. It features fully programmable video interface timing for non-interlaced flat panel or dual scan displays. Resolutions up to 1024 x 768 are supported from a unified SDRAM based frame buffer. A 16-bit PWM provides control for LCD panel contrast. LCD specific features include:

Real-Time Clock with Software Trim

The software trim feature on the real time clock (RTC) provides software controlled digital compensation of the 32.768 kHz input clock. This compensation is accurate to ±1.24 sec/month.

Note: A real time clock must be connected to RTCXTALI or the EP9315 device will not boot.

Table L. Real-Time Clock with Pin Assignments

Pin Mnemonic	Pin Name - Description
RTCXTALI	Real-Time Clock Oscillator Input
RTCXTALO	Real-Time Clock Oscillator Output

PLL and Clocking

The processor and the peripheral clocks operate from a single 14.7456 MHz crystal.

The real time clock operates from a 32.768 kHz external oscillator.

Table M. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Name - Description
XTALI	Main Oscillator Input
XTALO	Main Oscillator Output
VDD_PLL	Main Oscillator Power
GND_PLL	Main Oscillator Ground

Timers

The Watchdog Timer insures proper operation by requiring periodic attention to prevent a reset-on-time-out.

Two 16-bit timers operate as free running down-counters or as periodic timers for fixed interval interrupts and have a range of 0.03 ms to 4.27 seconds.

One 32-bit timer, plus a 6-bit prescale counter, has a range of 0.03 µs to 73.3 hours.

One 40-bit debug timer, plus 6-bit prescale counter, has a range of 1.0 µs to 12.7 days.

Interrupt Controller

The interrupt controller allows up to 64 interrupts to generate an Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) signal to the processor core. Thirty-two hardware priority assignments are provided for assisting IRQ vectoring, and two levels are provided for FIQ vectoring. This allows time critical interrupts to be processed in the shortest time possible. Internal interrupts may be programmed as active-high or active-low, level-sensitive inputs. GPIO may be programmed as active-high level-sensitive, active-low level-sensitive, rising-edge-triggered, falling-edge-triggered, or combined rising/falling-edge-triggered.

- Supports 64 interrupts from a variety of sources (such as UARTs, GPIO, and key matrix)
- Routes interrupt sources to either the ARM920T's IRQ or FIQ (Fast IRQ) inputs
- Four dedicated off-chip interrupt lines INT[3:0] operate as active-high, level-sensitive interrupts
- Any of the 16 GPIO lines maybe configured to generate interrupts
- Software supported priority mask for all FIQs and IRQs

Table N. External Interrupt Pin Assignment

Pin Mnemonic	Pin Name - Description
INT[3:0]	External Interrupt 3-0

Dual LED Drivers

Two pins are assigned specifically to drive external LEDs.

Table O. Dual LED Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
GRLED	Green LED	General Purpose I/O
REDLED	Red LED	General Purpose I/O

General Purpose Input/Output (GPIO)

The 16 EGPIO pins may each be configured individually as an output, an input, or an interrupt input. Port F may be configured as GPIO. Each Port F pin may be configured individually as an output, input or an interrupt input.

There are 23 pins that may be used as alternate inputs or outputs, but do not support interrupts. These pins are:

- Key Matrix ROW[7:0], COL[7:0]
- Ethernet MDIO
- Both LED Outputs
- Two-wire Clock and Data
- SLA [1:0]

6 pins may alternatively be used as inputs only:

- CTSn, DSRn / DCDn
- 4 Interrupt Lines

2 pins may alternatively be used as outputs only:

- RTSn
- ARSTn

Table P. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[7:0]	Expanded General Purpose Input / Output Pins with Interrupts

Note: Port F defaults as PCMCIA pins. Port F must be configured by software to be used as GPIO.

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 200 MHz (184 MHz for industrial conditions).

Table Q. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Note: The JTAG interface does not support boundary scan.

Table R. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

Internal Boot ROM

The Internal 16-kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP93xx User's Manual for operational details

12-channel DMA Controller

The DMA module contains 12 separate DMA channels. Ten of these may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio, and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

PCMCIA Interface

The EP9315 has a single PCMCIA port which can be used to access either 8 or 16-bit devices.

Table S. PCMCIA Interface

Pin Mnemonic	Pin Name - Description
VS1	Voltage sense
VS2	Voltage sense
MCD1	Card detect
MCD2	Card detect
MCBVD1	Voltage detection / status change
MCBVD2	Voltage detection
MCDIR	Data transceiver direction control
MCDAENn	Data bus transceiver enable
MCADENn	Address bus transceiver enable
MCREGn	Memory card register
MCEHn	Memory card high byte select
MCELn	Memory card low byte select
IORDn	I/O card read
IOWRn	I/O card write
MCRDn	Memory card read
MCWRn	Memory card write
READY	Ready / interrupt
WP	Write protect
MCWAITn	Wait Input
MCRESETn	Card reset

Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	- - - -	3.96 2.16 2.16 3.96	V V V V
Total Power Dissipation	(Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)			-	±10	mA
Output current per pin, DC			-	±50	mA
Digital Input voltage	(Note 2)		-0.3	RVDD+0.3	V
Storage temperature			-40	+125	°C

Note: 1. Includes all power generated due to AC and/or DC output loading.
2. The power supply pins are at recommended maximum values.

Caution: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	3.0 1.71 1.71 3.0	3.3 1.80 1.80 3.3	3.6 1.94 1.94 3.6	V V V V
Operating Ambient Temperature - Commercial	(Note 3)	T_A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	(Note 4)	T_A	-40	+25	+85	°C
Processor Clock Speed - Commercial		FCLK	-	-	200	MHz
Processor Clock Speed - Industrial		FCLK	-	-	184	MHz
System Clock Speed - Commercial		HCLK	-	-	100	MHz
System Clock Speed - Industrial		HCLK	-	-	92	MHz

Note: 3. The device is capable of operating up to 70° C ambient under typical operating conditions with power consumption less than 1.5W.
4. The device is capable of operating up to 85° C ambient under typical operating conditions with power consumption less than 1.5W.

Timings

Timing Diagram Conventions

This data sheet contains one or more timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

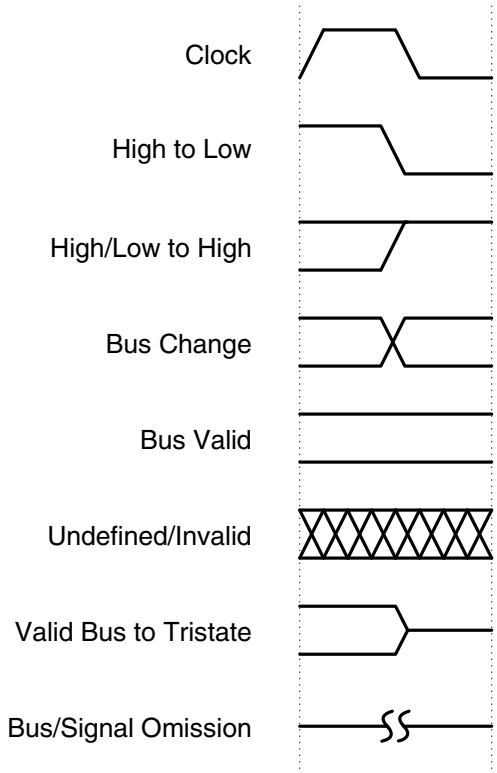

Figure 1. Timing Diagram Drawing Key

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements.

- T_A = 0 to 70° C
- CVDD = VDD_PLL = 1.8V
- RVDD = 3.3 V
- All grounds = 0 V
- Logic 0 = 0 V, Logic 1 = 3.3 V
- Output loading = 50 pF
- Timing reference levels = 1.5 V
- The Processor Bus Clock (HCLK) is programmable and is set by the user. The frequency is typically between 33 MHz and 100 MHz (92 MHz for industrial conditions).

SDRAM Burst Read Cycle

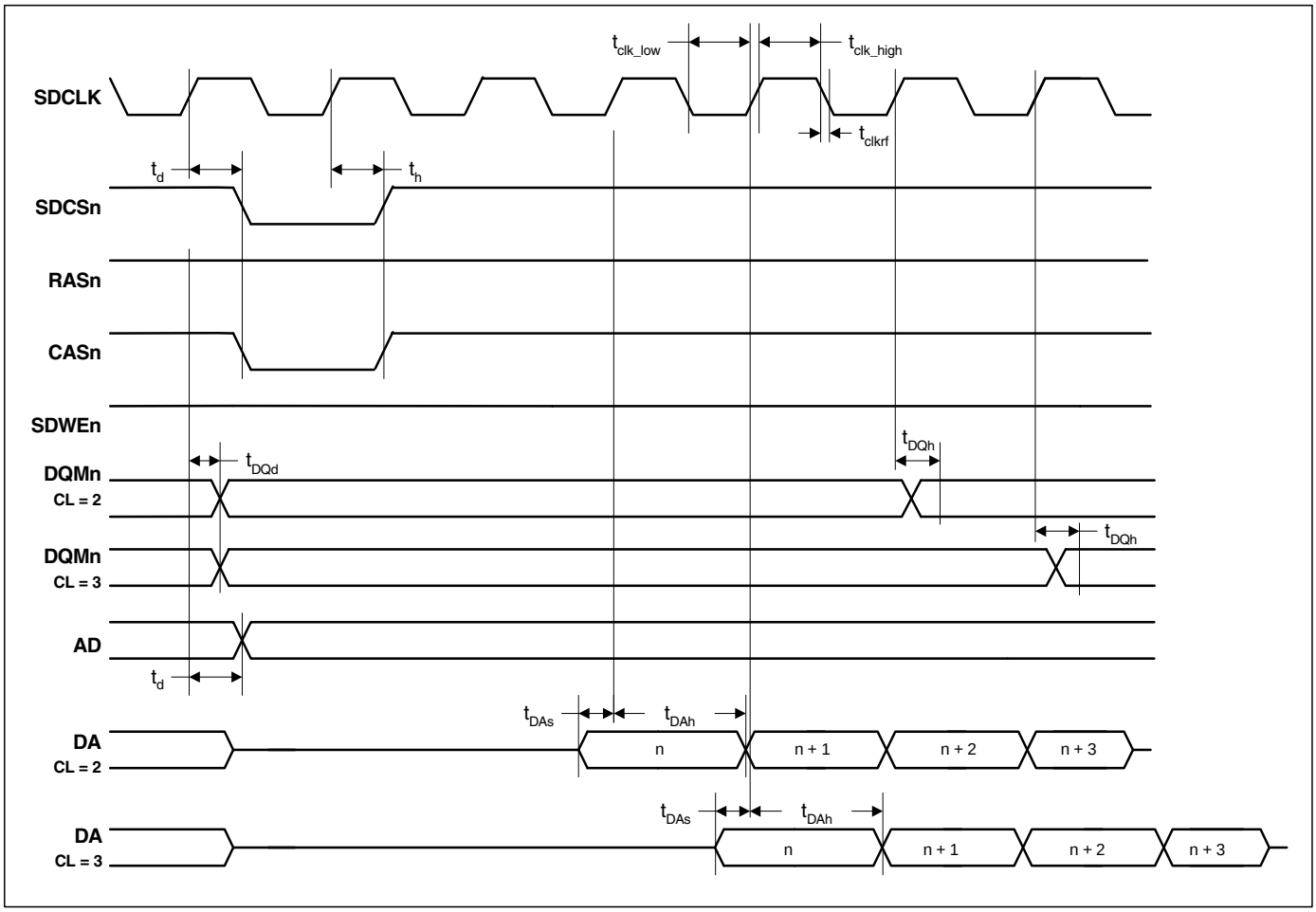

Figure 3. SDRAM Burst Read Cycle Timing Measurement

SDRAM Burst Write Cycle

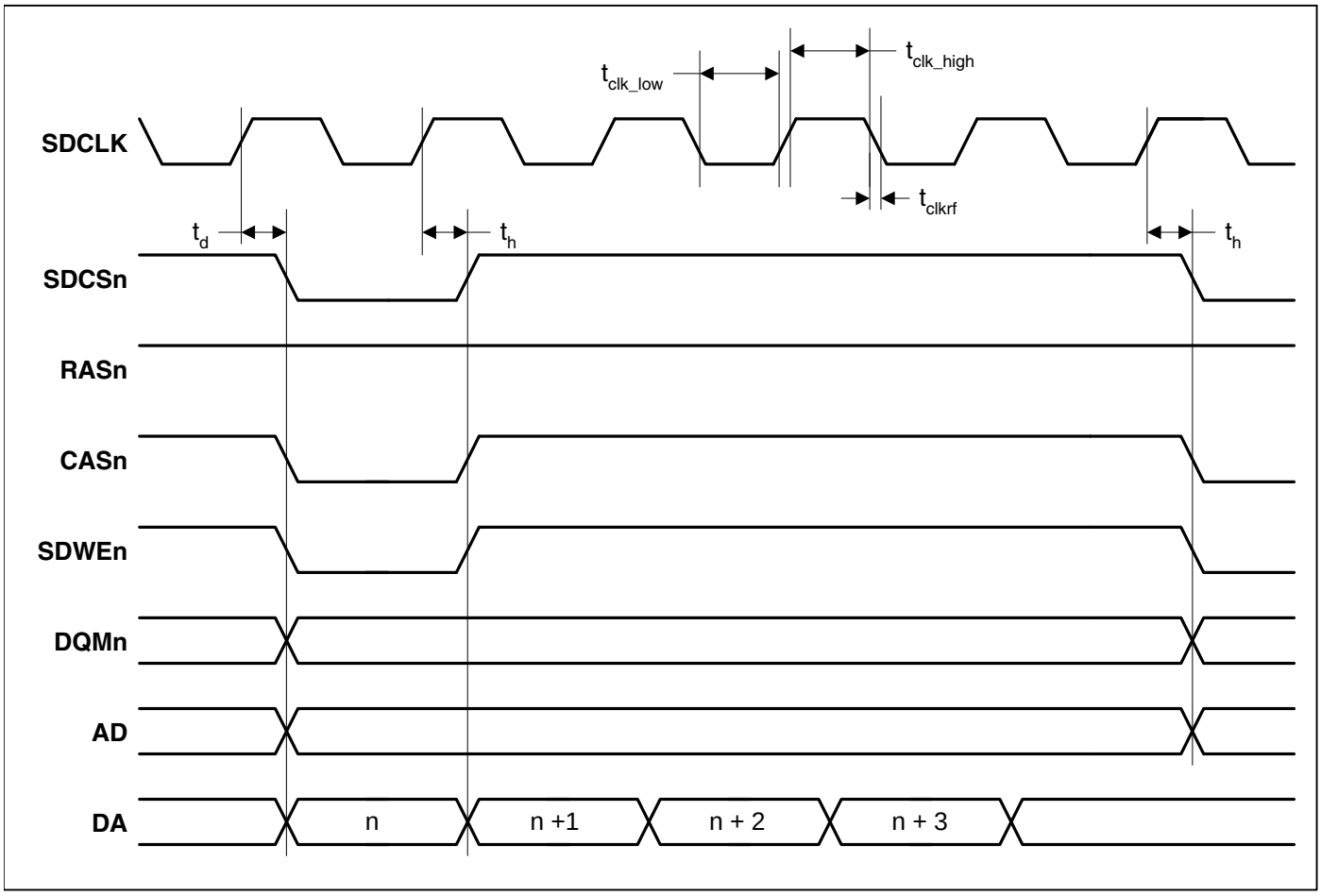

Figure 4. SDRAM Burst Write Cycle Timing Measurement

Static Memory 32-bit Write on 16-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	-	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh1}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

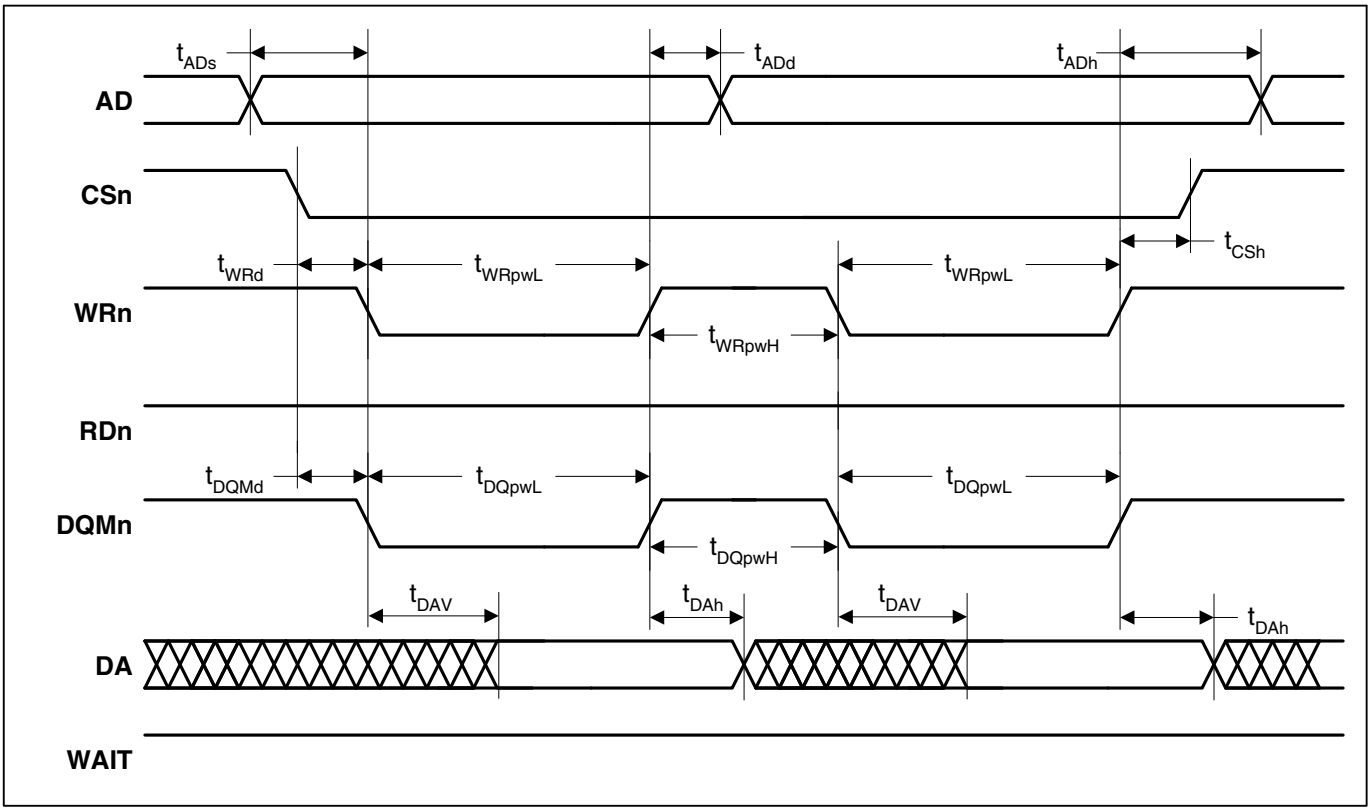

Figure 11. Static Memory Multiple Word Write 16-bit Cycle Timing Measurement

Static Memory Burst Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to Address 1 transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{ADd2}	-	$t_{HCLK} \times (WST2 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to CSn deassert time	t_{DAs2}	t_{HCLK} + 12	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

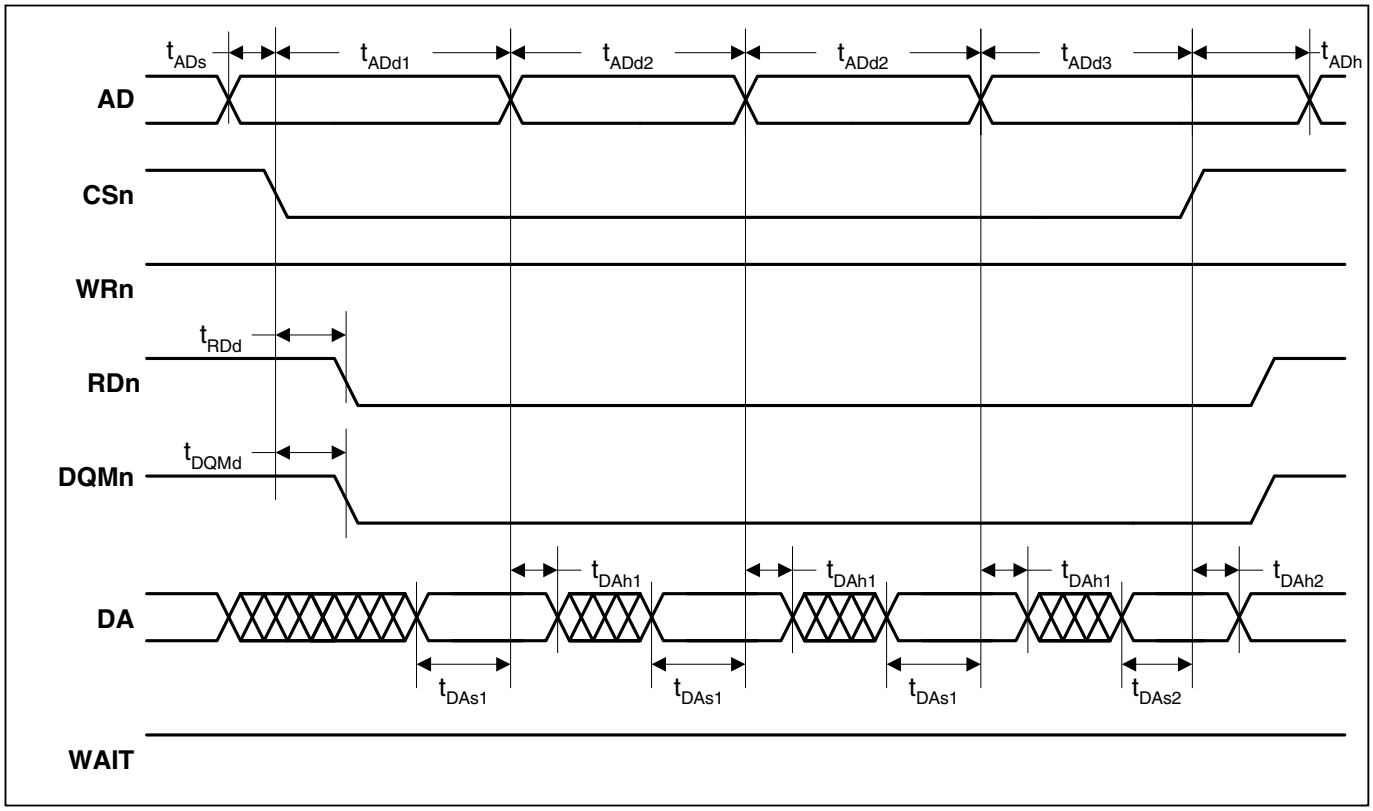

Figure 12. Static Memory Burst Read Cycle Timing Measurement

Static Memory Single Read Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

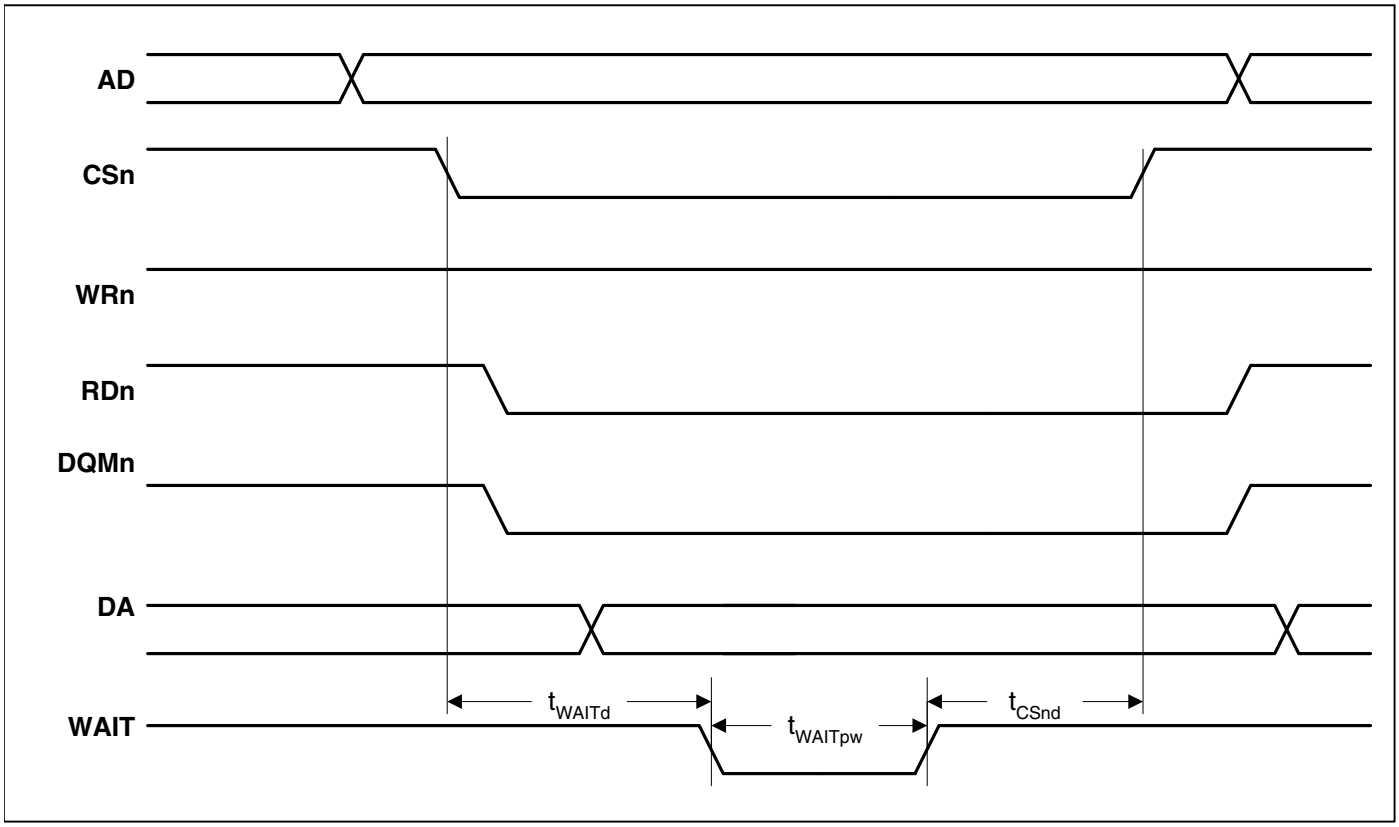

Figure 14. Static Memory Single Read Wait Cycle Timing Measurement

Static Memory Single Write Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
WAIT to WRn deassert delay time	t_{WRd}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 4$	ns
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times$ (WST1-2)	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

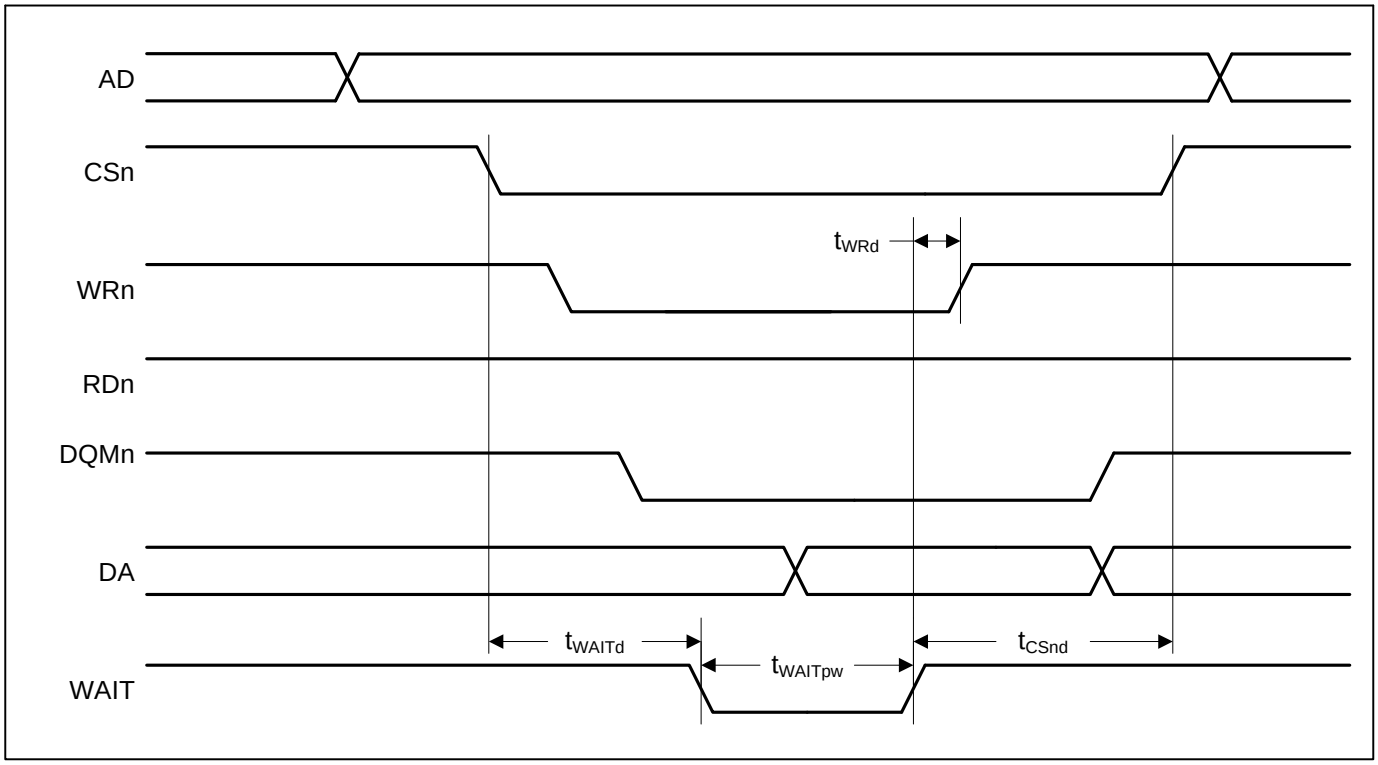

Figure 15. Static Memory Single Write Wait Cycle Timing Measurement

PCMCIA Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to signal transition time	t_{ADs}	0	-	-	ns
MCDIR hold time	t_{MCDh}	0	-	-	ns
MCEHn/MCELn/MCREGn hold time	t_{MCEh}	0	-	-	ns
DATA invalid delay time	t_{DAfo}	0	-	-	ns
Wait Time[1]	t_W	-	-	t_A-[2 × t_{HCLK}]	ns
Attribute Mode Timing					
Attribute access time	t_A	[(AA + 1) × t_{HCLK}] - 14	(AA + 1) × t_{HCLK}	-	ns
Attribute hold time	t_H	[(HA + 1) × t_{HCLK}] - 3	(HA + 1) × t_{HCLK}	-	ns
Attribute space pre-charge delay time	t_p	(PA + 1) × t_{HCLK}	(PA + 1) × t_{HCLK}	-	ns
Common Mode Timing					
Common access time	t_A	[(AC + 1) × t_{HCLK}] - 14	(AC + 1) × t_{HCLK}	-	ns
Common hold time	t_H	[(HC + 1) × t_{HCLK}] - 3	(HC + 1) × t_{HCLK}	-	ns
Common space pre-charge delay time	t_p	(PC + 1) × t_{HCLK}	(PC + 1) × t_{HCLK}	-	ns
I/O Mode Timing					
I/O access time	t_A	[(AI + 1) × t_{HCLK}] - 14	(AI + 1) × t_{HCLK}	-	ns
I/O hold time	t_H	[(HI + 1) × t_{HCLK}] - 3	(HI + 1) × t_{HCLK}	-	ns
I/O space pre-charge delay time	t_p	(PI + 1) × t_{HCLK}	(PI + 1) × t_{HCLK}	-	ns

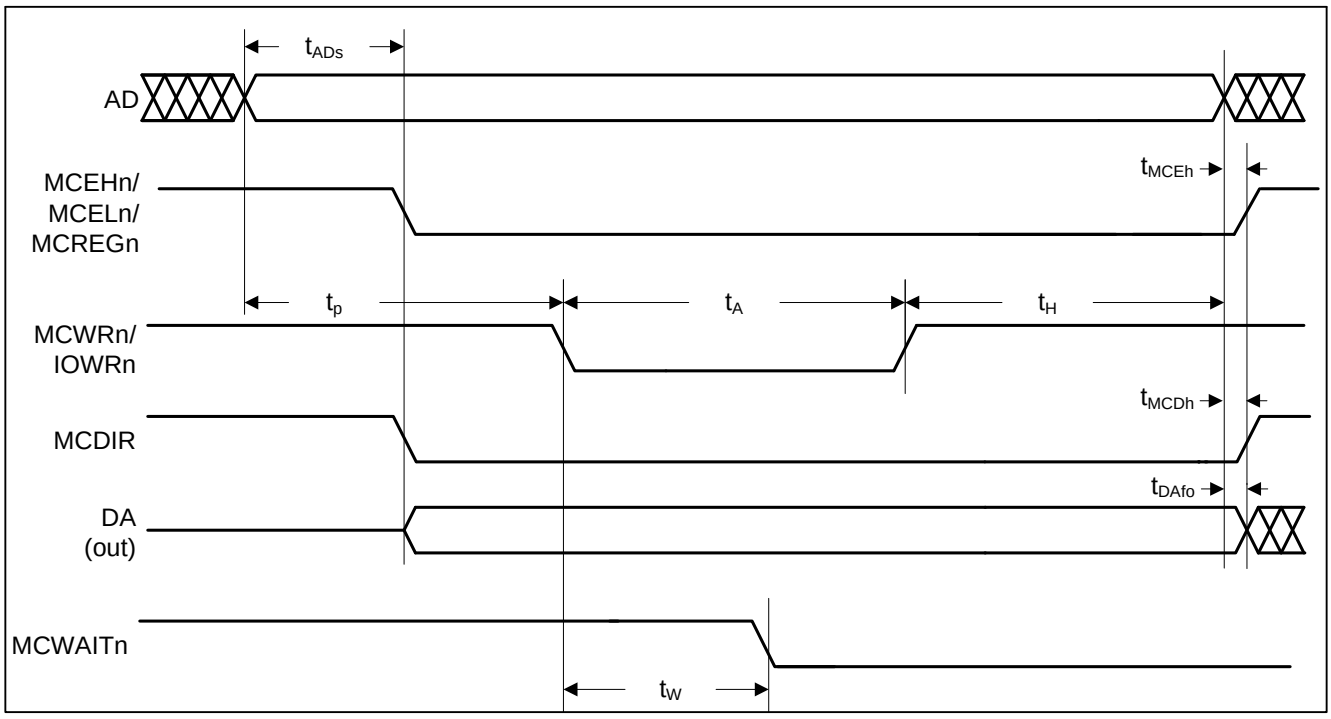

Figure 18. PCMCIA Write Cycle Timing Measurement

Note: MCWAITn asserted will extend the MCWR / IOWR strobe time.

IDE Interface

Register Transfers

Parameter			Symbol	Mode 0 (in ns)	Mode 1 (in ns)	Mode 2 (in ns)	Mode 3 (in ns)	Mode 4 (in ns)
Cycle time	(min)	(Notes 1, 4, 5)	t_0	600	383	330	180	120
Address valid to DIORn / DIOWn setup	(min)	(Note 4)	t_1	70	50	30	30	25
DIORn / DIOWn pulse width 8-bit	(min)	(Note 1, 4)	t_2	290	290	290	80	70
DIORn / DIOWn recovery time	(min)	(Note 1, 4)	t_{2i}	-	-	-	70	25
DIOWn data setup	(min)	(Note 4)	t_3	60	45	30	30	20
DIOWn data hold	(min)		t_4	0	0	0	0	0
DIORn data setup	(min)		t_5	20	20	20	20	20
DIORn data hold	(min)		t_6	0	0	0	0	0
DIORn data high impedance state	(max)	(Note 2, 4)	t_{6z}	30	30	30	30	30
DIORn / DIOWn to address valid hold	(min)	(Note 4)	t_9	20	15	10	10	10
Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	(Note 4)	t_{RD}	0	0	0	0	0
IORDY Setup time		(Note 3, 4)	t_A	35	35	35	35	35
IORDY Pulse Width	(max)	(Note 4)	t_B	1250	1250	1250	1250	1250
IORDY assertion to release	(max)		t_C	5	5	5	5	5
DIOWn assert to data valid	(max)		t_{DDV}	10	10	10	10	10

Note: 1. t_0 is the minimum total cycle time, t_2 is the minimum DIORn / DIOWn assertion time, and t_{2i} is the minimum DIORn / DIOWn negation time. A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2. This parameter specifies the time from the negation edge of DIORn to the time that the data bus is released by the device.

3. The delay from the activation of DIORn or DIOWn until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIORn or DIOWn, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIORn or DIOWn, then t_{RD} shall be met and t_5 is not applicable.

4. Timings based upon software control. See User's Guide.

5. ATA / ATAPI standards prior to ATA / ATAPI-5 inadvertently specified an incorrect value for mode 2 time t_0 by utilizing the 16-bit PIO value.

6. All IDE timing is based upon HCLK = 100 MHz.

PIO Data Transfers

Parameter			Symbol	Mode 0 (in ns)	Mode 1 (in ns)	Mode 2 (in ns)	Mode 3 (in ns)	Mode 4 (in ns)
Cycle time	(min)	(Note 1, 4)	t_0	600	383	240	180	120
Address valid to DIORn / DIOWn setup	(min)	(Note 4)	t_1	70	50	30	30	25
DIORn / DIOWn 16-bit	(min)	(Note 1, 4)	t_2	165	125	100	80	70
DIORn / DIOWn recovery time	(min)	(Note 1, 4)	t_{2i}	-	-	-	70	25
DIOWn data setup	(min)	(Note 4)	t_3	60	45	30	30	20
DIOWn data hold	(min)		t_4	0	0	0	0	0
DIORn data setup	(min)		t_5	20	20	20	20	20
DIORn data hold	(min)		t_6	0	0	0	0	0
DIORn data high impedance state	(max)	(Note 2, 4)	t_{6z}	30	30	30	30	30
DIORn / DIOWn to address valid hold	(min)	(Note 4)	t_9	20	15	10	10	10
Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	(Note 4)	t_{RD}	0	0	0	0	0
IORDY Setup time		(Note 3, 4)	t_A	35	35	35	35	35
IORDY Pulse Width	(max)	(Note 4)	t_B	1250	1250	1250	1250	1250
IORDY assertion to release	(max)		t_C	5	5	5	5	5
DIOWn assert to data valid	(max)		t_{DDV}	10	10	10	10	10

Note: 1. t_0 is the minimum total cycle time, t_2 is the minimum DIORn / DIOWn assertion time, and t_{2i} is the minimum DIORn / DIOWn negation time. A host implementation shall lengthen t_2 and/or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2. This parameter specifies the time from the negation edge of DIORn to the time that the data bus is released by the device.

3. The delay from the activation of DIORn or DIOWn until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIORn or DIOWn, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIORn or DIOWn, then t_{RD} shall be met and t_5 is not applicable.

4. Timings based upon software control. See User's Guide.

5. All IDE timing is based upon HCLK = 100 MHz.

Table R. 352 Pin Diagram Dimensions

Symbol	dimension in mm			dimension in inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.20	2.30	2.50	0.087	0.092	0.098
A1	-	0.60	-	-	0.024	-
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	-	0.75	-	-	0.030	-
c	0.51	0.56	0.61	0.020	0.022	0.024
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	-	24.13	-	-	0.950	-
D2	23.80	24.00	24.20	0.937	0.945	0.953
D3	17.95	18.00	18.05	0.707	0.709	0.711
E	26.80	27.00	27.20	1.055	1.063	1.071
E1	-	24.13	-	-	0.950	-
E2	23.80	24.00	24.20	0.937	0.945	0.953
E3	17.95	18.00	18.05	0.707	0.709	0.711
e	-	1.27	-	-	0.050	-
ddd	-	-	0.15	-	-	0.006
q	30° TYP			30° TYP		

Note: 1. Controlling Dimension: Millimeter.
2. Primary Datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to Primary Datum C.
4. There shall be a minimum clearance of 0.25 mm between the edge of the solder ball and the body edge.
5. Reference Document: JEDEC MO-151, BAL-2

352 Pin BGA Pinout (Bottom View)

The following table shows the 352 pin BGA pinout. (For better understanding, compare the coordinates on the x and y axis on Figure 40, "352 PIN BGA PINOUT", on page 57 with Figure 40, "352 Pin PBGA Pin Diagram", on page 55.

- VDD_core is CVDD.
- VDD_ring is RVDD.
- All core and ring grounds are connected together and are labelled GND.
- Other special power requirements are clearly labelled (i.e. H18=ADC_VDD and H19=ADC_GND).
- NC means that the pin is not connected.

Pin List

The following Plastic Ball Grid Array (PBGA) ball assignment table is sorted in order of ball.

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	CSN[7]	E9	RVDD	L3	DA[16]	T13	CVDD
A2	DA[28]	E10	GND	L4	DA[15]	T14	GND
A3	AD[18]	E11	GND	L5	GND	T15	INT[0]
A4	DD[8]	E12	RVDD	L8	GND	T16	USBM[1]
A5	DD[4]	E13	CVDD	L9	GND	T17	RXD[0]
A6	AD[17]	E14	CVDD	L10	GND	T18	TXD[2]
A7	RDN	E15	GND	L11	GND	T19	ROW[2]
A8	RXCLK	E16	ASDI	L12	GND	T20	ROW[4]
A9	MIIRXD[0]	E17	DIOWN	L13	GND	U1	AD[0]
A10	RXDVAL	E18	EGPIO[0]	L16	CVDD	U2	P[15]
A11	MIITXD[2]	E19	EGPIO[3]	L17	COL[5]	U3	P[10]
A12	TXERR	E20	EGPIO[5]	L18	COL[7]	U4	P[7]
A13	CLD	F1	SDCSN[3]	L19	RSTON	U5	P[6]
A14	VS2	F2	DA[22]	L20	PRSTN	U6	P[4]
A15	MCBVD1	F3	DA[24]	M1	AD[7]	U7	P[0]
A16	MCREGN	F4	AD[25]	M2	DA[14]	U8	AD[13]
A17	EGPIO[12]	F5	RVDD	M3	AD[6]	U9	DA[3]
A18	EGPIO[15]	F6	GND	M4	AD[5]	U10	DA[0]
A19	IOWRN	F7	CVDD	M5	CVDD	U11	DSRN
A20	MCRESETN	F14	CVDD	M8	GND	U12	BOOT[1]
B1	CSN[2]	F15	GND	M9	GND	U13	NC
B2	DA[31]	F16	GND	M10	GND	U14	SSPRX1
B3	DA[30]	F17	EGPIO[2]	M11	GND	U15	INT[1]
B4	DA[27]	F18	EGPIO[4]	M12	GND	U16	PWMOUT
B5	DD[7]	F19	EGPIO[6]	M13	GND	U17	USBM[0]
B6	DD[3]	F20	EGPIO[8]	M16	GND	U18	RXD[1]
B7	WRN	G1	SDCSN[0]	M17	COL[4]	U19	TXD[1]
B8	MDIO	G2	SDCSN[1]	M18	COL[3]	U20	ROW[1]
B9	MIIRXD[1]	G3	SDWEN	M19	COL[6]	V1	P[16]
B10	RXERR	G4	SDCLK	M20	CSN[0]	V2	P[11]
B11	MIITXD[1]	G5	RVDD	N1	DA[13]	V3	P[8]
B12	CRS	G6	RVDD	N2	DA[12]	V4	DD[15]
B13	VS1	G15	RVDD	N3	DA[11]	V5	DD[13]
B14	MCD1	G16	RVDD	N4	AD[3]	V6	P[1]
B15	MCBVD2	G17	EGPIO[7]	N5	CVDD	V7	AD[14]
B16	MCEHN	G18	EGPIO[9]	N6	CVDD	V8	AD[12]
B17	EGPIO[13]	G19	EGPIO[10]	N8	GND	V9	DA[2]
B18	MCRDN	G20	EGPIO[11]	N9	GND	V10	IDECS0N
B19	WAITN	H1	DQMN[3]	N10	GND	V11	IDEDA[2]
B20	TRSTN	H2	CASN	N11	GND	V12	TDI
C1	CSN[1]	H3	RASN	N12	GND	V13	GND
C2	CSN[3]	H4	SDCSN[2]	N13	GND	V14	ASYNC

The following section focuses on the EP9315 pin signals from two viewpoints - the pin usage and pad characteristics, and the pin multiplexing usage. The first table (Table S) is a summary of all the EP9315 pin signals. The second table (Table T) illustrates the pin signal multiplexing and configuration options.

Table S is a summary of the EP9315 pin signals, which illustrates the pad type and pad pull type (if any). The symbols used in the table are defined as follows. (Note: A blank box means Not Applicable (NA) or, for Pull Type, No Pull (NP).)

Under the Pad Type column:

- A - Analog pad
- P - Power pad
- G - Ground pad
- I - Pin is an input only
- I/O - Pin is input/output
- 4mA - Pin is a 4 mA output driver
- 8mA - Pin is an 8 mA output driver
- 12mA - Pin is an 12 mA output driver

See the text description for additional information about bi-directional pins.

Under the Pull Type Column:

- PU - Resistor is a pull up to the RVDD supply
- PD - Resistor is a pull down to the RGND supply

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Table S. Pin Descriptions

Pin Name	Block	Pad Type	Pull Type	Description
TCK	JTAG	I	PD	JTAG clock in
TDI	JTAG	I	PD	JTAG data in
TDO	JTAG	4ma		JTAG data out
TMS	JTAG	I	PD	JTAG test mode select
TRSTn	JTAG	I	PD	JTAG reset
BOOT[1:0]	System	I	PD	Boot mode select in
XTALI	PLL	A		Main oscillator input
XTALO	PLL	A		Main oscillator output
VDD_PLL	PLL	P		Main oscillator power, 1.8V
GND_PLL	PLL	G		Main oscillator ground
RTCXTALI	RTC	A		RTC oscillator input
RTCXTALO	RTC	A		RTC oscillator output
WRn	EBUS	4ma		SRAM Write strobe out
RDn	EBUS	4ma		SRAM Read / OE strobe out
WAITn	EBUS	I	PU	SRAM Wait in
AD[25:0]	EBUS	8ma		Shared Address bus out
DA[31:0]	EBUS	8ma	PU	Shared Data bus in/out
CSn[3:0]	EBUS	4ma	PU	Chip select out
CSn[7:6]	EBUS	4ma	PU	Chip select out
DQMn[3:0]	EBUS	8ma		Shared data mask out
SDCLK	SDRAM	8ma		SDRAM clock out
SDCLKEN	SDRAM	8ma		SDRAM clock enable out
SDCSn[3:0]	SDRAM	4ma		SDRAM chip selects out
RASn	SDRAM	8ma		SDRAM RAS out
CASn	SDRAM	8ma		SDRAM CAS out
SDWEn	SDRAM	8ma		SDRAM write enable out
P[17:0]	Raster	4ma	PU	Pixel data bus out

Table S. Pin Descriptions *(Continued)*

Pin Name	Block	Pad Type	Pull Type	Description
SPCLK	Raster	12ma	PU	Pixel clock in/out
HSYNC	Raster	8ma	PU	Horizontal synchronization / line pulse out
V_CSYNC	Raster	8ma	PU	Vertical or composite synchronization / frame pulse out
BLANK	Raster	8ma	PU	Composite blanking signal out
BRIGHT	Raster	4ma		PWM brightness control out
PWMOUT	PWM	8ma		Pulse width modulator output
Xp, Xm	ADC	A		Touchscreen ADC X axis
Yp, Ym	ADC	A		Touchscreen ADC Y axis
sXp, sXm	ADC	A		Touchscreen ADC X axis feedback
sYp, sYm	ADC	A		Touchscreen ADC Y axis feedback
VDD_ADC	ADC	P		Touchscreen ADC power, 3.3V
GND_ADC	ADC	G		Touchscreen ADC ground
COL[7:0]	Key	8ma	PU	Key matrix column inputs
ROW[7:0]	Key	8ma	PU	Key matrix row outputs
USBp[2:0]	USB	A		USB positive signals
USBm[2:0]	USB	A		USB negative signals
TXD0	UART1	4ma		Transmit out
RXD0	UART1	I	PU	Receive in
CTSn	UART1	I	PU	Clear to send / transmit enable
DSRn	UART1	I	PU	Data set ready / Data Carrier Detect
DTRn	UART1	4ma		Data Terminal Ready output
RTSn	UART1	4ma		Ready to send
TXD1	UART2	4ma		Transmit / IrDA output
RXD1	UART2	I	PU	Receive / IrDA input
TXD2	UART3	4ma		Transmit
RXD2	UART3	I	PU	Receive
MDC	EMAC	4ma		Management data clock

Acronyms and Abbreviations

The following tables list abbreviations and acronyms used in this data sheet.

Term	Definition
ADC	Analog-to-Digital Converter
ALT	Alternative
AMBA	Advanced Micro-controller Bus Architecture
ATAPI	ATA Packet Interface
CODEC	COder / DECoder
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	Direct-Memory Access
EBUS	External Memory Bus
EEPROM	Electronically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
FIFO	First In / First Out
FIQ	Fast Interrupt Request
FLASH	Flash memory
GPIO	General Purpose I/O
HDLC	High-level Data Link Control
I/F	Interface
I^2S	Inter-IC Sound
IC	Integrated Circuit
ICE	In-Circuit Emulator
IDE	Integrated Drive Electronics
IEEE	Institute of Electronics and Electrical Engineers
IrDA	Infrared Data Association
IRQ	Standard Interrupt Request
ISO	International Standards Organization
JTAG	Joint Test Action Group
LFSR	Linear Feedback Shift Register
MII	Media Independent Interface
MMU	Memory Management Unit
OHCI	Open Host Controller Interface
PHY	Ethernet PHYsical layer interface
PIO	Programmed I/O
RISC	Reduced Instruction Set Computer
SDMI	Secure Digital Music Initiative
SDRAM	Synchronous Dynamic RAM
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STA	Station - Any device that contains an IEEE 802.11 conforming Medium Access Control (MAC) and physical layer (PHY) interface to the wireless medium
TFT	Thin Film Transistor
TLB	Translation Lookaside Buffer
USB	Universal Serial Bus

Units of Measurement

Symbol	Unit of Measure
$^{\circ}C$	degree Celsius
Hz	Hertz = cycle per second
Kbps	Kilobits per second
kbyte	Kilobyte
kHz	KiloHertz = 1000 Hz
Mbps	Megabits per second
MHz	MegaHertz = 1,000 kHz
µA	microAmpere = 10^{-6} Ampere
µs	microsecond = 1,000 nanoseconds = 10^{-6} seconds
mA	milliAmpere = 10^{-3} Ampere
ms	millisecond = 1,000 microseconds = 10^{-3} seconds
mW	milliWatt = 10^{-3} Watts
ns	nanosecond = 10^{-9} seconds
pF	picoFarad = 10^{-12} Farads
V	Volt
W	Watt