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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-LQFP
Supplier Device Package	36-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f2h08au-eb-2e

■PWM: Multifrequency 12-bit PWM × 2 channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
- Noise rejection function (noise filter time constant selectable from 1 tCYC/32 tCYC/128 tCYC)

■Clock Output Function
- Can generate clock outputs with a frequency of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock selected as the system clock.
- Can generate the source clock for the subclock

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts
- 20 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 128levels (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits
- Internal oscillation circuits
  Low-speed RC oscillation circuit : For system clock (100kHz)
  Medium-speed RC oscillation circuit : For system clock (1MHz)
  Multifrequency RC oscillation circuit : For system clock (8MHz)
- External oscillation circuits
  Hi-speed CF oscillation circuit: For system clock, with internal Rf
  Low speed crystal oscillation circuit: For low-speed system clock, with internal Rf
  1) The CF and crystal oscillation circuits share the same pins. The active circuit is selected under program control.
  2) Both the CF and crystal oscillator circuits stop operation on a system reset. When the reset is released, only the CF oscillation circuit resumes operation.

■System Clock Divider Function
- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■Internal reset function
- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

■Standby Function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are three ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC and crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
     * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0.
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF and RC oscillator automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) System resetting by watchdog timer or low-voltage detection.
     (3) Having an interrupt source established at either INT0, INT1, INT2, INT4 or INT5
     * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0.
     (5) Having an interrupt source established in the base timer circuit.
     Note: Available only when X'tal oscillation is selected.

■Onchip Debugger
- Supports software debugging with the IC mounted on the target board.
- Two channels of on-chip debugger pins are available to be compatible with small pin count devices.
  DBGP0 (P0), DBGP1 (P1)

■Data Security Function (flash versions only)
- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■Package Form
- QFP36 (7×7): Lead-free type

■Development Tools
- On-chip debugger: TCB87 type B + LC87F2H08A

■Programming Boards

Package	Programming boards
QFP36(7×7)	W87F24Q

■Flash ROM Programmer

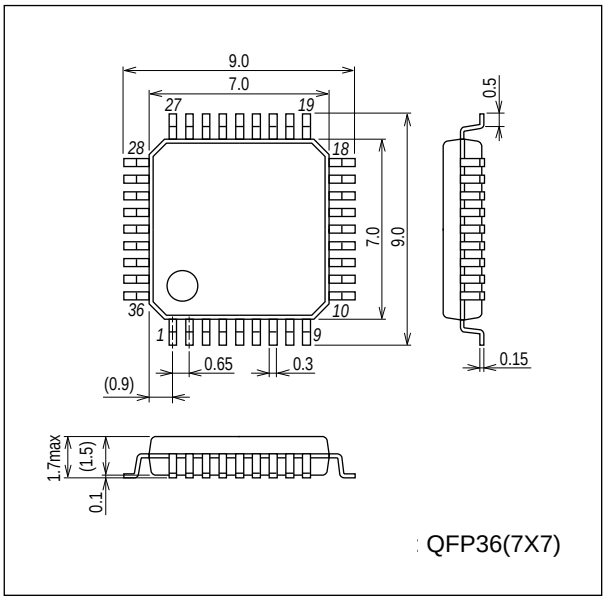
Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9708 AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev 02.72 or later	LC87F2H08A
	Gang Programmer	AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models)	-	-
		AF9833(Unit) (Including Ando Electric Co., Ltd. models)	-	-
Flash Support Group, Inc. (FSG) + Our company (Note 1)	In-circuit Programmer	AF9101/AF9103(Main body) (FSG models)	(Note 2)	LC87F2H08A
		SIB87(Inter Face Driver) (Our company model)		
Our company	Single/Gang Programmer	SKK/SKK Type B (SANYO FWS)	Application Version 1.04 or later Chip Data Version 2.10 or later	LC87F2H08A
	In-circuit/Gang Programmer	SKK-DBG Type B (SANYO FWS)		

For information about AF-Series:
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

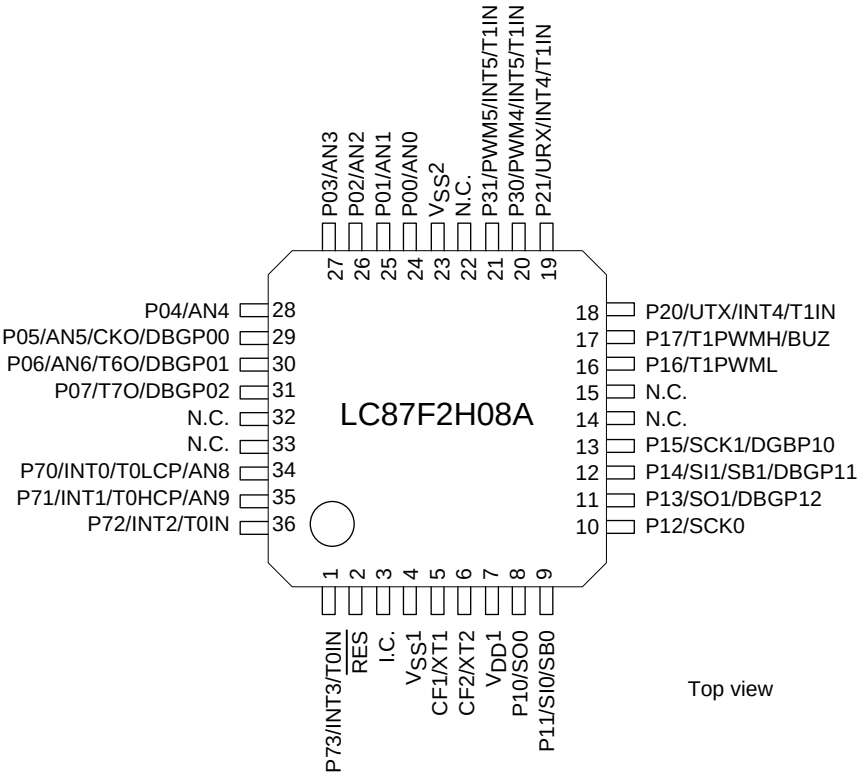
Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87) together
can give a PC-less, standalone on-board-programming capabilities.
Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or Our company for the information.

Package Dimensions

unit : mm (typ)
3162C



Pin Assignment



Top view

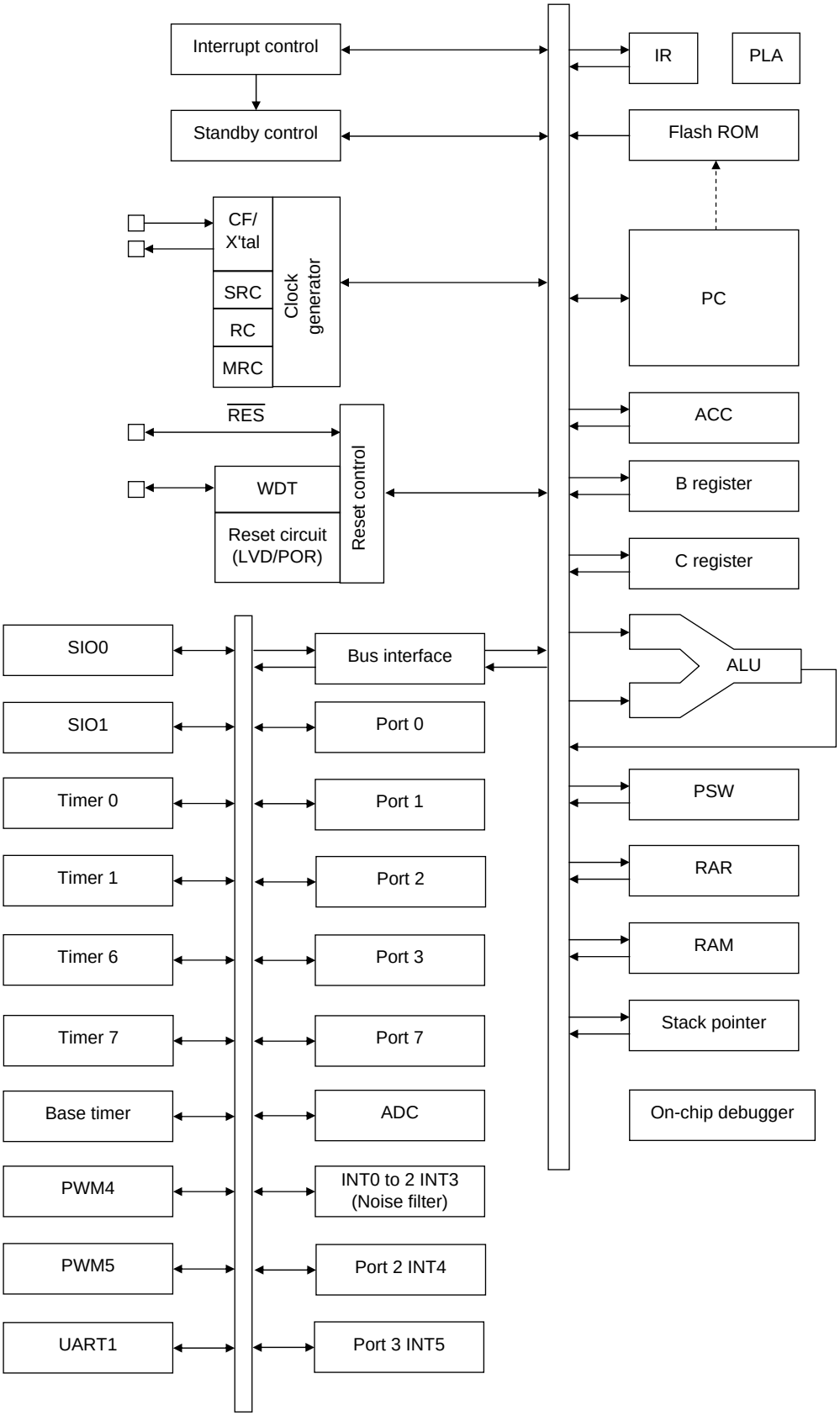
QFP36 (7×7) “Lead-free Type”

QFP36	NAME
1	P73/INT3/T0IN
2	$\overline{\text{RES}}$
3	I.C.
4	$V_{SS}1$
5	CF1/XT1
6	CF2/XT2
7	$V_{DD}1$
8	P10/SO0
9	P11/SI0/SB0
10	P12/SCK0
11	P13/SO1/DBGP12
12	P14/SI1/SB1/DBGP11
13	P15/SCK1/DBGP10
14	N.C.
15	N.C.
16	P16/T1PWML
17	P17/T1PWMH/BUZ
18	P20/UTX/INT4/T1IN

QFP36	NAME
19	P21/URX/INT4/T1IN
20	P30/PWM4/INT5/T1IN
21	P31/PWM5/INT5/T1IN
22	N.C.
23	$V_{SS}2$
24	P00/AN0
25	P01/AN1
26	P02/AN2
27	P03/AN3
28	P04/AN4
29	P05/AN5/CKO/DBGP00
30	P06/AN6/T6O/DBGP01
31	P07/T7O/DBGP02
32	N.C.
33	N.C.
34	P70/INT0/T0LCP/AN8
35	P71/INT1/T0HCP/AN9
36	P72/INT2/T0IN

Note I.C. and N.C. pins must be held open (disconnected).

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$,$V_{SS}2$</td><td>-</td><td>- power supply pins</td><td>No</td></tr>
<tr><td>$V_{DD}1$</td><td>-</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistors can be turned on and off in 4-bit units.
• HOLD reset input
• Port 0 interrupt input
• Pin functions
P05: System clock output
P06: Timer 6 toggle output
P07: Timer 7 toggle output
P00(AN0) to P06(AN6):AD converter input
P05(DBGP00) to P07(DBGP02):On-chip debugger 0 port</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/beeper output
P15(DBGP10) to P13(DBGP12):On-chip debugger 1 port</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P21</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P20: UART transmit
P21: UART receive
P20 to P21: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P31</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P30: PWM4 output
P31: PWM5 output
P30 to P31: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD reset input/timer 0H capture input
P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input
P73: INT3 input (input with noise filter)/timer 0 event input/timer 0H capture input
P70(AN8),P71(AN9) : AD converter input
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset Input/internal reset output</td><td>No</td></tr>
<tr><td>CF1/XT1</td><td>I</td><td>• Ceramic resonator or 32.768kHz crystal oscillator input pin
• Pin function
General-purpose input port</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>I/O</td><td>• Ceramic resonator or 32.768kHz crystal oscillator output pin
• Pin function
General-purpose input port</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P21	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P31	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

Note: Be sure to electrically short-circuit between the $V_{SS}1$ and $V_{SS}2$ pins.

User Option Table

Option Name	Option to be Applied on	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	O	1 bit	CMOS
				Nch-open drain
	P10 to P17	O	1 bit	CMOS
				Nch-open drain
	P20 to P21	O	1 bit	CMOS
				Nch-open drain
	P30 to P31	O	1 bit	CMOS
				Nch-open drain
Program start address	-	O	-	00000h
				01E00h
Low-voltage detection reset function	Detect function	O	-	Enable:Use
				Disable:Not Used
	Detect level	O	-	7-level
Power-on reset function	Power-On reset level	O	-	8-level

Recommended Unused Pin Connections

Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P10 to P17	Open	Output low
P20 to P21	Open	Output low
P30 to P31	Open	Output low
P70 to P73	Open	Output low
CF1/XT1	Pulled low with a 100kΩ resistor or less	General-purpose input port
CF2/XT2	Pulled low with a 100kΩ resistor or less	General-purpose input port

On-chip Debugger pin connection requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 on-chip debugger installation manual" and "LC872000 series on-chip debugger pin connection requirements"

Note: Be sure to electrically short-circuit between the $V_{SS}1$ and $V_{SS}2$ pins.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$			-0.3		+6.5	V
Input voltage		V_I	CF1, CF2			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}	Ports 0, 1, 2, 3 Port 7			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-10			mA
		IOPH(2)	P71 to P73	Per 1 applicable pin		-5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3	CMOS output select Per 1 applicable pin		-7.5			
		IOMH(2)	P71 to P73	Per 1 applicable pin		-3			
	Total output current	ΣIOAH(1)	P71 to P73	Total of all applicable pins		-10			
		ΣIOAH(2)	P10 to P14	Total of all applicable pins		-20			
		ΣIOAH(3)	P15 to P17 Ports 0, 2, 3	Total of all applicable pins		-20			
		ΣIOAH(4)	Ports 0, 1, 2, 3	Total of all applicable pins		-25			
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Port 7	Per 1 applicable pin				10	
	Mean output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
		IOML(3)	Port 7	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Port 7	Total of all applicable pins				15	
		ΣIOAL(2)	Port 0	Total of all applicable pins				40	
		ΣIOAL(3)	P10 to P14	Total of all applicable pins				35	
		ΣIOAL(4)	Ports 1, 2, 3	Total of all applicable pins				40	
		ΣIOAL(5)	Ports 0, 1, 2, 3	Total of all applicable pins				70	
Power Dissipation		Pd max(1)	QFP36(7×7)	Ta=-40 to +85°C Package only				120	mW
		Pd max(2)		Ta=-40 to +85°C Package with thermal resistance board (Note 1-2)				275	
Operating ambient Temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6tmm, glass epoxy) is used.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1$	0.245µs ≤ tCYC ≤ 200µs		2.7		5.5	V
	$V_{DD}(2)$		0.294µs ≤ tCYC ≤ 200µs		2.2		5.5	
	$V_{DD}(3)$		0.735µs ≤ tCYC ≤ 200µs		1.8		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 3, P71 to P73 P70 port input/ interrupt side		1.8 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(2)$	Ports 0		1.8 to 5.5	$0.3V_{DD}+0.7$		V_{DD}	
	$V_{IH}(3)$	Port 70 watchdog timer side		1.8 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	CF1, $\overline{RES}$		1.8 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3, P71 to P73 P70 port input/ interrupt side		4.0 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Ports 0		4.0 to 5.5	V_{SS}		$0.15V_{DD}+0.4$	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Port 70 watchdog timer side		1.8 to 5.5	V_{SS}		$0.8V_{DD}-1.0$	
	$V_{IL}(4)$	CF1, $\overline{RES}$		1.8 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-1)	tCYC (Note 2-2)			2.7 to 5.5	0.245		200	µs
				2.2 to 5.5	0.294		200	
				1.8 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	2.7 to 5.5	0.1		12	MHz
				1.8 to 5.5	0.1		4	
			• CF2 pin open • System clock frequency division ratio=1/2 • External system clock duty=50±5%	3.0 to 5.5	0.2		24.4	
				2.0 to 5.5	0.2		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	10MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		10		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation. CF oscillation normal amplifier size selected. See Fig. 1. (CFLAMP=0)	1.8 to 5.5		4		
			4MHz ceramic oscillation. CF oscillation low amplifier size selected. (CFLAMP=1) See Fig. 1.	2.2 to 5.5		4		
	FmMRC		Frequency variable RC oscillation. 1/2 frequency division ration. (RCCTD=0) (Note 2-4)	2.7 to 5.5	7.44	8.0	8.56	
	FmRC		Internal medium-speed RC oscillation	1.8 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation	1.8 to 5.5	50	100	200	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	1.8 to 5.5		32.768		

Note 2-1: V_{DD} must be held greater than or equal to 2.2V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: When switching the system clock, allow an oscillation stabilization time of 100µs or longer after the multifrequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	1.8 to 5.5			1	µA
	$I_{IH}(2)$	CF1	$V_{IN}=V_{DD}$	1.8 to 5.5			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	1.8 to 5.5	-1			
	$I_{IL}(2)$	CF1	$V_{IN}=V_{SS}$	1.8 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2 P71 to P73	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.35mA	2.7 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$		I_{OH}=-0.15mA	1.8 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	Port 3	I_{OH}=-6mA	4.5 to 5.5	V_{DD}-1			
	$V_{OH}(5)$		I_{OH}=-1.4mA	2.7 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$		I_{OH}=-0.8mA	1.8 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.4mA	2.7 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=0.8mA	1.8 to 5.5			0.4	
	$V_{OL}(4)$	Port 7	I_{OL}=1.4mA	2.7 to 5.5			0.4	
	$V_{OL}(5)$		I_{OL}=0.8mA	1.8 to 5.5			0.4	
	$V_{OL}(6)$	P00, P01	I_{OL}=25mA	4.5 to 5.5			1.5	
	$V_{OL}(7)$		I_{OL}=4mA	2.7 to 5.5			0.4	
	$V_{OL}(8)$		I_{OL}=2mA	1.8 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$ When Port 0 selected low-impedance pull-up.	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			1.8 to 4.5	18	50	230	
	Rpu(3)	Port 0	$V_{OH}=0.9V_{DD}$ When Port 0 selected high-impedance pull-up.	1.8 to 5.5	100	210	400	
Hysteresis voltage	VHYS(1)	Ports 1, 2, 3, 7 $\overline{RES}$		2.7 to 5.5		$0.1V_{DD}$		V
	VHYS(2)			1.8 to 2.7		$0.07V_{DD}$		
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	1.8 to 5.5		10		pF

Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 5.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			µs
	Data hold time		thDI(1)				0.05			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-2)	1.8 to 5.5			(1/3)tCYC +0.08	
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-2)				1tCYC +0.08	
	Output clock		tdD0(3)		(Note 4-1-2)				(1/3)tCYC +0.08	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 5.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			µs
	Data hold time		thDI(2)				0.05			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5.	1.8 to 5.5			(1/3)tCYC +0.08	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P21), INT5(P30 to P31)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	1.8 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are nabled.	1.8 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	256			
	tPIL(5)	$\overline{RES}$	• Resetting is enabled.	1.8 to 5.5	200			µs

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = 0V$

<12bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Resolution	N	AN0(P00) to AN6(P06), AN8(P70), AN9(P71)		2.4 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±16	LSB
			(Note 6-1) • Ta=-10 to +50°C	2.4 to 3.6			±20	
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	µs
				3.0 to 5.5	64		115	
			• See Conversion time calculation formulas. (Note 6-2) • Ta=-10 to +50°C	2.4 to 3.6	410		425	
Analog input voltage range	VAIN			2.4 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.4 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	2.4 to 5.5	-1			

<8bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Resolution	N	AN0(P00) to AN6(P06) AN8(P70) AN9(P71)		2.4 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	2.4 to 5.5			±1.5	LSB
Conversion time	TCAD		• See Conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	20		90	µs
				3.0 to 5.5	40		90	
			• See Conversion time calculation formulas. (Note 6-2) • Ta=-10 to +50°C	2.4 to 3.6	250		265	
Analog input voltage range	VAIN			2.4 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	2.4 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	2.4 to 5.5	-1			

Conversion time calculation formulas:

12bits AD Converter Mode: TCAD(Conversion time) = ((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time) = ((32/(AD division ratio))+2)× (1/3)×tCYC

External oscillation (FmCF)	Operating supply voltage range (V_{DD})	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD) 12bit AD	8bit AD
CF-12MHz	4.0V to 5.5V	1/1	250ns	1/8	34.8µs	21.5µs
	3.0V to 5.5V	1/1	250ns	1/16	69.5µs	42.8µs
CF-10MHz	4.0V to 5.5V	1/1	300ns	1/8	41.8µs	25.8µs
	3.0V to 5.5V	1/1	300ns	1/16	83.4µs	51.4µs
CF-4MHz	3.0V to 5.5V	1/1	750ns	1/8	104.5µs	64.5µs
	2.4V to 3.6V	1/1	750ns	1/32	416.5µs	256.5µs

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(1)	$V_{DD}1$	• FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 5.5		7.4	13.0	mA
				2.7 to 3.6		4.4	8.1	
	IDDOP(2)		• CF1=24MHz external clock • System clock set to CF1 side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 5.5		9.7	16.2	
				3.0 to 3.6		5.3	8.7	
	IDDOP(3)		• FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 5.5		6.6	11.9	
				2.2 to 3.6		4.0	7.4	
	IDDOP(4)		• FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		2.9	6.5	
				1.8 to 3.6		2.2	4.2	
	IDDOP(5)		• CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	2.2 to 5.5		1.1	2.5	
				2.2 to 3.6		0.6	1.3	
	IDDOP(6)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		0.6	1.7	
				1.8 to 3.6		0.3	0.9	
	IDDOP(7)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low speed and medium speed RC oscillation stopped. • System clock set to 8MHz with frequency variable RC oscillation • 1/1 frequency division ratio	2.7 to 5.5		5.0	9.1	
				2.7 to 3.6		3.6	5.8	
	IDDOP(8)		• External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation sopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		75	370	µA
				1.8 to 3.6		46	192	
	IDDOP(9)		• External FsX'tal and FmCF oscillation stopped. • System clock set to internal low speed RC oscillation. • Internal medium speed RC oscillation sopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio • Ta=-10 to +50°C	5.0		75	176	
				3.3		46	115	
				2.5		35	85	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(10)	V_{DD}1	• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		38	139	µA
				1.8 to 3.6		15	66	
	IDDOP(11)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C	5.0		38	101	
				3.3		15	46	
				2.5		9.0	28	
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(1)	V_{DD}1	• HALT mode • FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 5.5		3.1	5.6	mA
				2.7 to 3.6		1.6	2.9	
	IDDHALT(2)		• HALT mode • CF1=24MHz external clock • System clock set to CF1 side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 5.5		4.9	8.6	
				3.0 to 3.6		2.3	3.8	
	IDDHALT(3)		• HALT mode • FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 5.5		2.7	5.3	
				2.2 to 3.6		1.4	2.6	
	IDDHALT(4)		• HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		1.4	3.5	
				1.8 to 3.6		0.7	1.3	
	IDDHALT(5)		• HALT mode • CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal low speed and medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio	2.2 to 5.5		0.7	1.8	
				2.2 to 3.6		0.3	0.7	
	IDDHALT(6)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low speed RC oscillation stopped. • System clock set to internal medium speed RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		0.4	1.1	
				1.8 to 3.6		0.2	0.5	

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

Continued on next page.

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

• CF oscillation normal amplifier size selected (CFLAMP=0)

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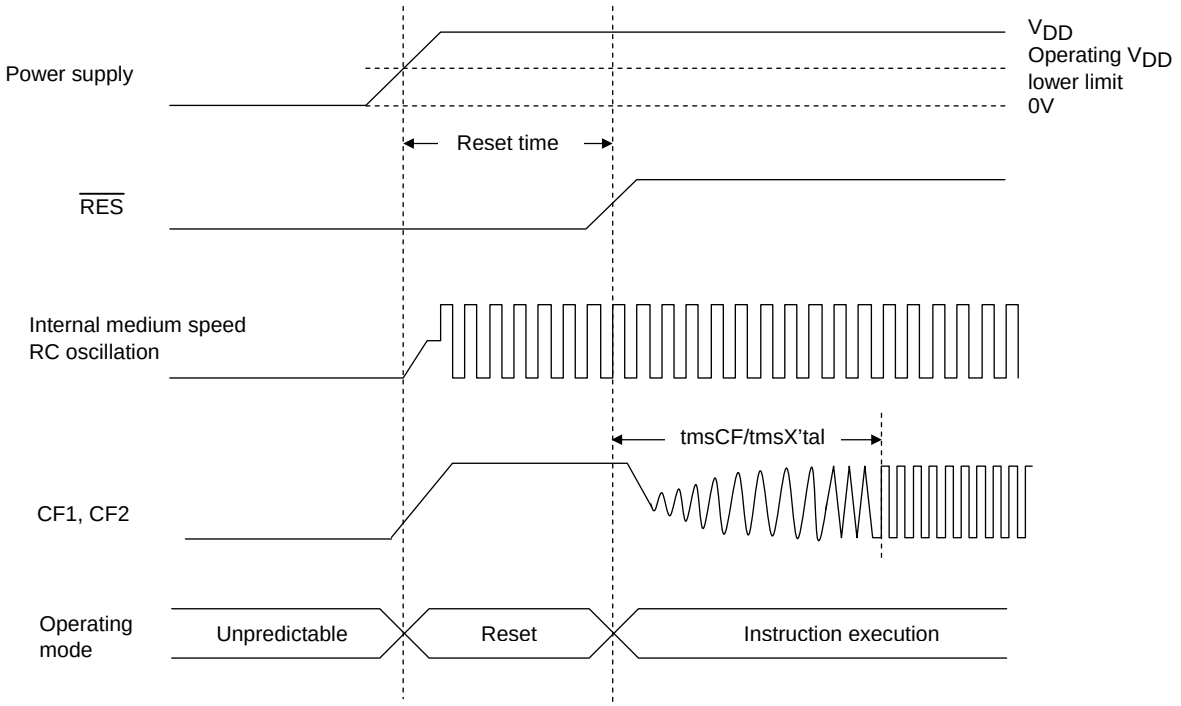
Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
12MHz	SMD	CSTCE12M0G52-R0	(10)	(10)	Open	1.0k	2.7 to 5.5	0.1	0.5	Internal C1,C2
10MHz	SMD	CSTCE10M0G52-R0	(10)	(10)	Open	680	2.2 to 3.6	0.1	0.5	
					Open	1.0k	2.3 to 5.5	0.1	0.5	
	LEAD	CSTLS10M0G53-B0	(15)	(15)	Open	1.0k	2.5 to 5.5	0.1	0.5	
8MHz	SMD	CSTCE8M00G52-R0	(10)	(10)	Open	1.5k	2.2 to 5.5	0.1	0.5	
	LEAD	CSTLS8M00G53-B0	(15)	(15)	Open	1.5k	2.2 to 5.5	0.1	0.5	
6MHz	SMD	CSTCR6M00G53-R0	(15)	(15)	Open	2.2k	2.2 to 5.5	0.1	0.5	
	LEAD	CSTLS6M00G53-B0	(15)	(15)	Open	2.2k	2.2 to 5.5	0.1	0.5	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	1.8 to 2.7	0.2	0.6	
					Open	3.3k	1.9 to 5.5	0.2	0.6	
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	3.3k	1.9 to 5.5	0.2	0.6	

• CF oscillation low amplifier size selected (CFLAMP=1)

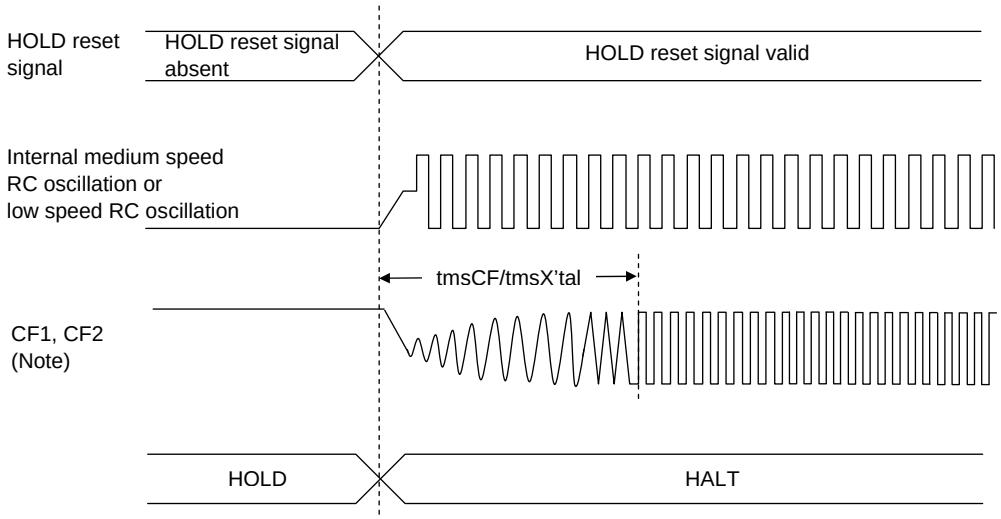
■MURATA

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		Typ [ms]	Max [ms]	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.0k	2.1 to 2.7	0.2	0.6	Internal C1,C2
					Open	2.2k	2.5 to 5.5	0.2	0.6	
		CSTCR4M00G53095-R0	(15)	(15)	Open	1.0k	1.9 to 2.7	0.2	0.7	
	LEAD	CSTLS4M00G53-B0	(15)	(15)	Open	1.0k	2.2 to 2.7	0.2	0.6	
					Open	2.2k	2.5 to 5.5	0.2	0.6	
		CSTLS4M00G53095-B0	(15)	(15)	Open	1.0k	2.0 to 2.7	0.2	0.7	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 3).



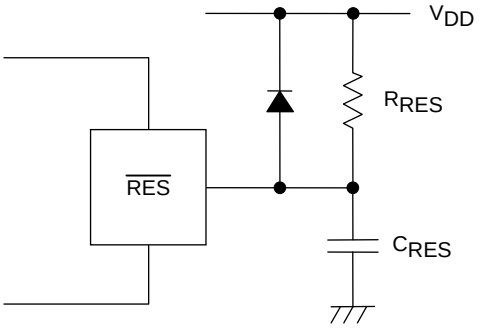
Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Note: External oscillation circuit is selected.

Figure 3 Oscillation Stabilization Times



Note:
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information..

Figure 4 Reset Circuit

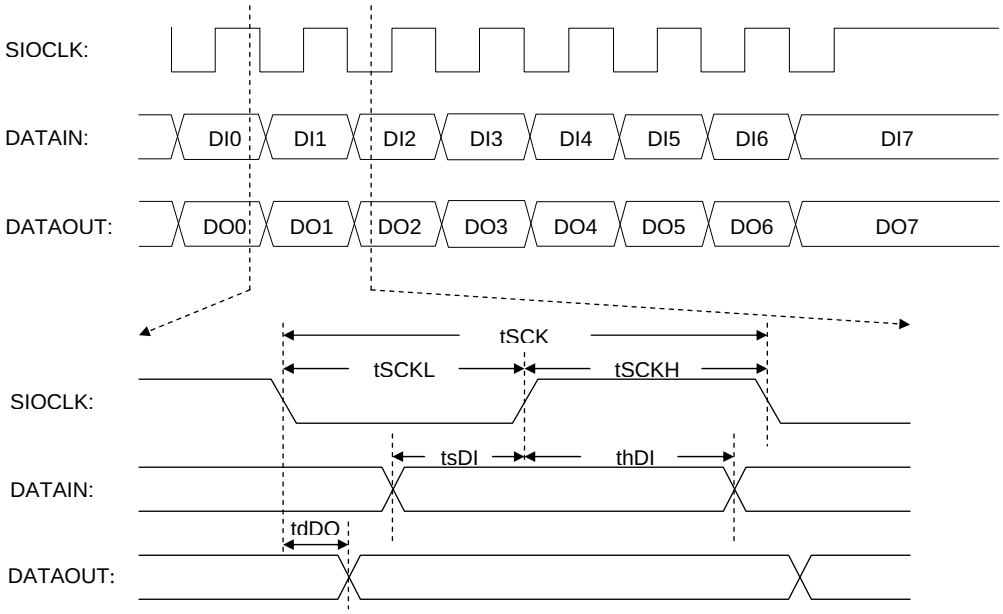


Figure 5 Serial I/O Output Waveforms

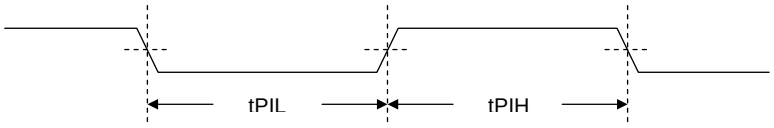


Figure 6 Pulse Input Timing Signal Waveform

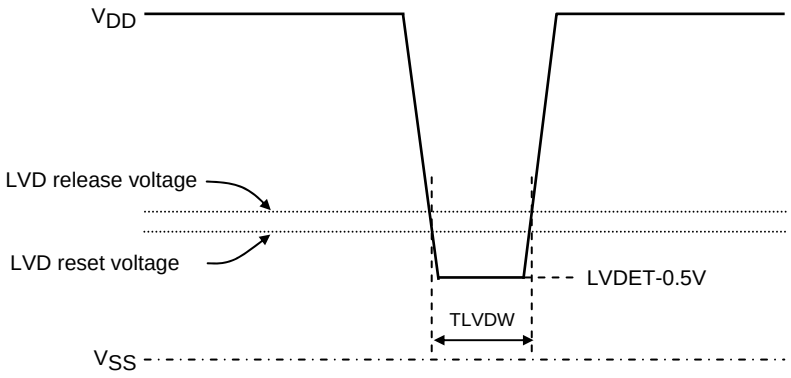


Figure 9 Low voltage detection minimum width
(Example of momentary power loss/Voltage variation waveform)