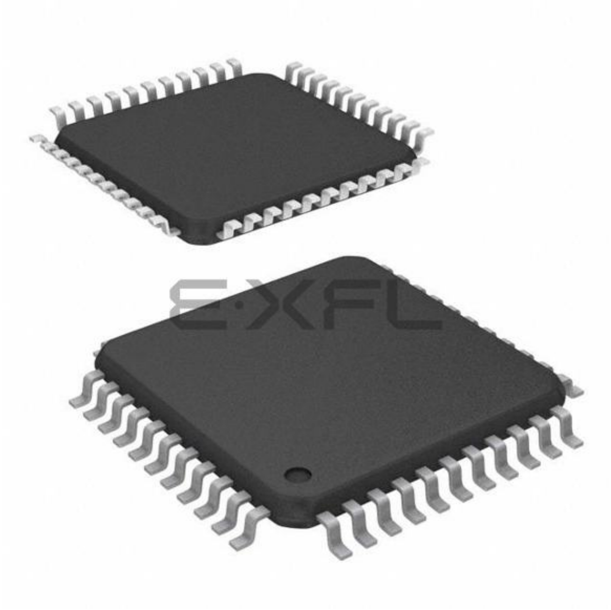


Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	37
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37032p44-125ac

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	388-Lead PBGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V					X		X	
CY37192V						X		X
CY37256V						X		X
CY37384V							X	X
CY37512V							X	X

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead CLCC	48-Lead FBGA	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	256-Lead FBGA	388-Lead PBGA	400-Lead FBGA
CY37032V	37		37											
CY37064V	37	37	37		69	69								
CY37128V				69	69	85	133							
CY37192V							125							
CY37256V							133	133	165		197	197		
CY37384V									165		197			
CY37512V									165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The PIM consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*® and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note *Understanding Bus-Hold—A Feature of Cypress CPLDs*.

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

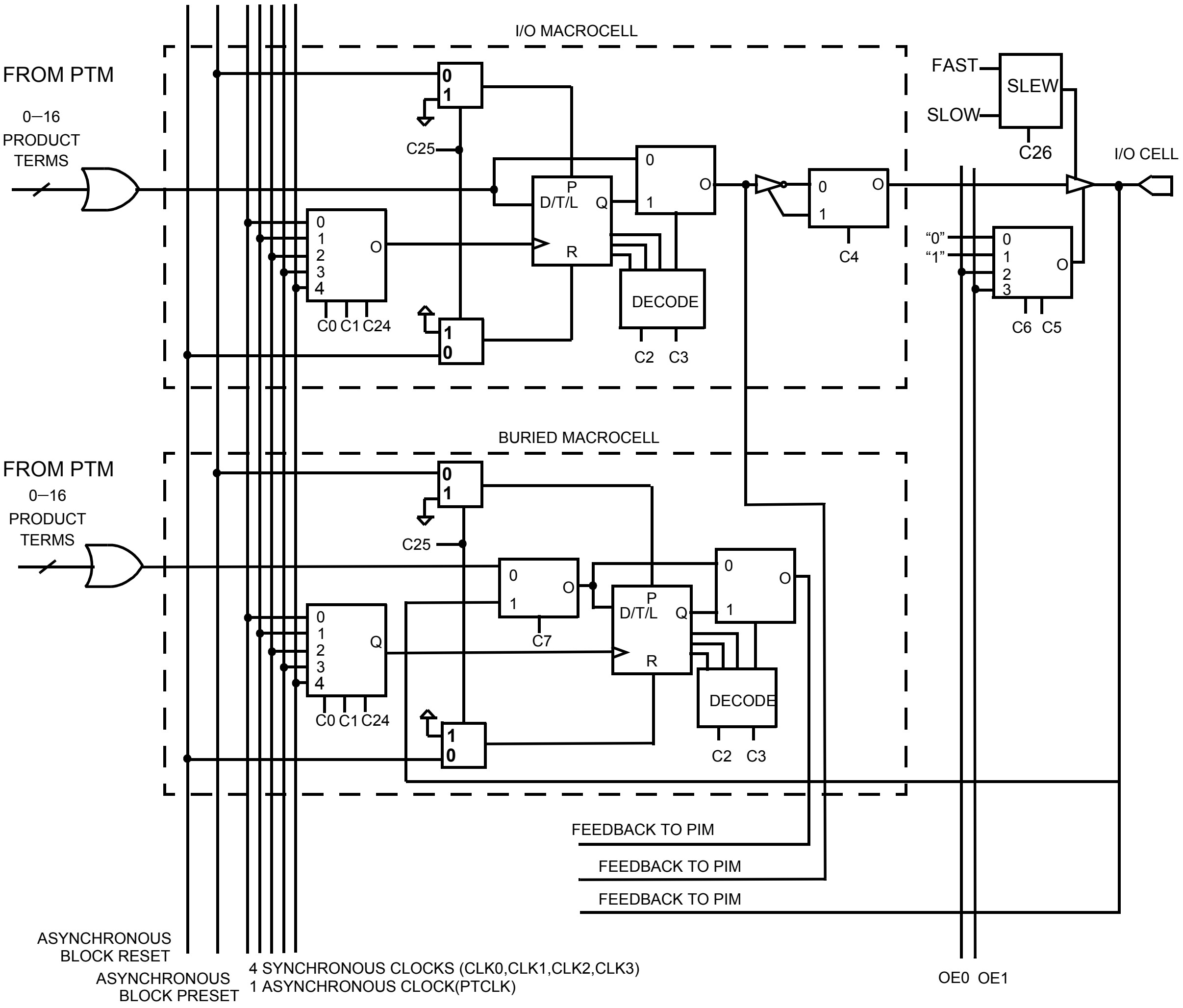


Figure 2. I/O and Buried Macrocells

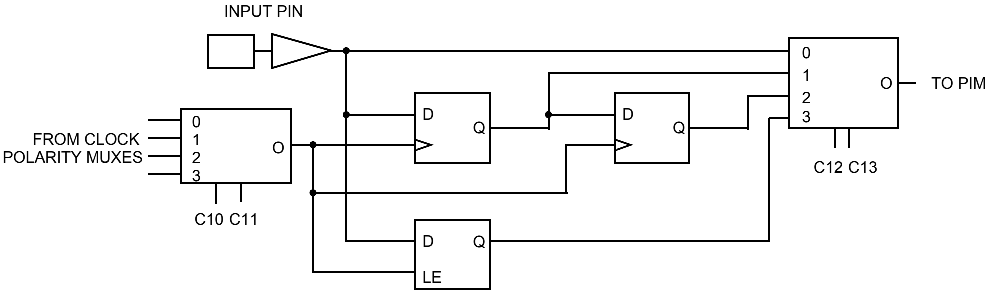


Figure 3. Input Macrocell

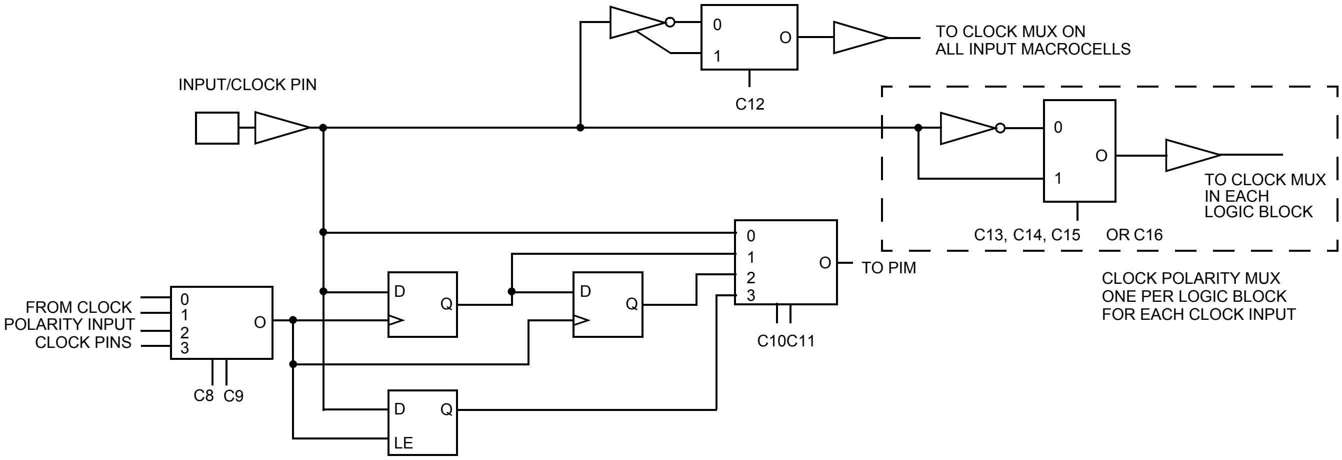


Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

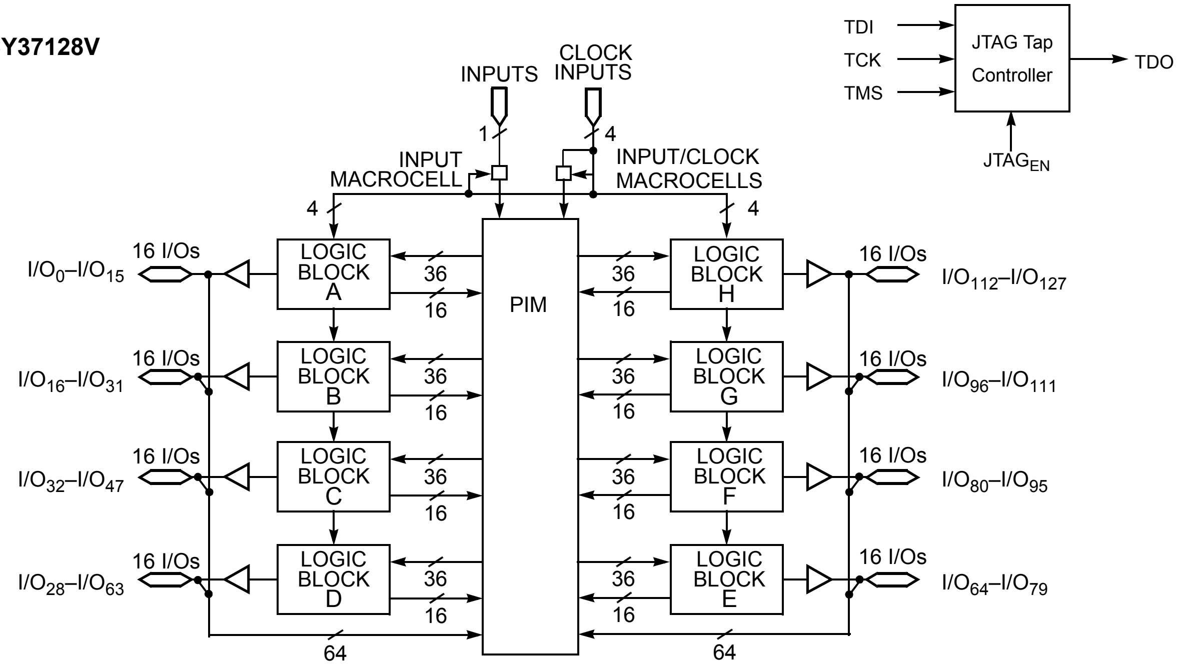
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

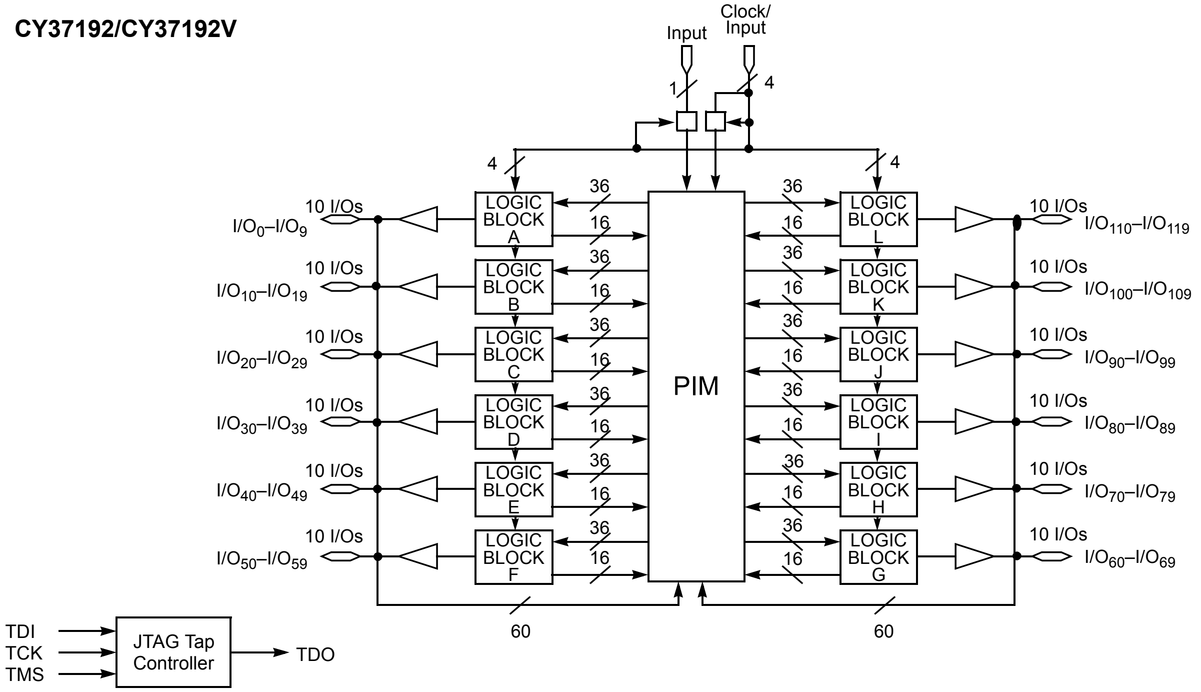
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams (continued)

CY37128/CY37128V



CY37192/CY37192V



Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual-Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

3.3V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State...–0.5V to +7.0V

DC Input Voltage ....–0.5V to +7.0V

DC Program Voltage.. 3.0 to 3.6V

Current into Outputs .... 8 mA

Static Discharge Voltage.. > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}[10]
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com’l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com’l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Notes:

[9] Dual pins are I/O with JTAG pins.

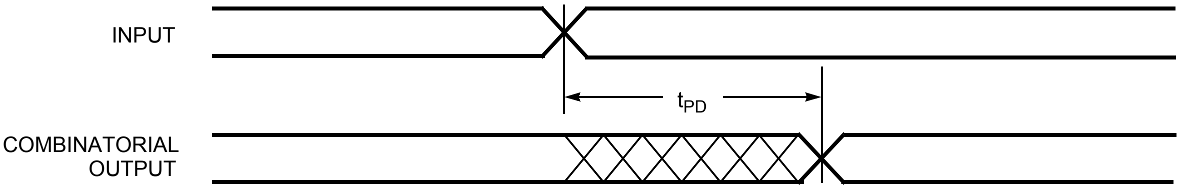
[10] For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V± 0.16V.

Switching Characteristics Over the Operating Range (continued)[12]

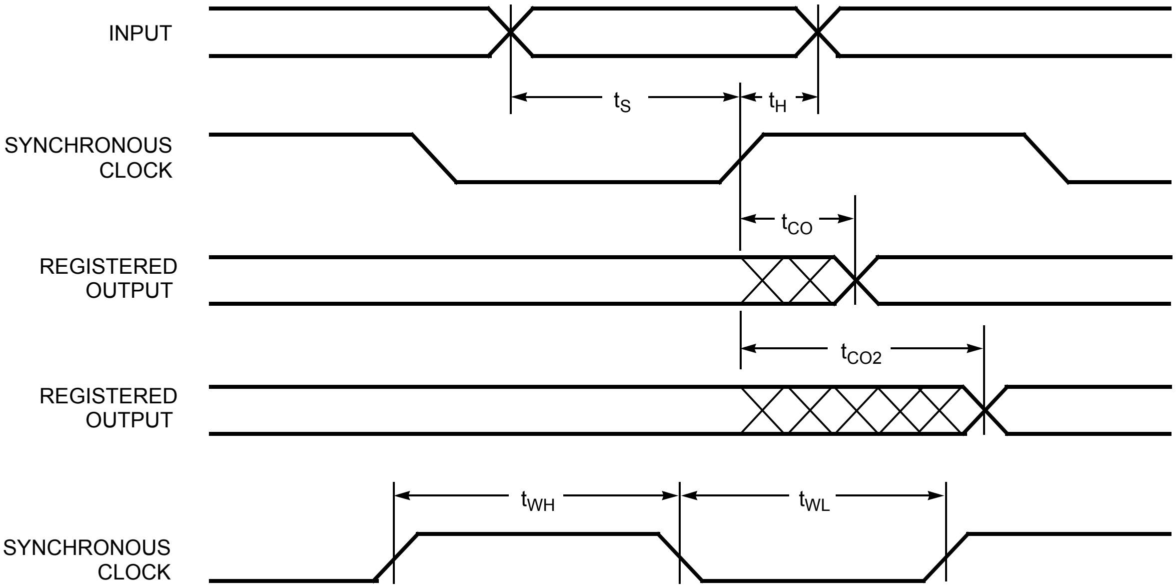
Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RO}[13, 14, 15]		12		13		13		14		15		18		21		26	ns
t_{PW}	8		8		8		8		10		12		15		20		ns
t_{PR}[13]	10		10		10		10		12		14		17		22		ns
t_{PO}[13, 14, 15]		12		13		13		14		15		18		21		26	ns
User Option Parameters																	
t_{LP}		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{SLEW}		3		3		3		3		3		3		3		3	ns
$t_{3.3IO}$[19]		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
JTAG Timing Parameters																	
$t_{S\ JTAG}$	0		0		0		0		0		0		0		0		ns
$t_{H\ JTAG}$	20		20		20		20		20		20		20		20		ns
$t_{CO\ JTAG}$		20		20		20		20		20		20		20		20	ns
f_{JTAG}		20		20		20		20		20		20		20		20	MHz

Switching Waveforms

Combinatorial Output



Registered Output with Synchronous Clocking

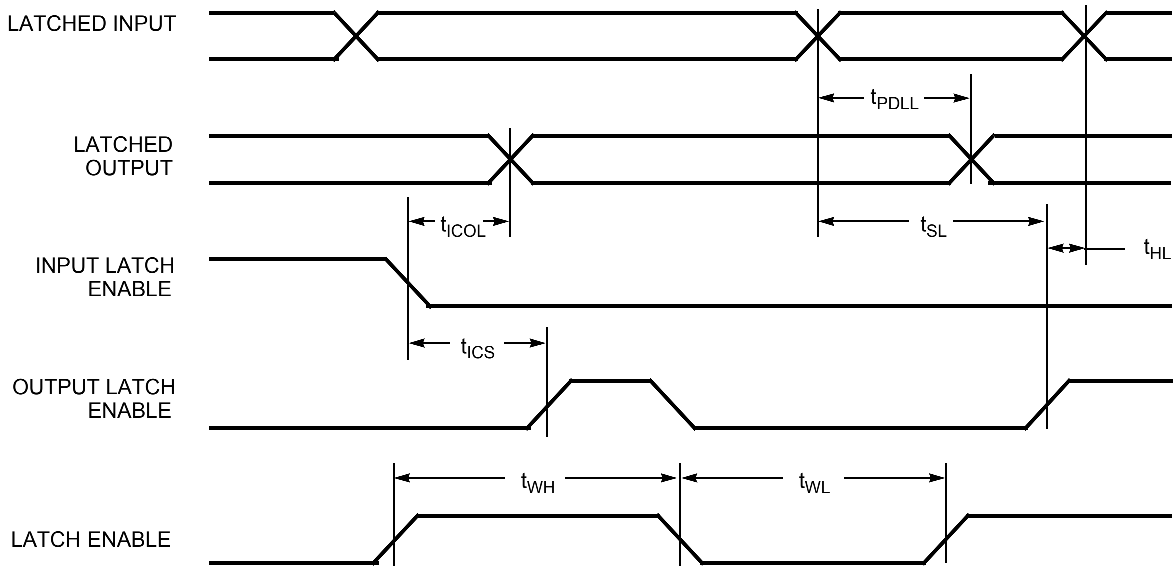


Note:

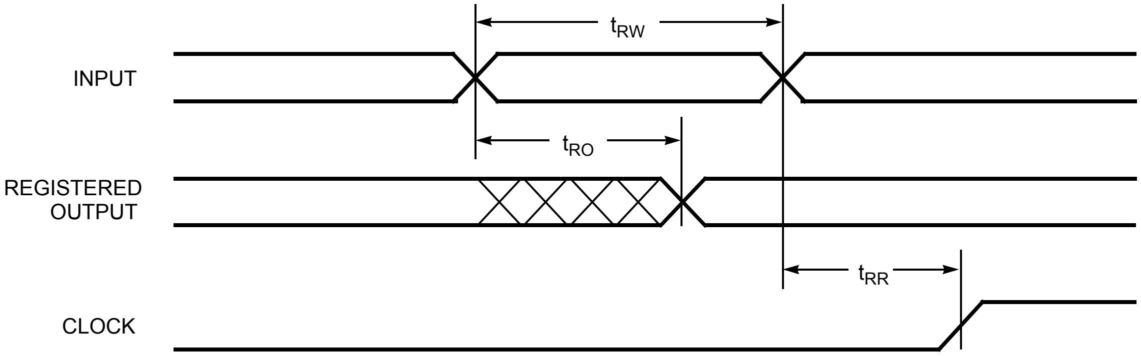
19. Only applicable to the 5V devices.

Switching Waveforms (continued)

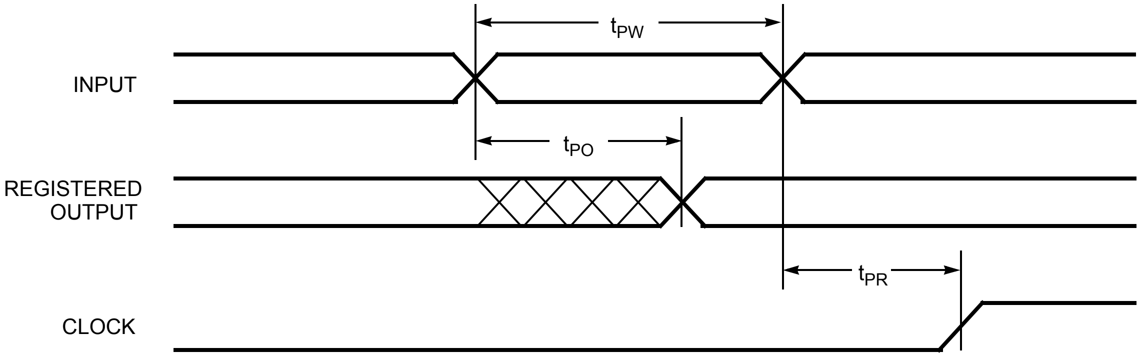
Latched Input and Output



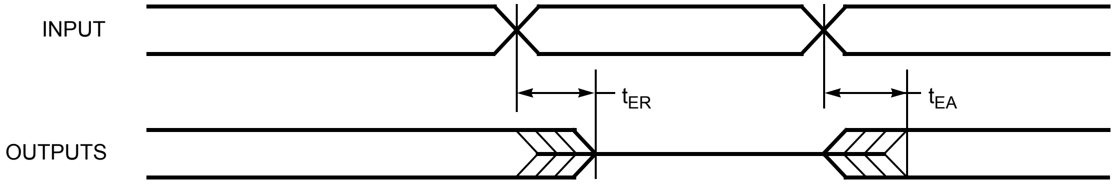
Asynchronous Reset



Asynchronous Preset

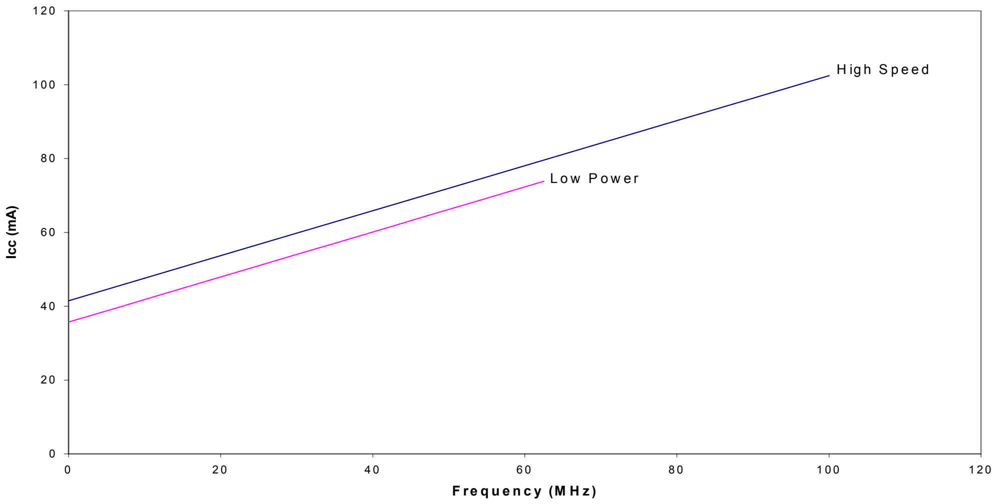


Output Enable/Disable



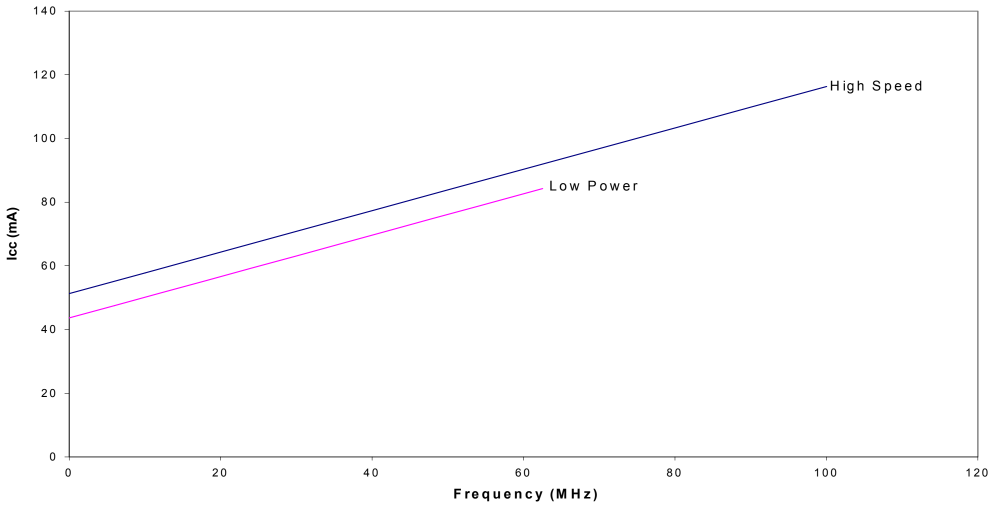
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

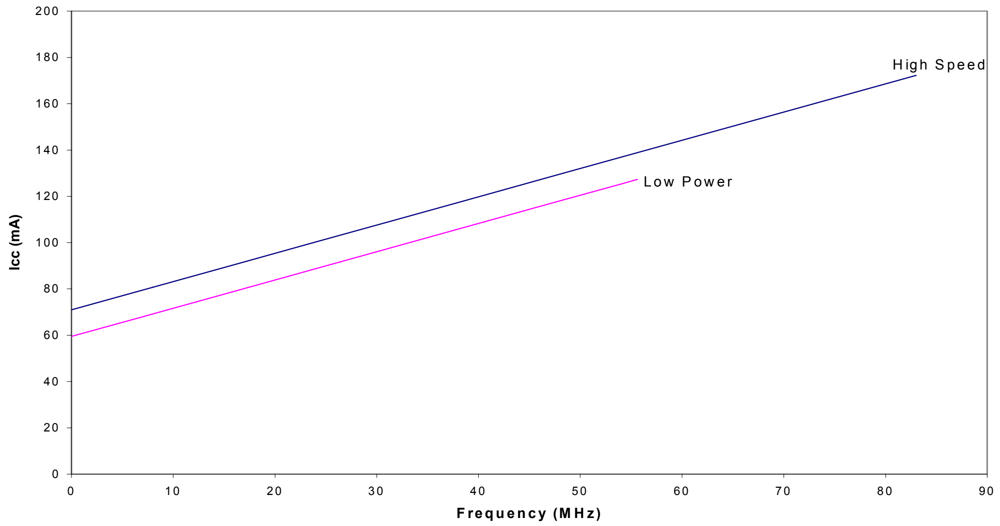
CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

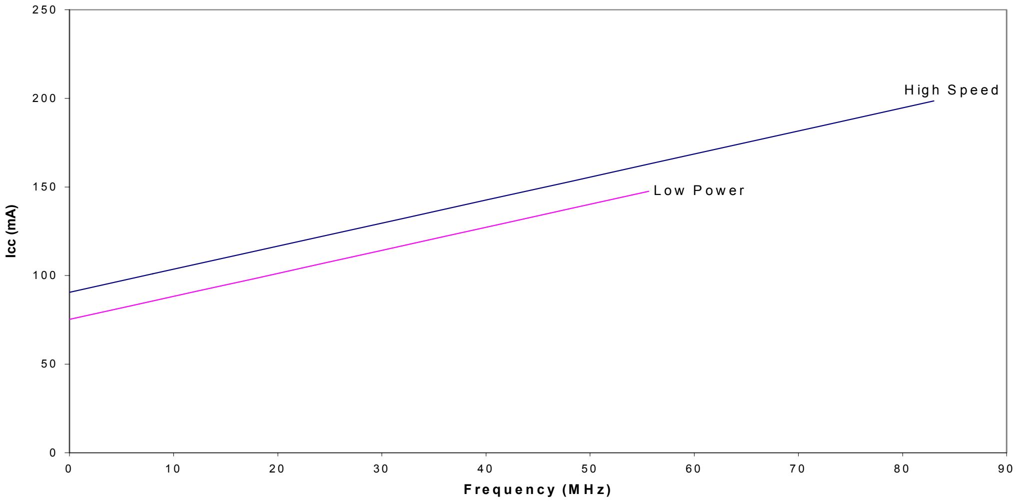
Typical 3.3V Power Consumption (continued)

CY37384V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

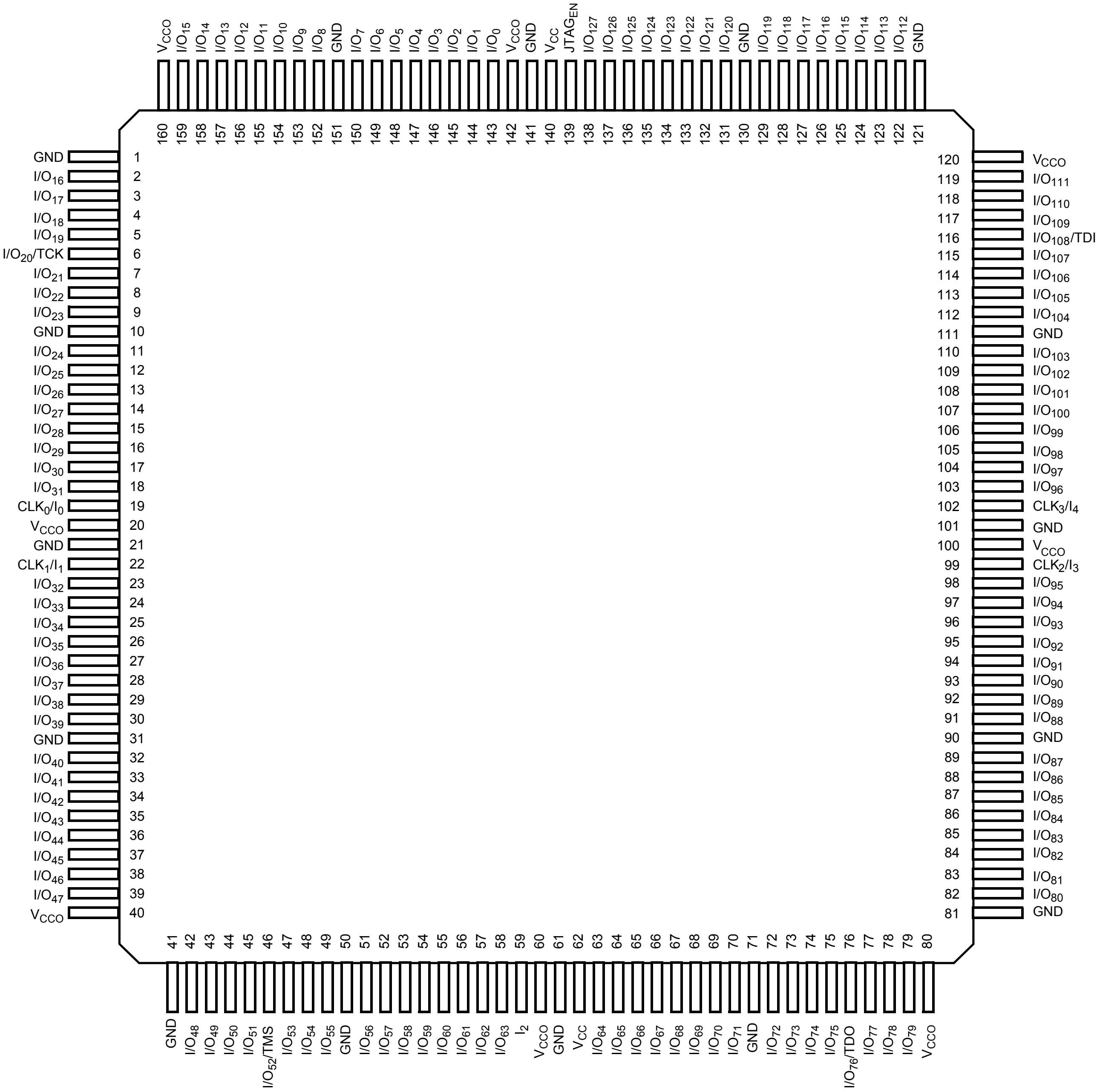
CY37512V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

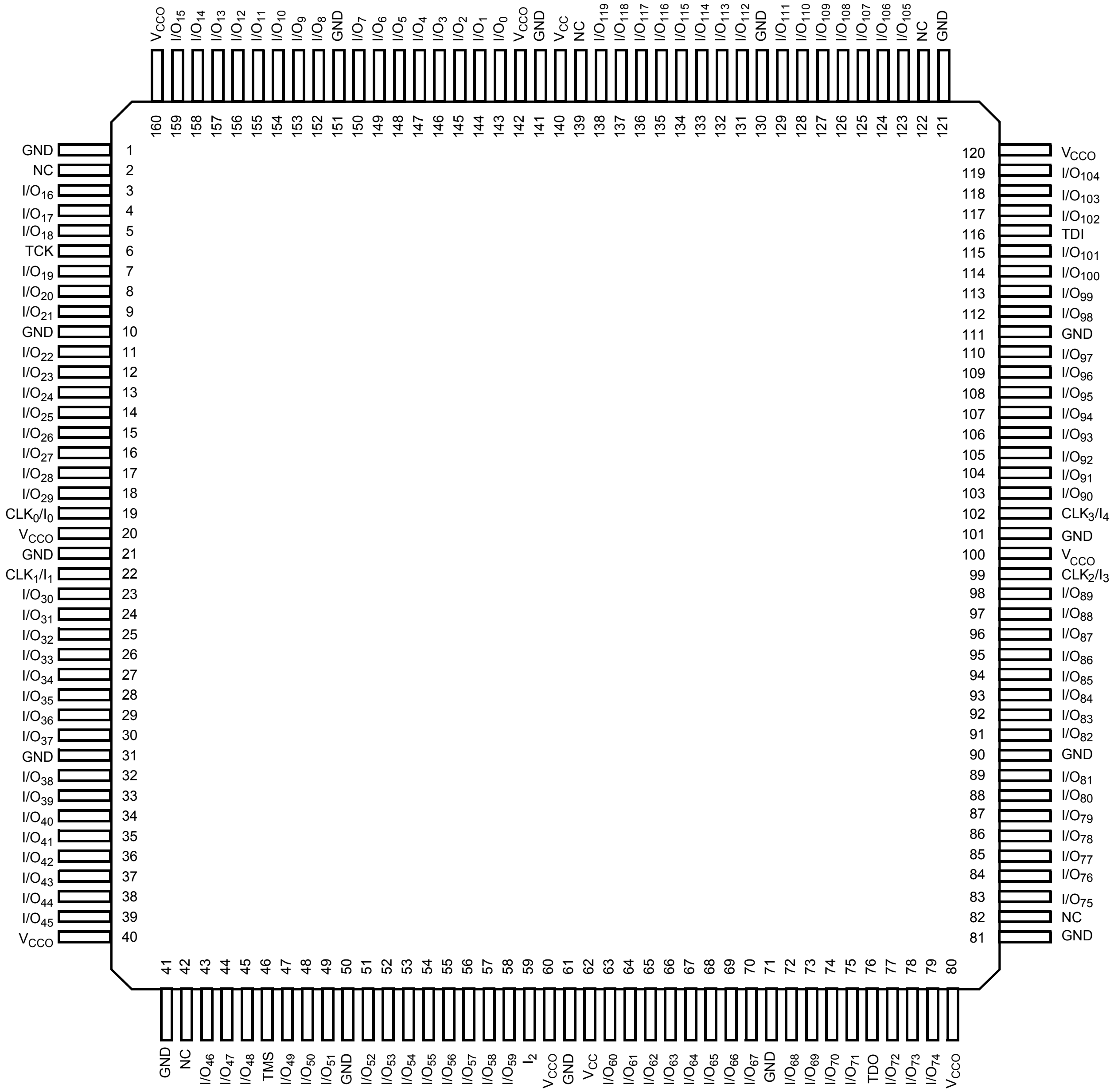
Pin Configurations[20] (continued)

160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View



Pin Configurations[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[20] (continued)

292-Ball PBGA (BG292)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O$_{21}$	NC	I/O$_{16}$	I/O$_{12}$	I/O$_{9}$	I/O$_{7}$	I/O$_{4}$	I/O$_{0}$	I/O$_{190}$	I/O$_{189}$	I/O$_{186}$	I/O$_{182}$	NC	I/O$_{178}$	I/O$_{175}$	NC	NC	I/O$_{169}$	I/O$_{168}$	A
B	I/O$_{23}$	I/O$_{20}$	I/O$_{19}$	I/O$_{18}$	I/O$_{15}$	I/O$_{11}$	I/O$_{8}$	I/O$_{5}$	I/O$_{1}$	I/O$_{191}$	I/O$_{187}$	I/O$_{185}$	I/O$_{181}$	NC	NC	I/O$_{174}$	I/O$_{171}$	I/O$_{170}$	NC	I/O$_{166}$	B
C	NC	NC	I/O$_{22}$	NC	I/O$_{17}$	I/O$_{14}$	I/O$_{10}$	I/O$_{6}$	I/O$_{2}$	NC	I/O$_{188}$	I/O$_{184}$	I/O$_{180}$	I/O$_{179}$	I/O$_{176}$	I/O$_{173}$	I/O$_{172}$	I/O$_{167}$	I/O$_{165}$	I/O$_{162}$	C
D	I/O$_{24}$	NC	NC	GND	NC	V$_{CCO}$	I/O$_{13}$	GND	I/O$_{3}$	NC	V$_{CC}$	I/O$_{183}$	GND	I/O$_{177}$	V$_{CCO}$	NC	GND	I/O$_{164}$	TDI	I/O$_{160}$	D
E	I/O$_{27}$	I/O$_{26}$	I/O$_{25}$	NC													I/O$_{163}$	I/O$_{161}$	I/O$_{159}$	I/O$_{156}$	E
F	I/O$_{30}$	TCK	I/O$_{28}$	V$_{CCO}$													V$_{CCO}$	I/O$_{158}$	NC	I/O$_{154}$	F
G	I/O$_{33}$	I/O$_{32}$	I/O$_{31}$	I/O$_{29}$													I/O$_{157}$	I/O$_{155}$	I/O$_{153}$	I/O$_{152}$	G
H	I/O$_{35}$	NC	I/O$_{34}$	GND				GND	GND	GND	GND	GND	GND				GND	I/O$_{151}$	I/O$_{150}$	I/O$_{149}$	H
J	I/O$_{39}$	I/O$_{38}$	I/O$_{37}$	I/O$_{36}$				GND	GND	GND	GND	GND	GND				I/O$_{148}$	I/O$_{147}$	I/O$_{146}$	I/O$_{145}$	J
K	I/O$_{42}$	I/O$_{40}$	I/O$_{41}$	V$_{CC}$				GND	GND	GND	GND	GND	GND				I/O$_{144}$	CLK$_{3}$/I$_{4}$	NC	NC	K
L	I/O$_{43}$	I/O$_{44}$	I/O$_{45}$	I/O$_{46}$				GND	GND	GND	GND	GND	GND				V$_{CC}$	CLK$_{2}$/I$_{3}$	I/O$_{143}$	NC	L
M	I/O$_{47}$	CLK$_{0}$/I$_{0}$	CLK$_{1}$/I$_{1}$	I/O$_{48}$				GND	GND	GND	GND	GND	GND				I/O$_{139}$	I/O$_{140}$	I/O$_{141}$	I/O$_{142}$	M
N	I/O$_{49}$	I/O$_{50}$	I/O$_{51}$	GND				GND	GND	GND	GND	GND	GND				GND	I/O$_{136}$	I/O$_{137}$	I/O$_{138}$	N
P	I/O$_{52}$	I/O$_{53}$	I/O$_{55}$	I/O$_{58}$													I/O$_{131}$	I/O$_{133}$	I/O$_{134}$	I/O$_{135}$	P
R	I/O$_{54}$	I/O$_{56}$	I/O$_{59}$	V$_{CCO}$													V$_{CCO}$	I/O$_{130}$	NC	I/O$_{132}$	R
T	I/O$_{57}$	I/O$_{60}$	I/O$_{62}$	I/O$_{65}$													I/O$_{124}$	I/O$_{127}$	I/O$_{128}$	I/O$_{129}$	T
U	I/O$_{61}$	I/O$_{63}$	I/O$_{66}$	GND	I/O$_{76}$	V$_{CCO}$	I/O$_{82}$	GND	I/O$_{91}$	V$_{CC}$	I/O$_{98}$	I/O$_{102}$	GND	I/O$_{112}$	V$_{CCO}$	NC	GND	I/O$_{123}$	I/O$_{122}$	I/O$_{126}$	U
V	I/O$_{64}$	I/O$_{67}$	I/O$_{69}$	I/O$_{75}$	I/O$_{78}$	I/O$_{81}$	I/O$_{85}$	I/O$_{88}$	I/O$_{92}$	I$_{2}$	I/O$_{97}$	I/O$_{101}$	I/O$_{105}$	I/O$_{109}$	I/O$_{113}$	TDO	I/O$_{114}$	I/O$_{117}$	I/O$_{121}$	I/O$_{125}$	V
W	I/O$_{68}$	I/O$_{70}$	I/O$_{72}$	I/O$_{74}$	I/O$_{79}$	I/O$_{83}$	I/O$_{86}$	I/O$_{89}$	I/O$_{93}$	I/O$_{95}$	I/O$_{96}$	I/O$_{100}$	I/O$_{104}$	I/O$_{107}$	I/O$_{110}$	NC	NC	I/O$_{115}$	I/O$_{118}$	I/O$_{120}$	W
Y	I/O$_{71}$	I/O$_{73}$	I/O$_{77}$	TMS	I/O$_{80}$	I/O$_{84}$	I/O$_{87}$	I/O$_{90}$	I/O$_{94}$	NC	NC	I/O$_{99}$	I/O$_{103}$	I/O$_{106}$	I/O$_{108}$	I/O$_{111}$	NC	NC	I/O$_{116}$	I/O$_{119}$	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Ordering Information

CY 37 512 V P400 - 83 BB X C

Cypress Semiconductor ID

Family Type
37 = Ultra37000 Family

Macrocell Density
32 = 32 Macrocells 256 = 256 Macrocells
64 = 64 Macrocells 384 = 384 Macrocells
128 = 128 Macrocells 512 = 512 Macrocells
192 = 192 Macrocells

Operating Reference Voltage
V = 3.3V Supply Voltage
(5.0V if not specified)

Pin Count
P44 = 44 Leads
P48 = 48 Leads
P84 = 84 Leads
P100 = 100 Leads
P160 = 160 Leads
P208 = 208 Leads
P256 = 256 Leads
P352 = 352 Leads
P400 = 400 Leads

Operating Conditions
Commercial 0°C to +70°C
Industrial -40°C to +85°C
Military -55°C to +125°C

Lead Free
X Lead Free

Package Type
A = Thin Quad Flat Pack (TQFP)
U = Ceramic Quad Flat Pack (CQFP)
N = Plastic Quad Flat Pack (PQFP)
NT = Thermally Enhanced Plastic Quad Flat Pack (EQFP)
J = Plastic Leaded Chip Carrier (PLCC)
Y = Ceramic Leaded Chip Carrier (CLCC)
BG = Plastic Ball Grid Array (PBGA)
BA = Fine-Pitch Ball Grid Array (FBGA) 0.8mm Lead Pitch
BB = Fine-Pitch Ball Grid Array (FBGA) 1.0mm Lead Pitch

Speed
200 = 200 MHz
167 = 167 MHz
154 = 154 MHz
143 = 143 MHz
125 = 125 MHz
100 = 100 MHz
83 = 83 MHz
66 = 66 MHz

5.0V Ordering Information

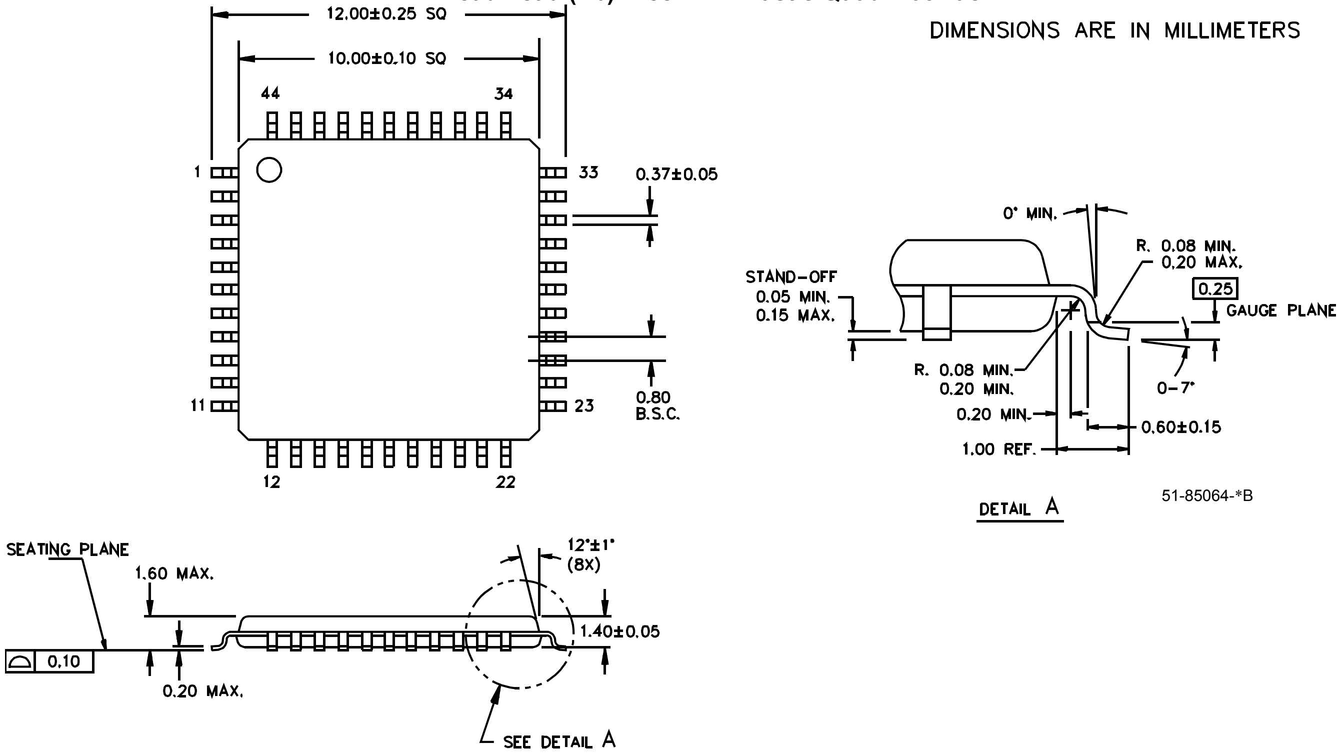
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	200	CY37032P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-200AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-200JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
	154	CY37032P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
	125	CY37032P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37032P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
64	200	CY37064P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-200AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-200JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-200JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-200AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-200AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	

3.3V Ordering Information (continued)

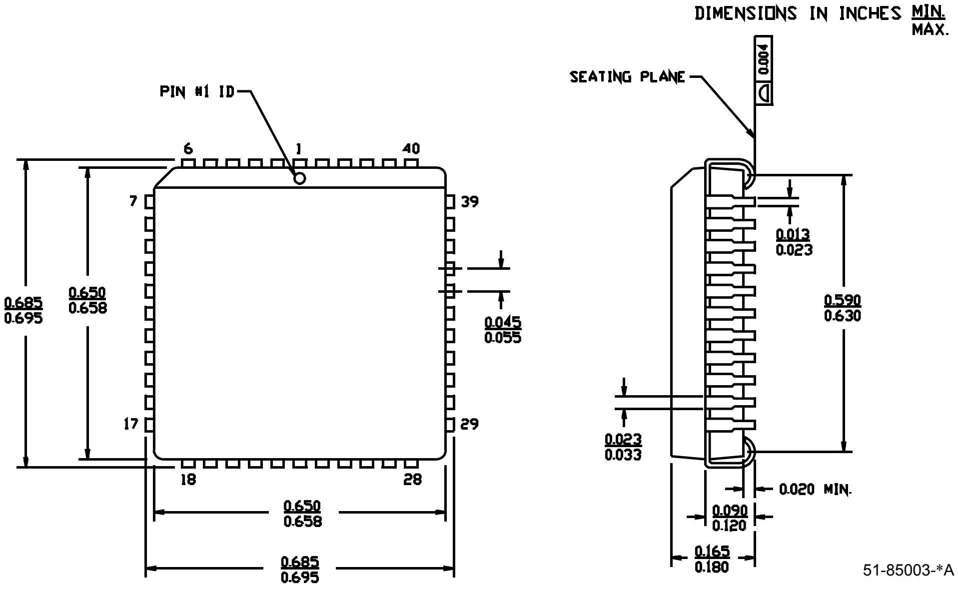
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

Package Diagrams

44-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack A44

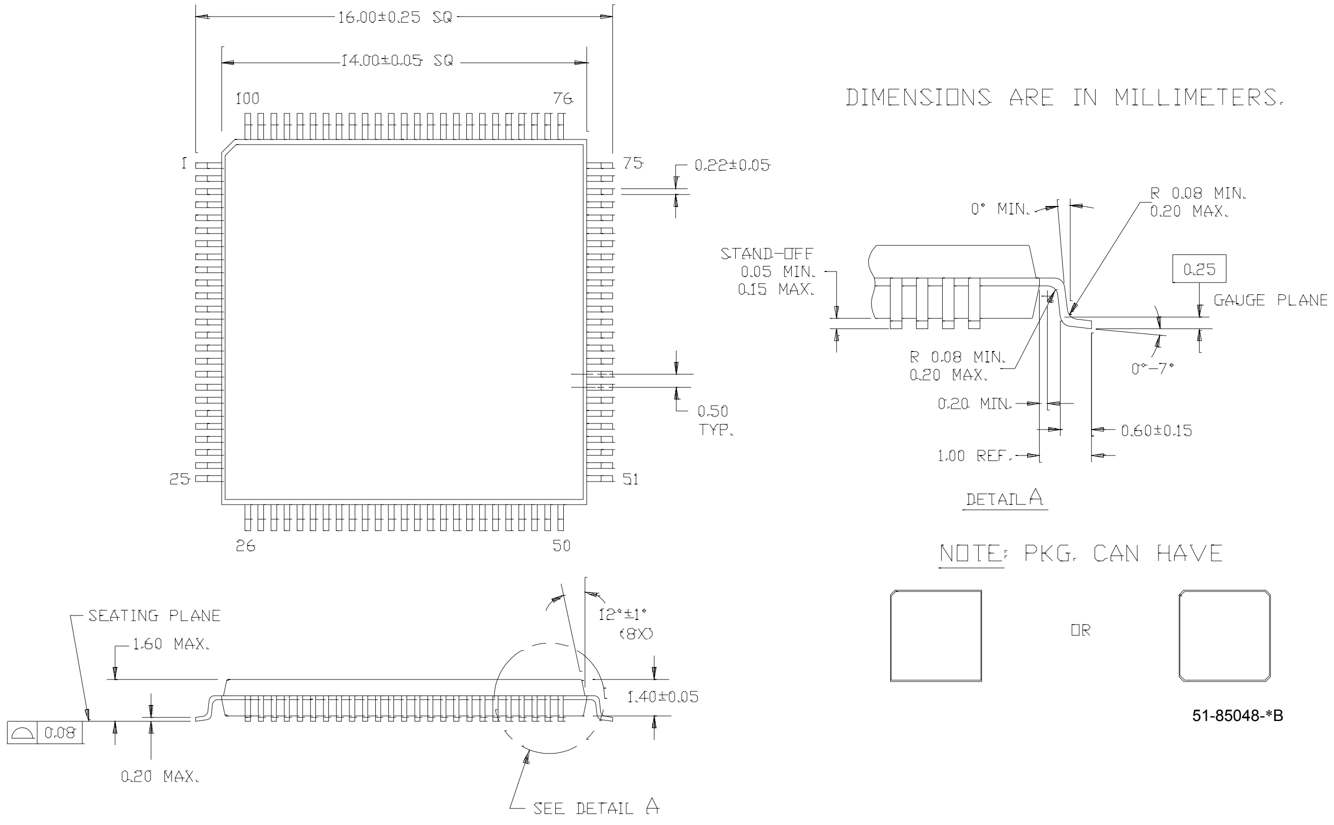


44-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J67



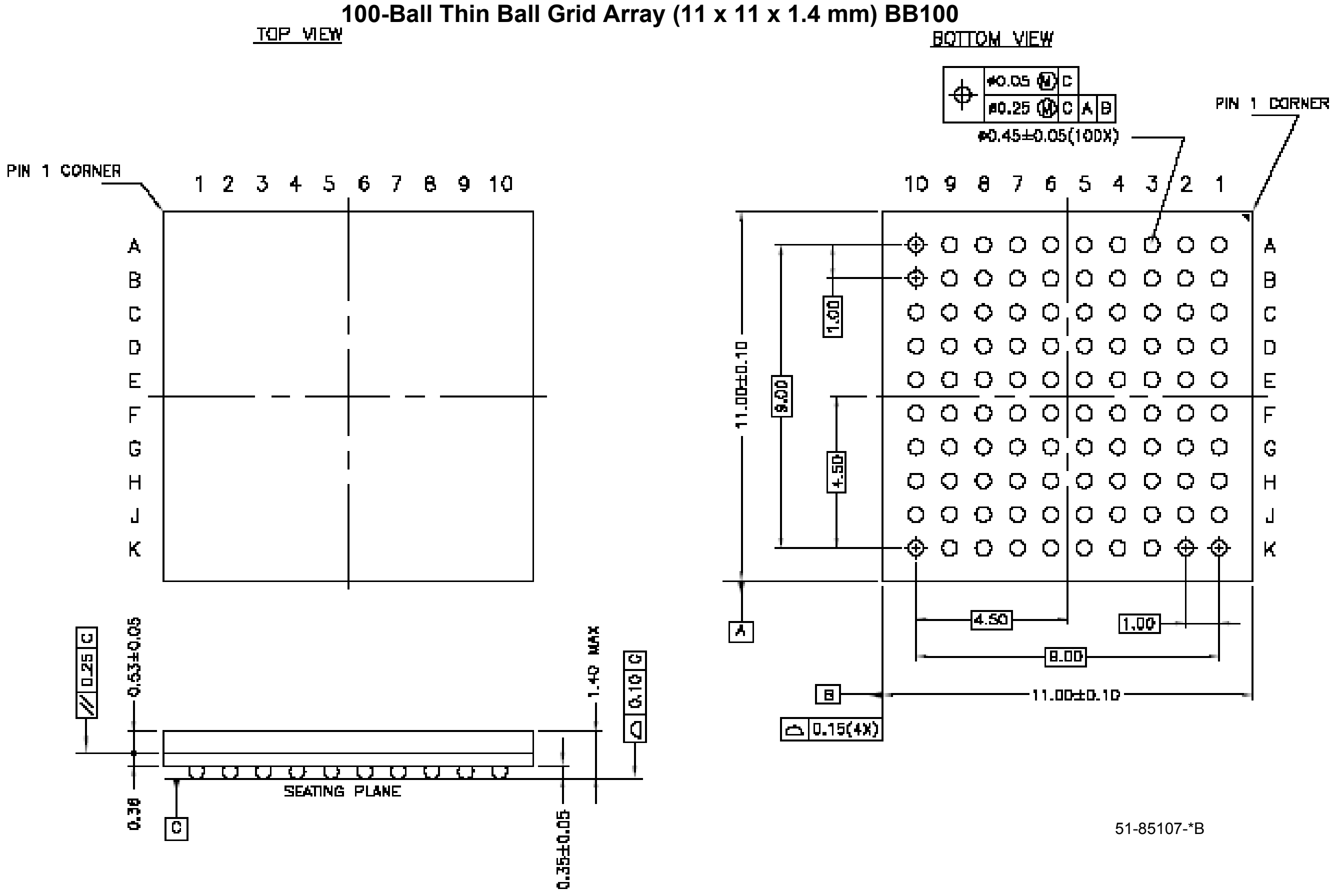
Package Diagrams (continued)

100-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (TQFP) A100



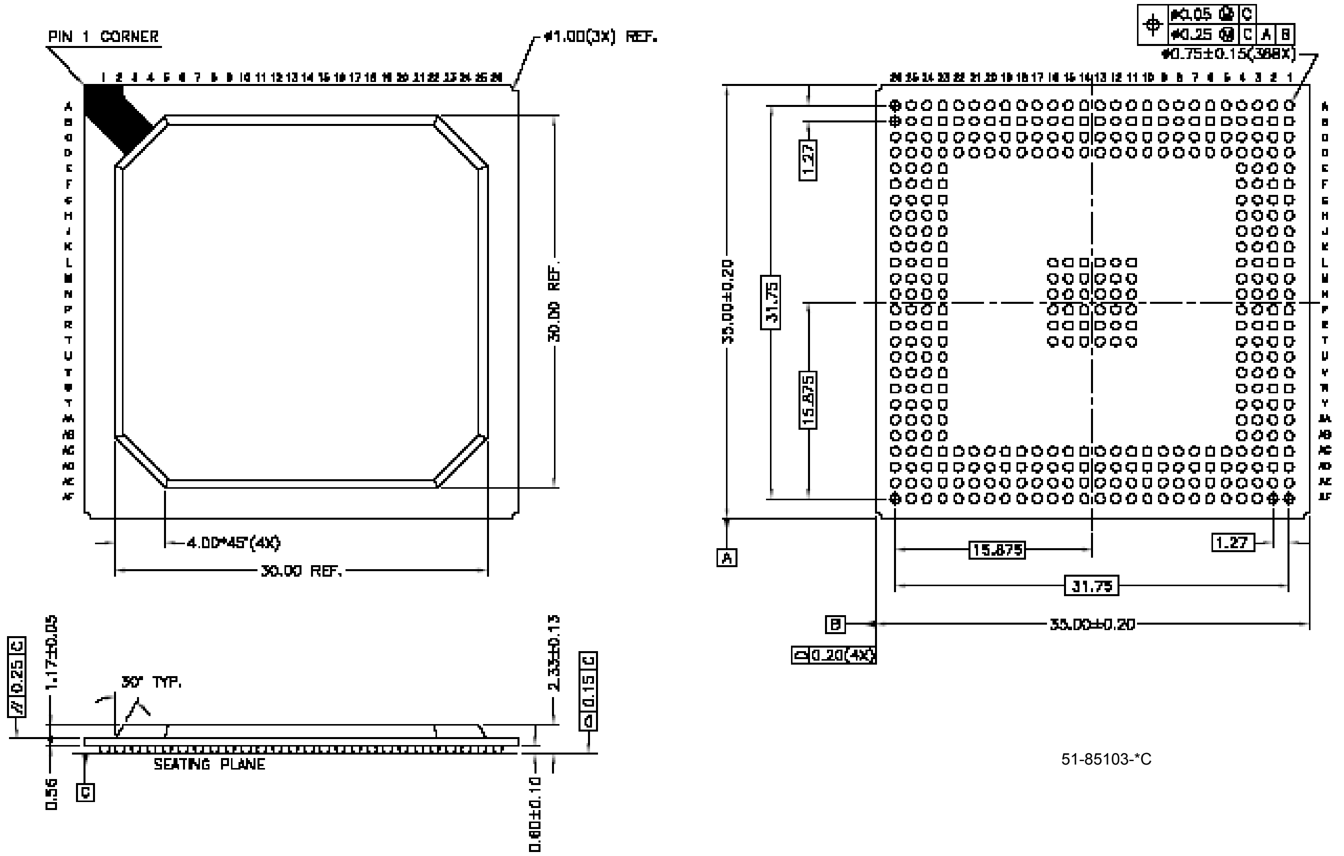
Package Diagrams (continued)

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388



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