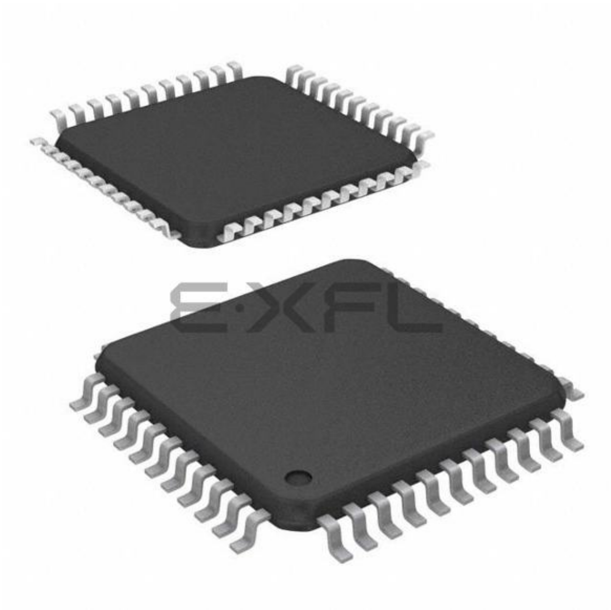


Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	37
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37032p44-125axct

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	388-Lead PBGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83

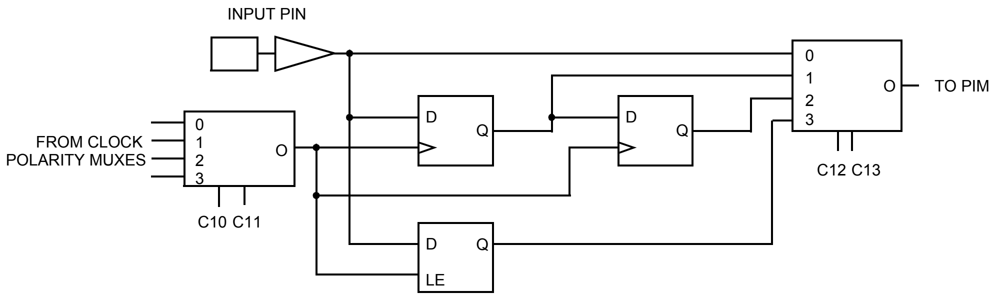


Figure 3. Input Macrocell

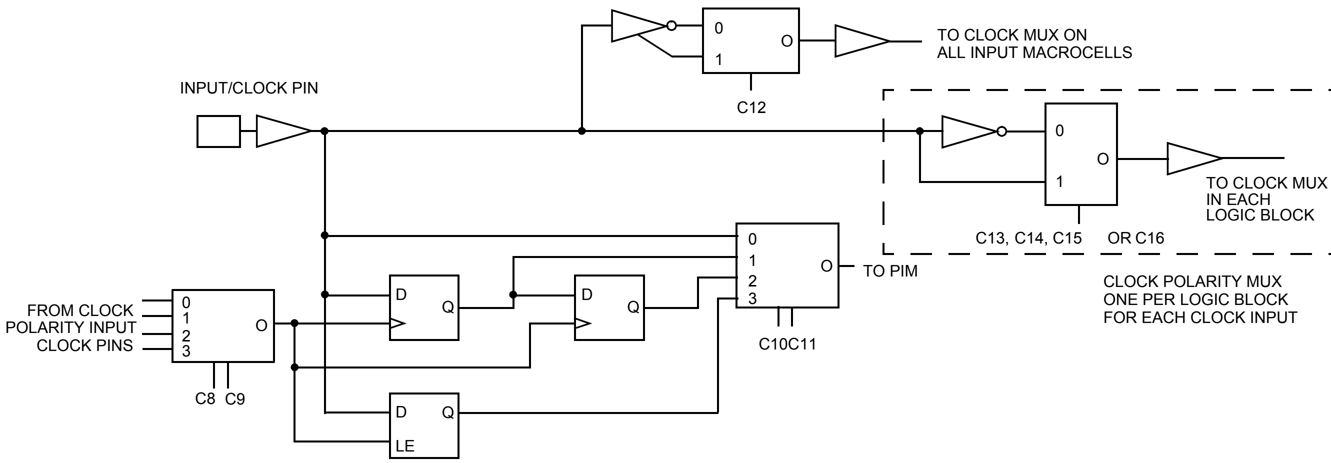


Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

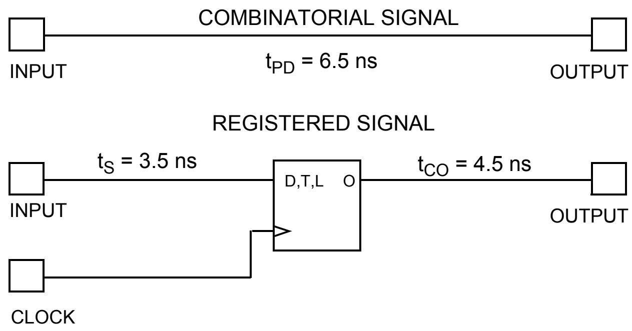


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

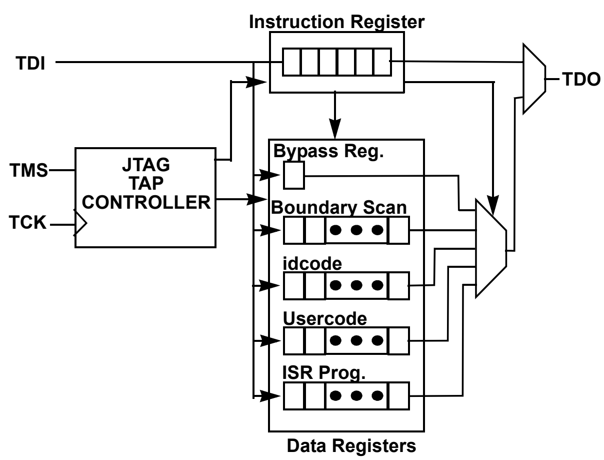


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC, *Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

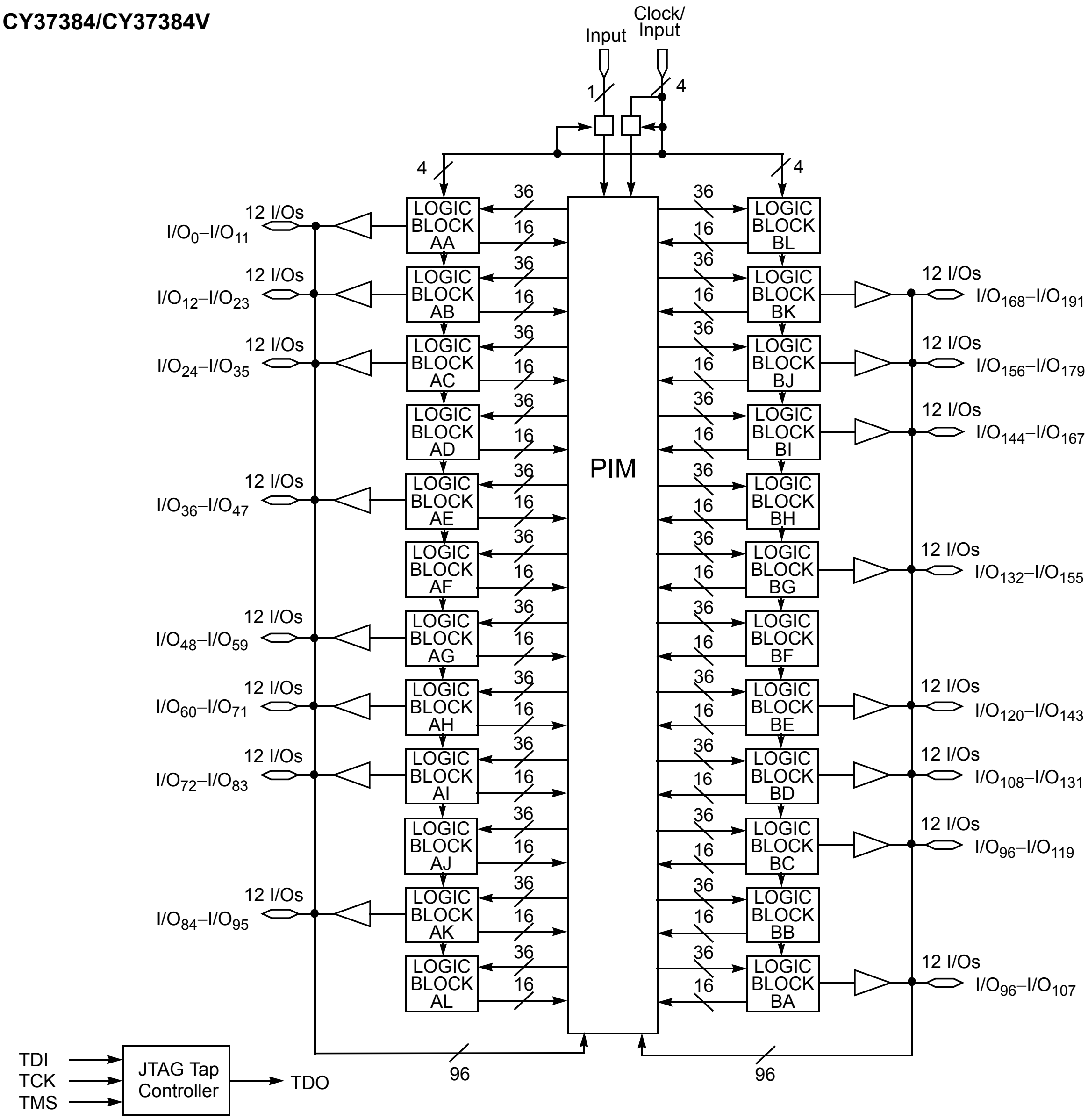
Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

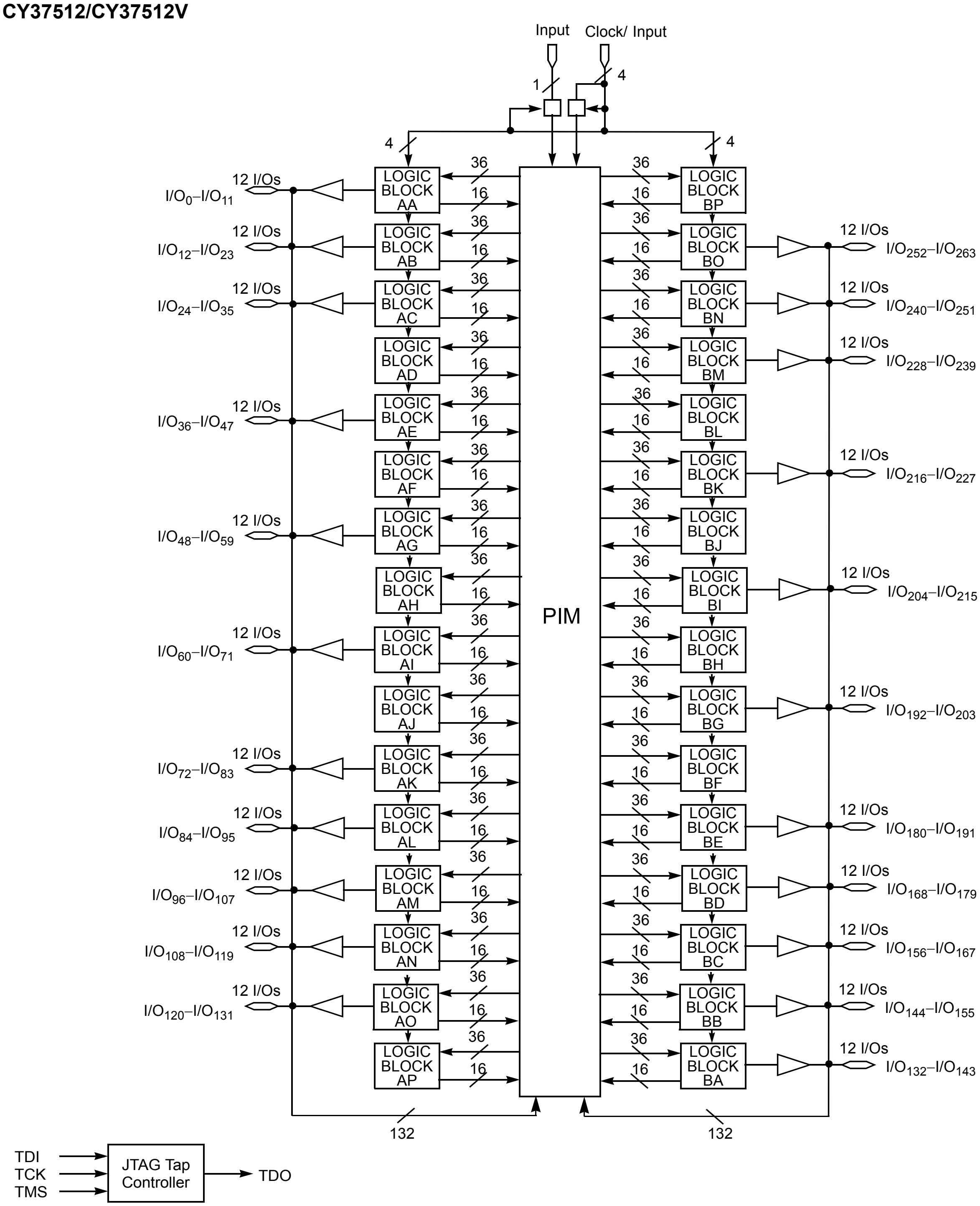
Logic Block Diagrams (continued)

CY37384/CY37384V



Logic Block Diagrams (continued)

CY37512/CY37512V



5.0V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied... –55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

DC Program Voltage... 4.5 to 5.5V

Current into Outputs .... 16 mA

Static Discharge Voltage.. > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[5]	V_{CC} = Max.	I_{OH} = 0 μA (Com'l)[6]			4.2	V
			I_{OH} = 0 μA (Ind/Mil)[6]			4.5	V
			I_{OH} = –100 μA (Com'l)[6]			3.6	V
			I_{OH} = –150 μA (Ind/Mil)[6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	μA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	μA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			μA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			μA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.				+500	μA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.				–500	μA

Notes:
2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled “An Introduction to In System Reprogramming with the Ultra37000.”
3. T_A is the “Instant On” case temperature.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note “Understanding Bus-Hold” for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual-Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

3.3V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with Power Applied...–55°C to +125°C

Supply Voltage to Ground Potential ....–0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State...–0.5V to +7.0V

DC Input Voltage ....–0.5V to +7.0V

DC Program Voltage... 3.0 to 3.6V

Current into Outputs .... 8 mA

Static Discharge Voltage.. > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}[10]
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	μA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	μA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		μA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		μA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	μA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	μA

Notes:
9. Dual pins are I/O with JTAG pins.
10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V± 0.16V.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

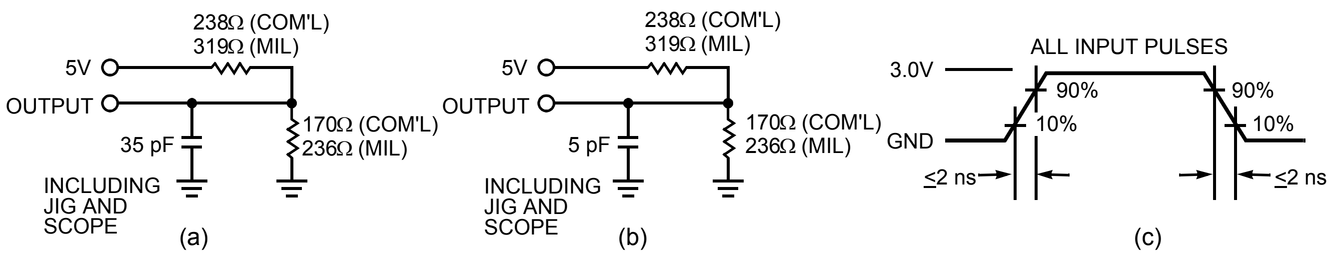
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

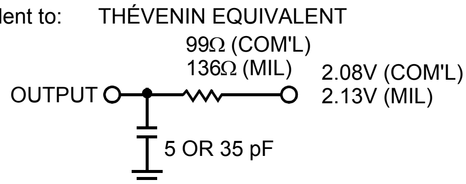
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Characteristics

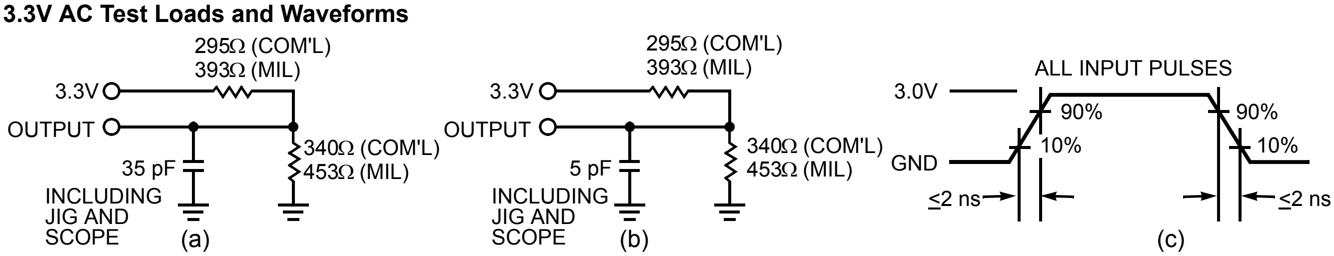
5.0V AC Test Loads and Waveforms



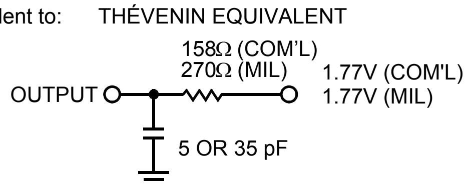
Equivalent to: THÉVENIN EQUIVALENT

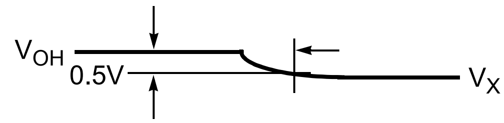
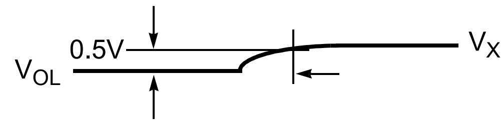
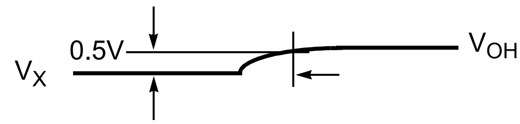
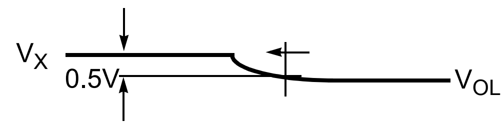


3.3V AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter[11]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

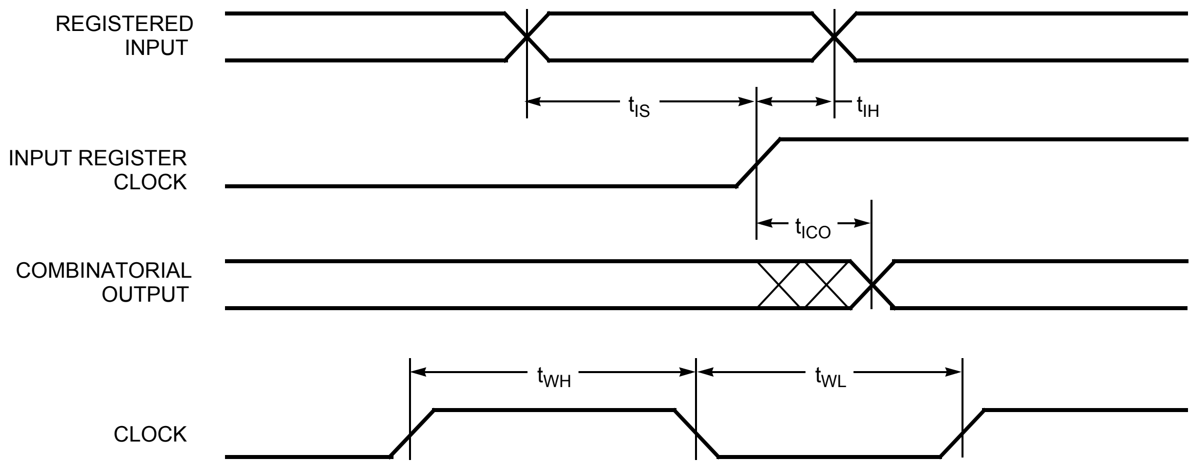
Switching Characteristics Over the Operating Range [12]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t_{PD}[13, 14, 15]	Input to Combinatorial Output	ns
t_{PDL}[13, 14, 15]	Input to Output Through Transparent Input or Output Latch	ns
t_{PDLL}[13, 14, 15]	Input to Output Through Transparent Input and Output Latches	ns
t_{EA}[13, 14, 15]	Input to Output Enable	ns
t_{ER}[11, 13]	Input to Output Disable	ns
Input Register Parameters		
t_{WL}	Clock or Latch Enable Input LOW Time[8]	ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	ns
t_{IS}	Input Register or Latch Set-up Time	ns
t_{IH}	Input Register or Latch Hold Time	ns
t_{ICO}[13, 14, 15]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t_{ICOL}[13, 14, 15]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t_{CO}[14, 15]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output	ns
t_S[13]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_H	Register or Latch Data Hold Time	ns
t_{CO2}[13, 14, 15]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t_{SCS}[13]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	ns
t_{SL}[13]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns

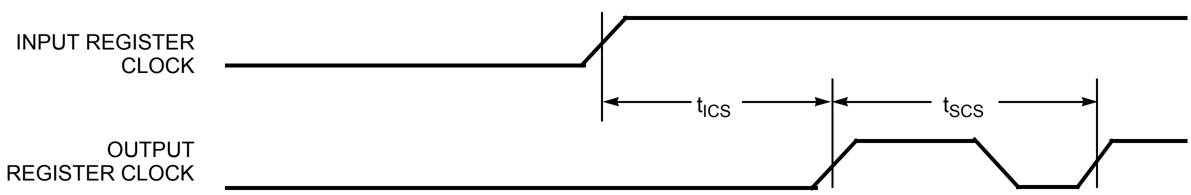
Notes:
11. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
12. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
13. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
14. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
15. When V_{CCO} = 3.3V, add $t_{3.3IO}$ to this spec.

Switching Waveforms (continued)

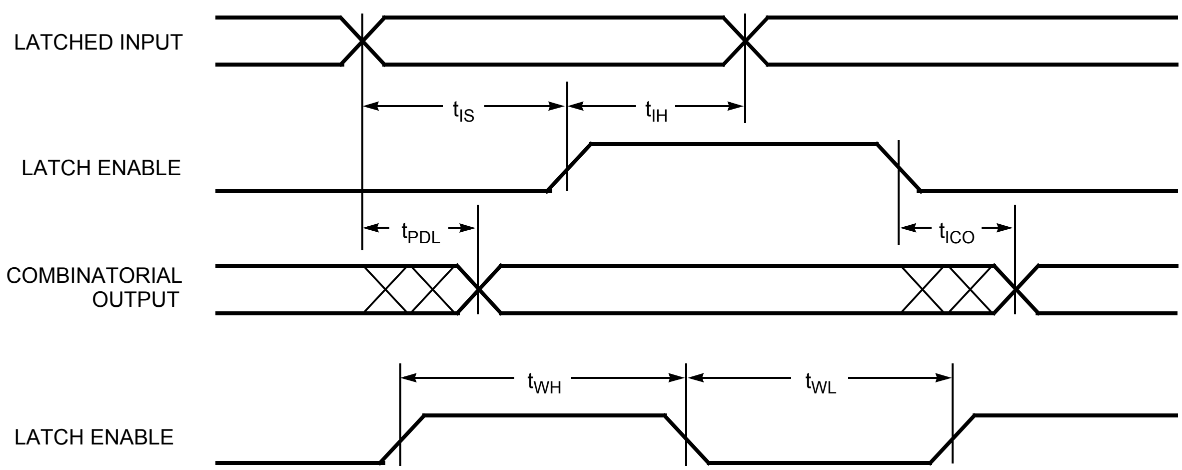
Registered Input



Clock to Clock

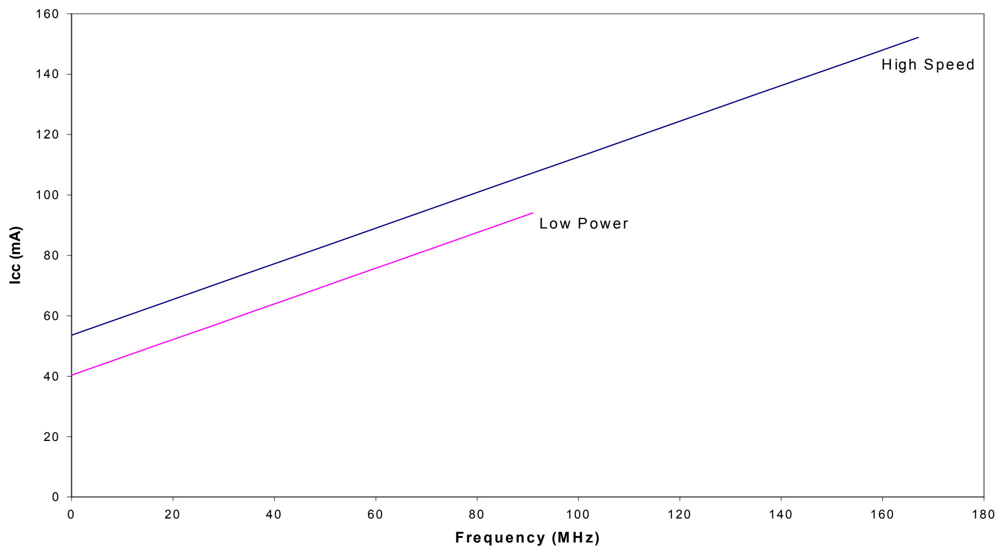


Latched Input



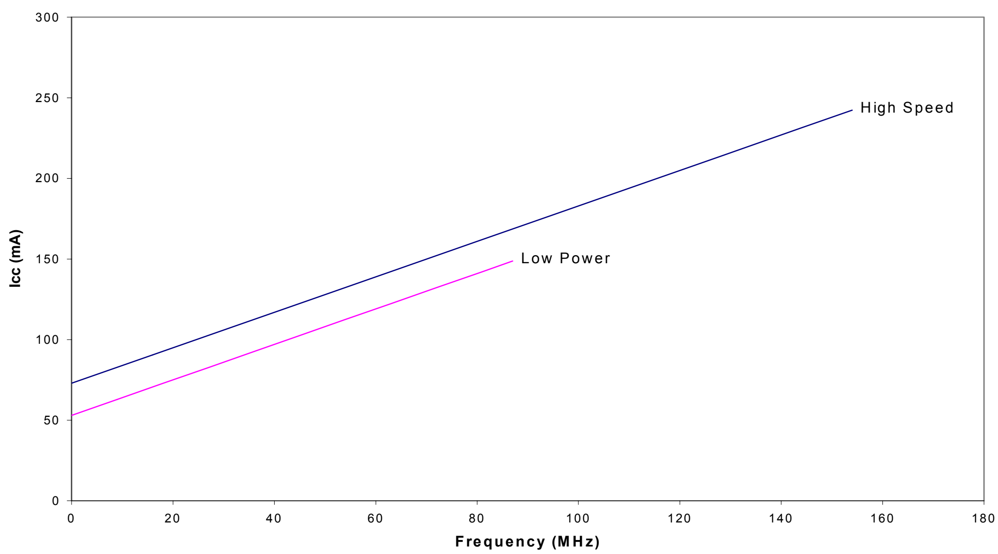
Typical 5.0V Power Consumption (continued)

CY37128



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

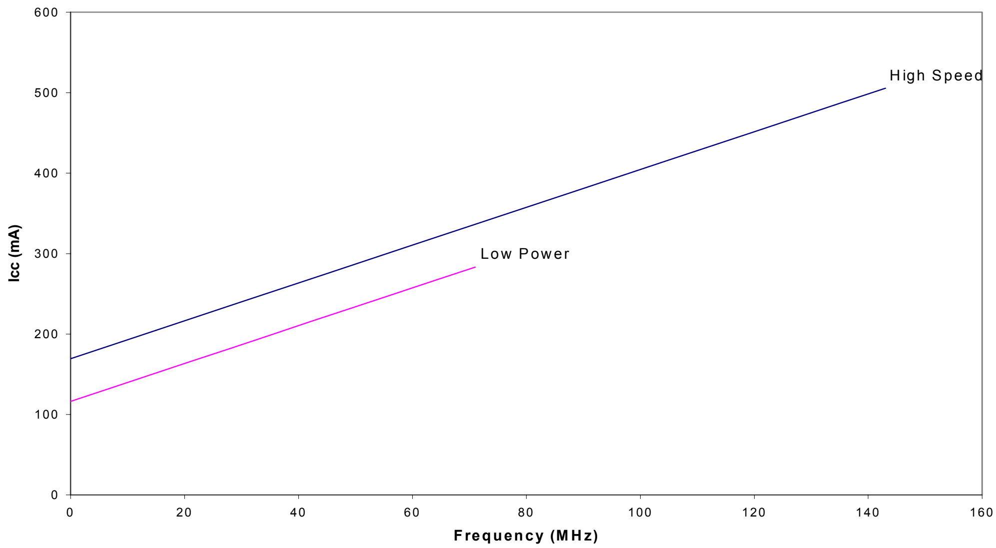
CY37192



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 5.0V Power Consumption (continued)

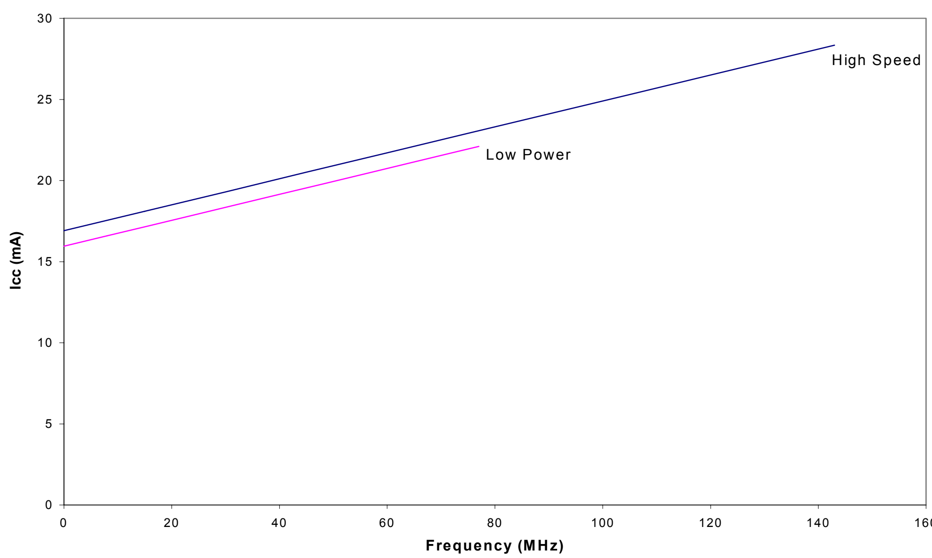
CY37512



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 3.3V Power Consumption

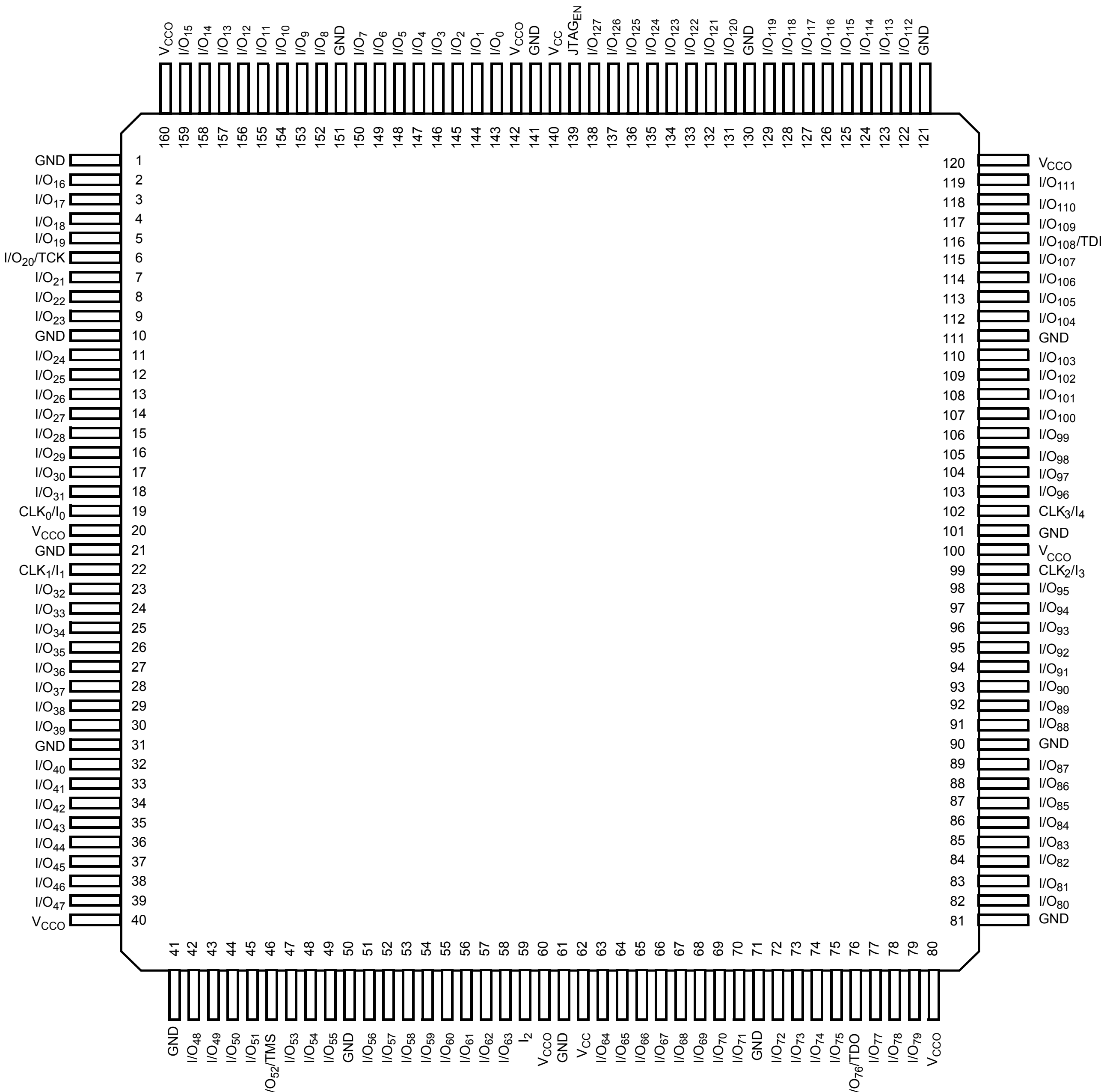
CY37032V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

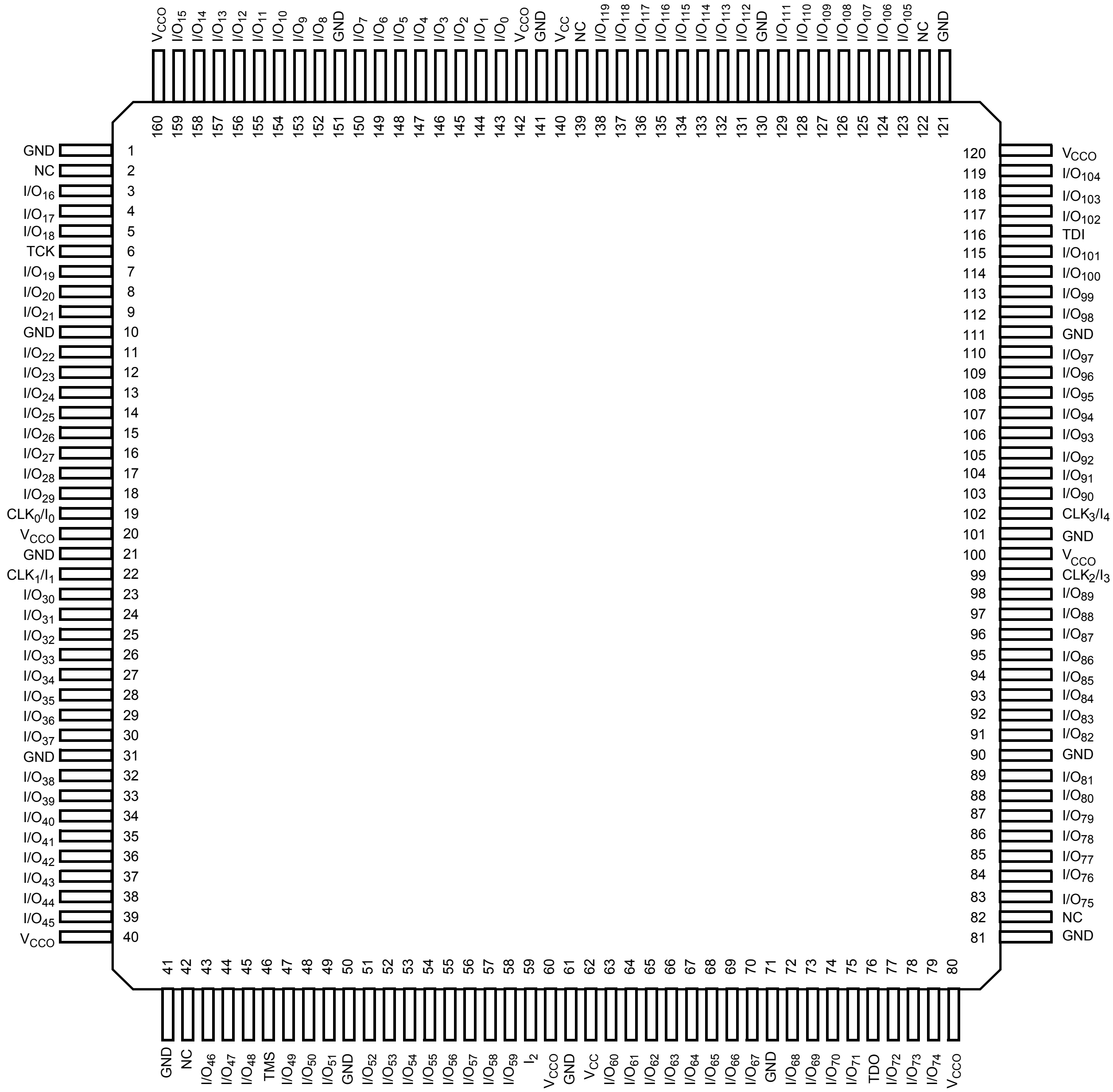
Pin Configurations[20] (continued)

160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View



Pin Configurations[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[20] (continued)

292-Ball PBGA (BG292)
Top View

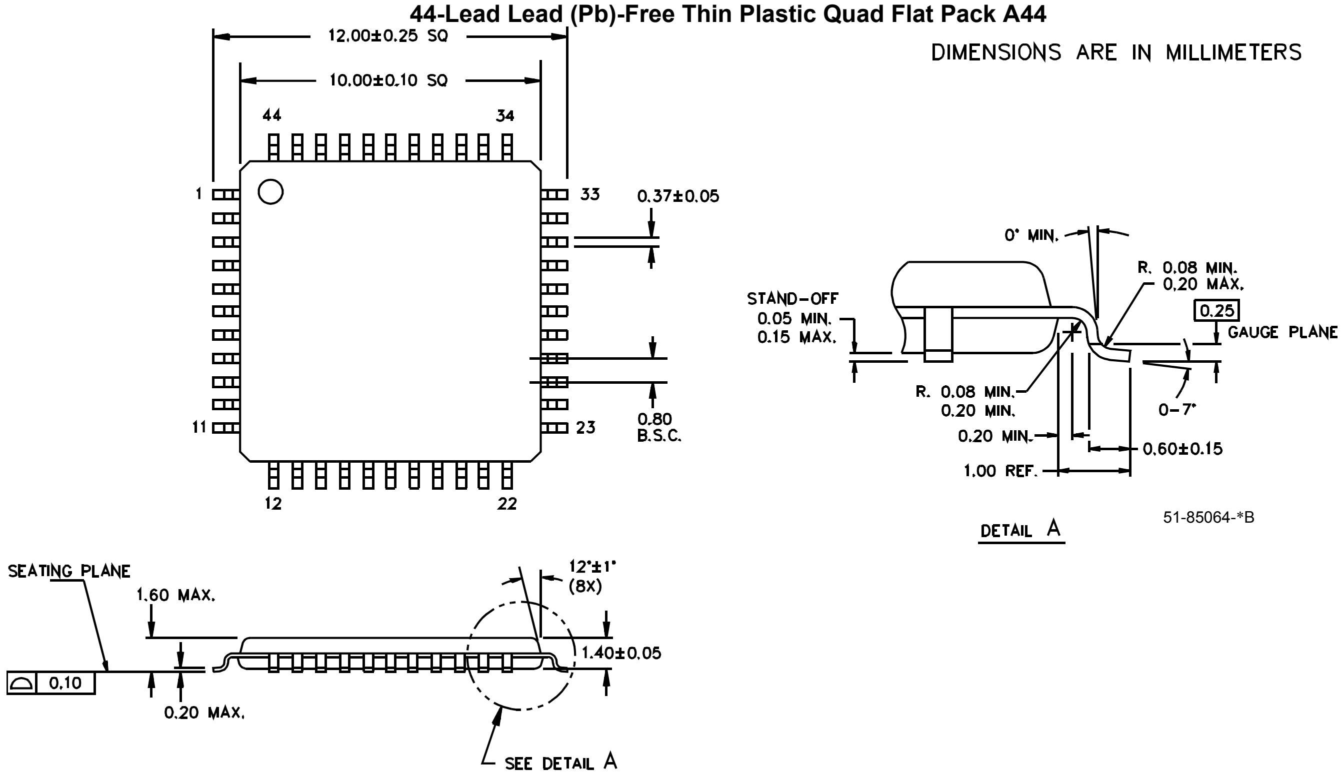
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O$_{21}$	NC	I/O$_{16}$	I/O$_{12}$	I/O$_{9}$	I/O$_{7}$	I/O$_{4}$	I/O$_{0}$	I/O$_{190}$	I/O$_{189}$	I/O$_{186}$	I/O$_{182}$	NC	I/O$_{178}$	I/O$_{175}$	NC	NC	I/O$_{169}$	I/O$_{168}$	A
B	I/O$_{23}$	I/O$_{20}$	I/O$_{19}$	I/O$_{18}$	I/O$_{15}$	I/O$_{11}$	I/O$_{8}$	I/O$_{5}$	I/O$_{1}$	I/O$_{191}$	I/O$_{187}$	I/O$_{185}$	I/O$_{181}$	NC	NC	I/O$_{174}$	I/O$_{171}$	I/O$_{170}$	NC	I/O$_{166}$	B
C	NC	NC	I/O$_{22}$	NC	I/O$_{17}$	I/O$_{14}$	I/O$_{10}$	I/O$_{6}$	I/O$_{2}$	NC	I/O$_{188}$	I/O$_{184}$	I/O$_{180}$	I/O$_{179}$	I/O$_{176}$	I/O$_{173}$	I/O$_{172}$	I/O$_{167}$	I/O$_{165}$	I/O$_{162}$	C
D	I/O$_{24}$	NC	NC	GND	NC	V_{CCO}	I/O$_{13}$	GND	I/O$_{3}$	NC	V_{CC}	I/O$_{183}$	GND	I/O$_{177}$	V_{CCO}	NC	GND	I/O$_{164}$	TDI	I/O$_{160}$	D
E	I/O$_{27}$	I/O$_{26}$	I/O$_{25}$	NC													I/O$_{163}$	I/O$_{161}$	I/O$_{159}$	I/O$_{156}$	E
F	I/O$_{30}$	TCK	I/O$_{28}$	V_{CCO}													V_{CCO}	I/O$_{158}$	NC	I/O$_{154}$	F
G	I/O$_{33}$	I/O$_{32}$	I/O$_{31}$	I/O$_{29}$													I/O$_{157}$	I/O$_{155}$	I/O$_{153}$	I/O$_{152}$	G
H	I/O$_{35}$	NC	I/O$_{34}$	GND				GND	GND	GND	GND	GND	GND				GND	I/O$_{151}$	I/O$_{150}$	I/O$_{149}$	H
J	I/O$_{39}$	I/O$_{38}$	I/O$_{37}$	I/O$_{36}$				GND	GND	GND	GND	GND	GND				I/O$_{148}$	I/O$_{147}$	I/O$_{146}$	I/O$_{145}$	J
K	I/O$_{42}$	I/O$_{40}$	I/O$_{41}$	V_{CC}				GND	GND	GND	GND	GND	GND				I/O$_{144}$	CLK$_{3}$/I$_{4}$	NC	NC	K
L	I/O$_{43}$	I/O$_{44}$	I/O$_{45}$	I/O$_{46}$				GND	GND	GND	GND	GND	GND				V_{CC}	CLK$_{2}$/I$_{3}$	I/O$_{143}$	NC	L
M	I/O$_{47}$	CLK$_{0}$/I$_{0}$	CLK$_{1}$/I$_{1}$	I/O$_{48}$				GND	GND	GND	GND	GND	GND				I/O$_{139}$	I/O$_{140}$	I/O$_{141}$	I/O$_{142}$	M
N	I/O$_{49}$	I/O$_{50}$	I/O$_{51}$	GND				GND	GND	GND	GND	GND	GND				GND	I/O$_{136}$	I/O$_{137}$	I/O$_{138}$	N
P	I/O$_{52}$	I/O$_{53}$	I/O$_{55}$	I/O$_{58}$													I/O$_{131}$	I/O$_{133}$	I/O$_{134}$	I/O$_{135}$	P
R	I/O$_{54}$	I/O$_{56}$	I/O$_{59}$	V_{CCO}													V_{CCO}	I/O$_{130}$	NC	I/O$_{132}$	R
T	I/O$_{57}$	I/O$_{60}$	I/O$_{62}$	I/O$_{65}$													I/O$_{124}$	I/O$_{127}$	I/O$_{128}$	I/O$_{129}$	T
U	I/O$_{61}$	I/O$_{63}$	I/O$_{66}$	GND	I/O$_{76}$	V_{CCO}	I/O$_{82}$	GND	I/O$_{91}$	V_{CC}	I/O$_{98}$	I/O$_{102}$	GND	I/O$_{112}$	V_{CCO}	NC	GND	I/O$_{123}$	I/O$_{122}$	I/O$_{126}$	U
V	I/O$_{64}$	I/O$_{67}$	I/O$_{69}$	I/O$_{75}$	I/O$_{78}$	I/O$_{81}$	I/O$_{85}$	I/O$_{88}$	I/O$_{92}$	I$_{2}$	I/O$_{97}$	I/O$_{101}$	I/O$_{105}$	I/O$_{109}$	I/O$_{113}$	TDO	I/O$_{114}$	I/O$_{117}$	I/O$_{121}$	I/O$_{125}$	V
W	I/O$_{68}$	I/O$_{70}$	I/O$_{72}$	I/O$_{74}$	I/O$_{79}$	I/O$_{83}$	I/O$_{86}$	I/O$_{89}$	I/O$_{93}$	I/O$_{95}$	I/O$_{96}$	I/O$_{100}$	I/O$_{104}$	I/O$_{107}$	I/O$_{110}$	NC	NC	I/O$_{115}$	I/O$_{118}$	I/O$_{120}$	W
Y	I/O$_{71}$	I/O$_{73}$	I/O$_{77}$	TMS	I/O$_{80}$	I/O$_{84}$	I/O$_{87}$	I/O$_{90}$	I/O$_{94}$	NC	NC	I/O$_{99}$	I/O$_{103}$	I/O$_{106}$	I/O$_{108}$	I/O$_{111}$	NC	NC	I/O$_{116}$	I/O$_{119}$	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

3.3V Ordering Information (continued)

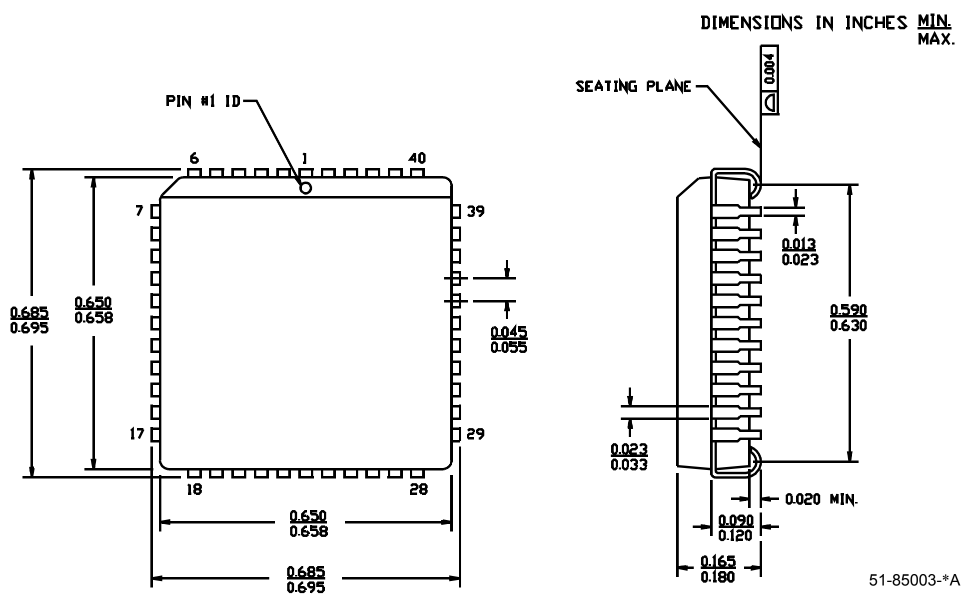
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

Package Diagrams

44-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack A44

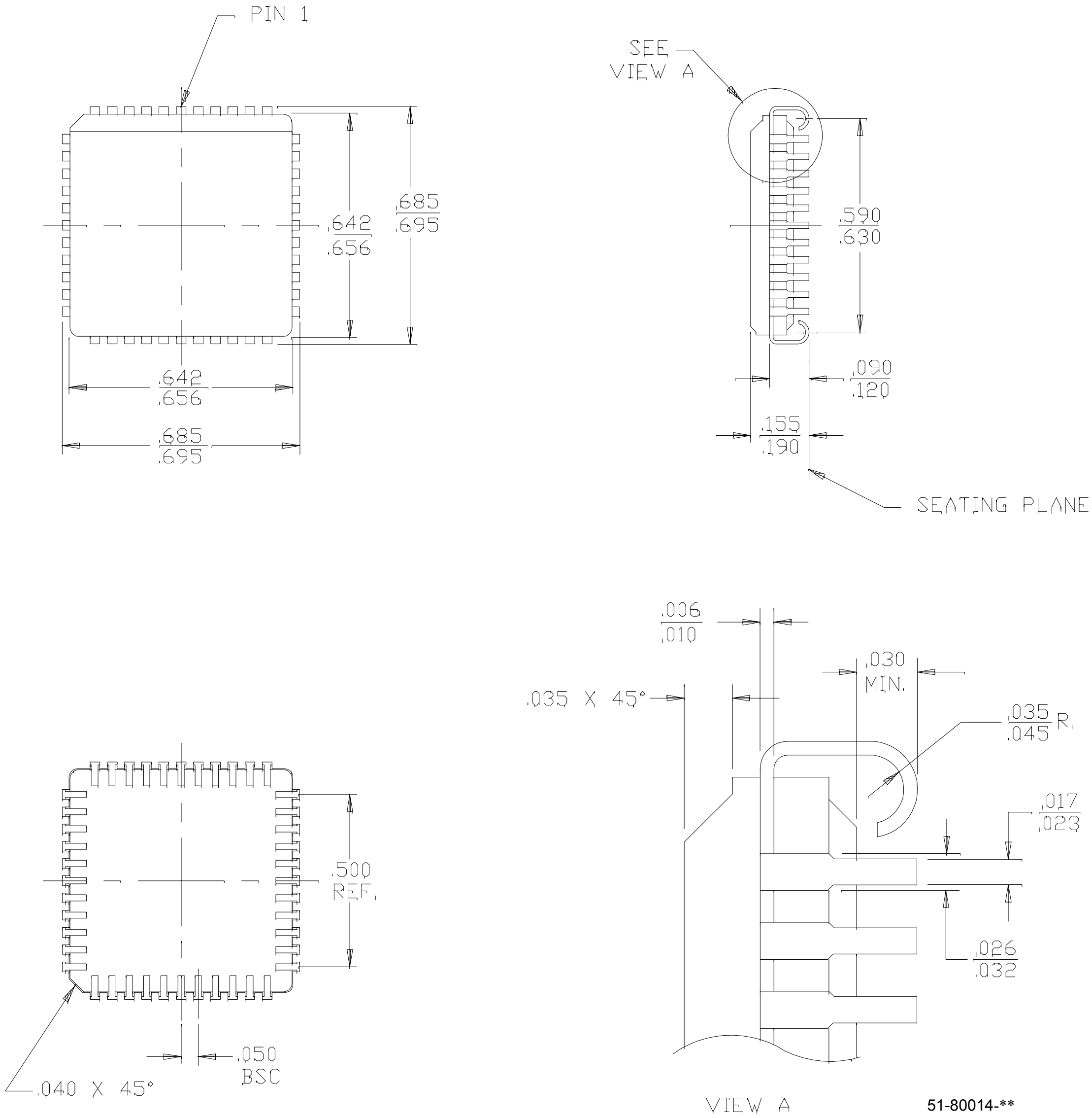


44-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J67



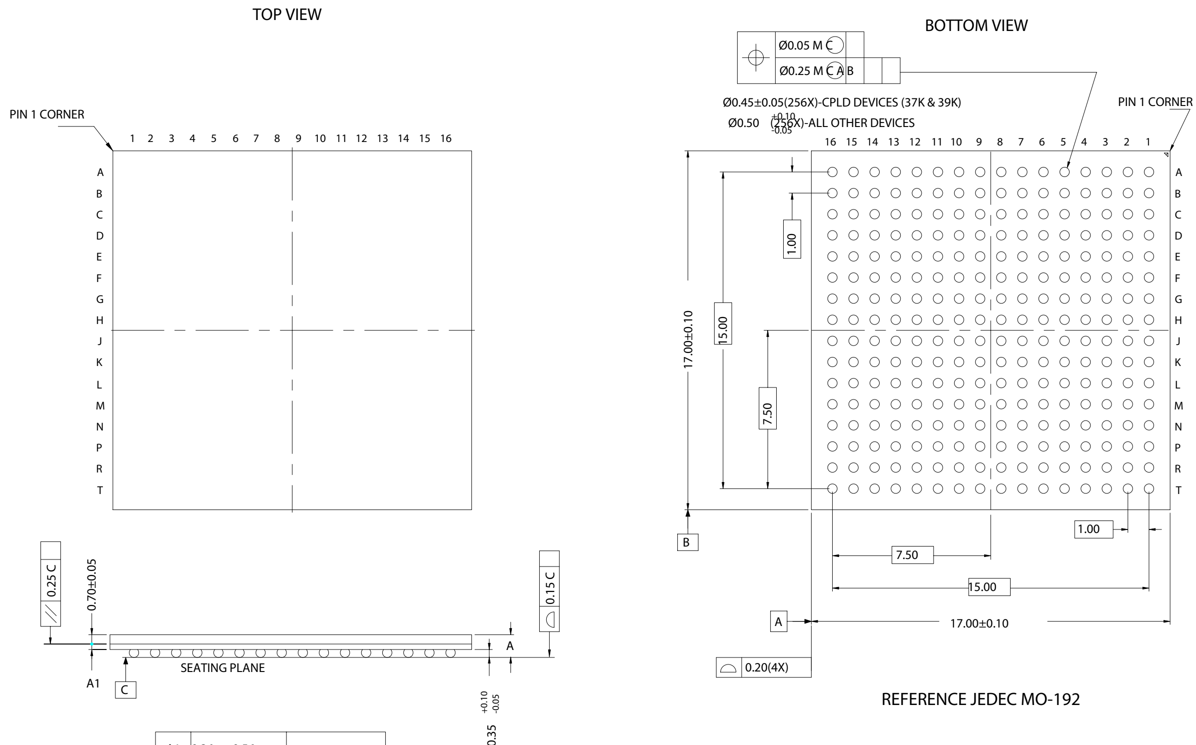
Package Diagrams (continued)

44-Lead Ceramic Leaded Chip Carrier Y67



Package Diagrams (continued)

256-Ball FBGA (17 x 17 mm) BB256



A1	0.36	0.56	
A	1.40 MAX.	1.70 MAX.	

51-85108-*F

Addendum

3.3V Operating Range

(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.16V