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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	37
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37032p44-154axi

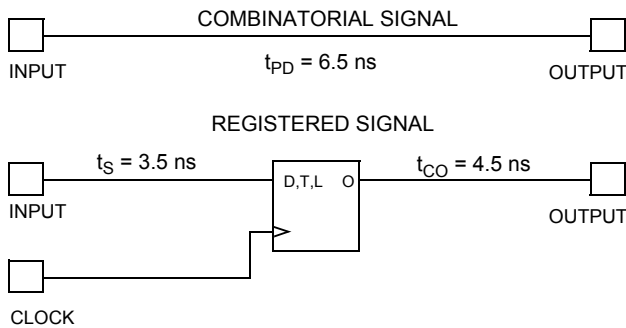


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in Figure 6.

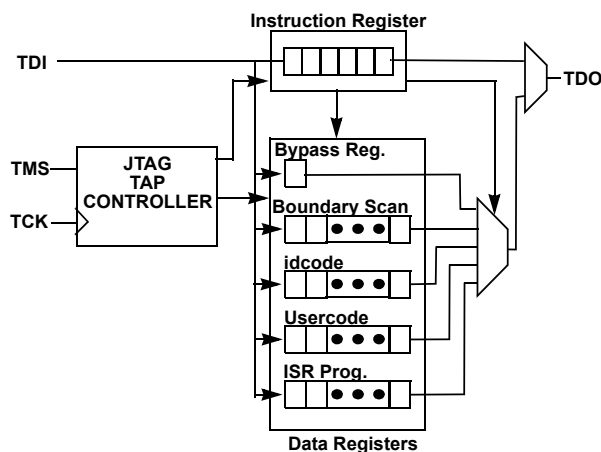


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing

resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the Warp for PC, Warp for UNIX, Warp Professional and Warp Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although Warp is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.



Ultra37000 CPLD Family

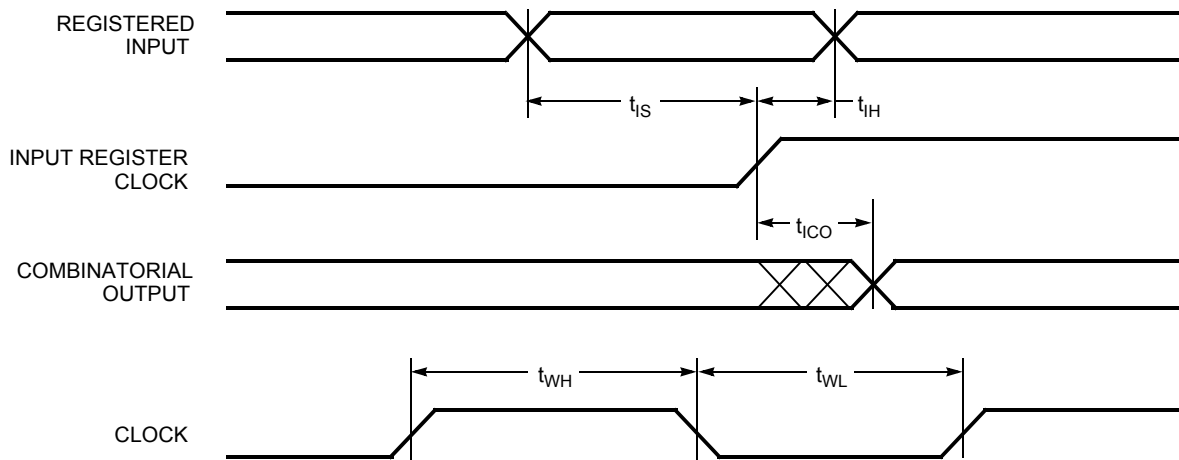
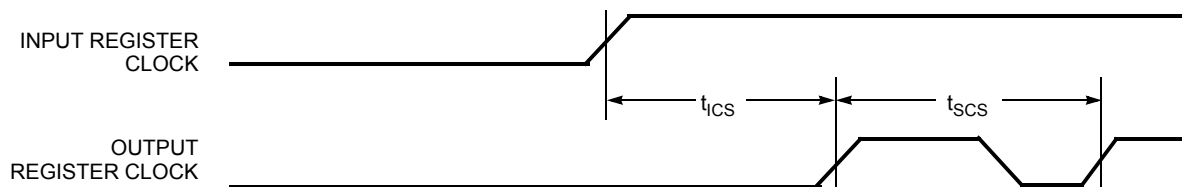
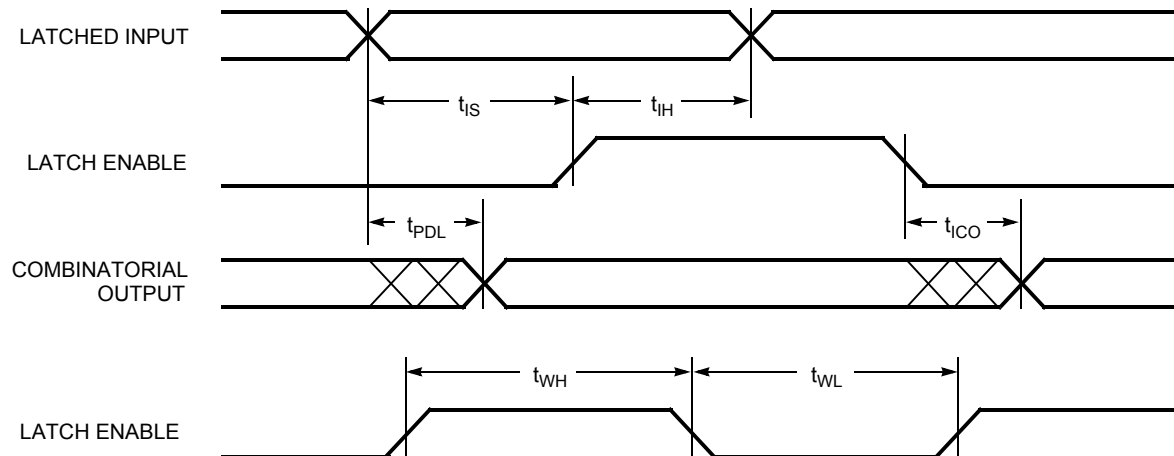
The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

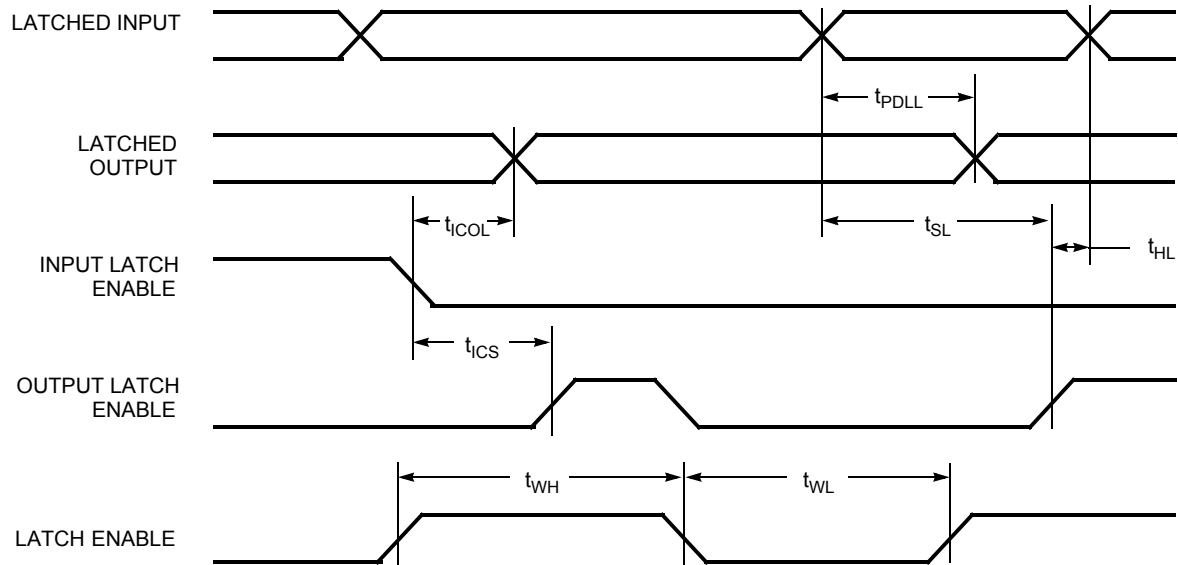
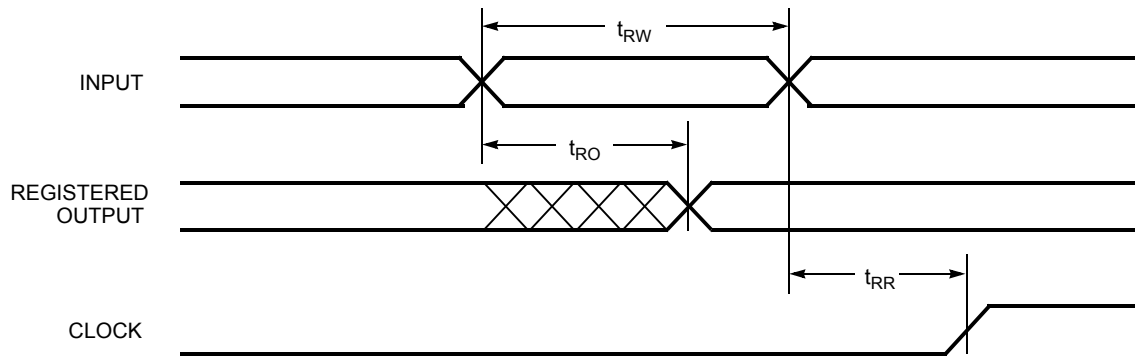
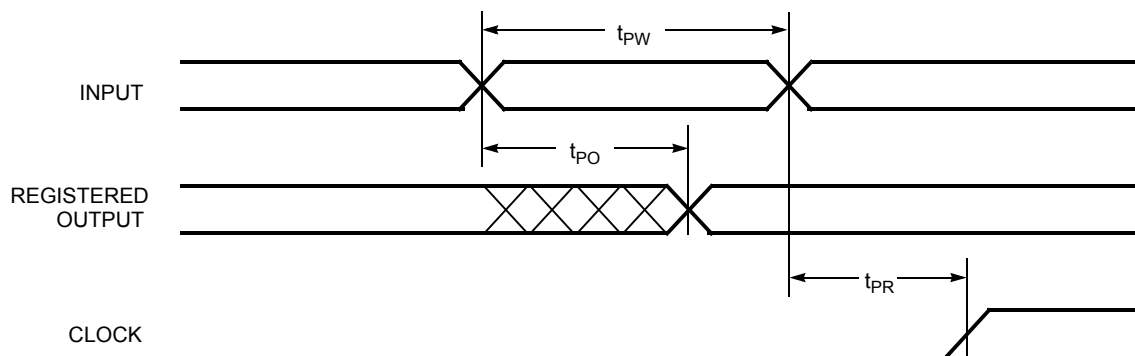
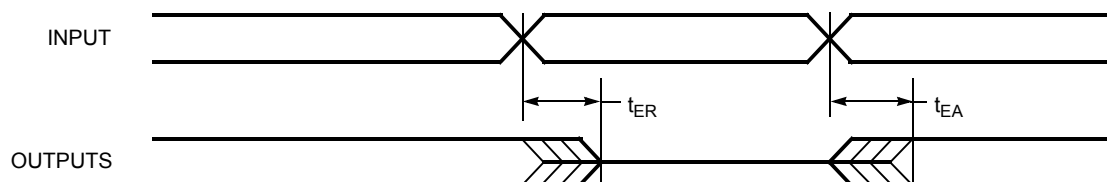
The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

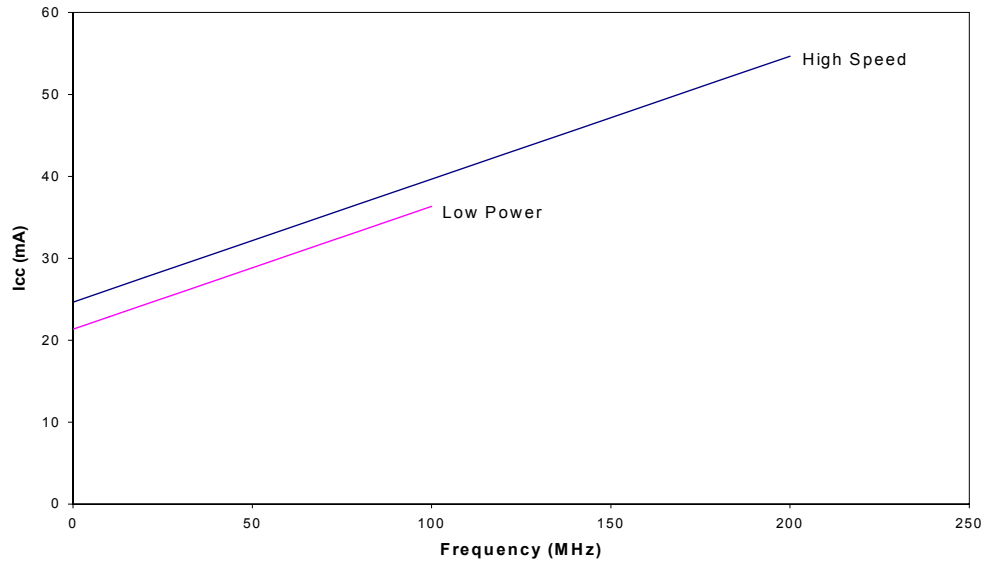
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Switching Waveforms (continued)
Registered Input

Clock to Clock

Latched Input


Switching Waveforms (continued)
Latched Input and Output

Asynchronous Reset

Asynchronous Preset

Output Enable/Disable


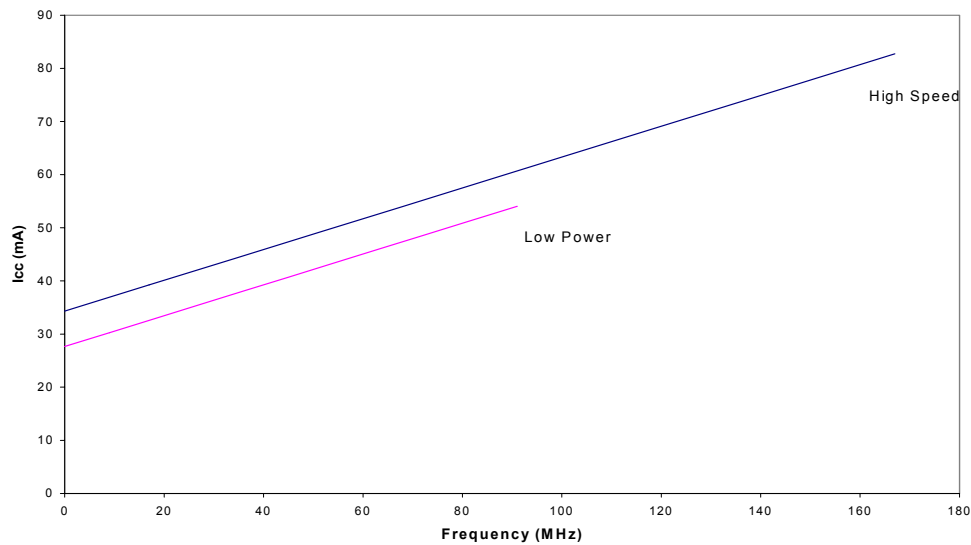
Power Consumption

Typical 5.0V Power Consumption CY37032

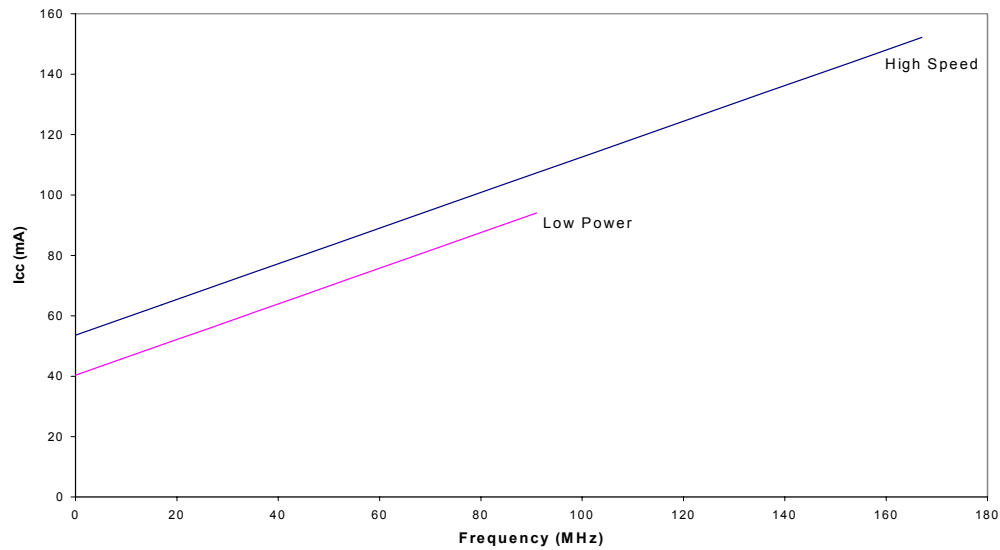


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

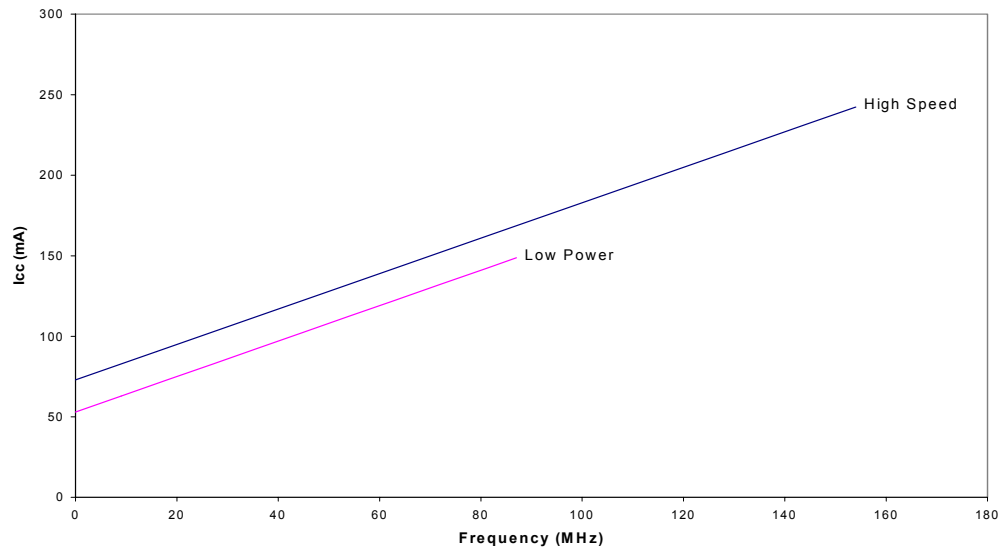
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 5.0V Power Consumption (continued)
CY37128


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

CY37192


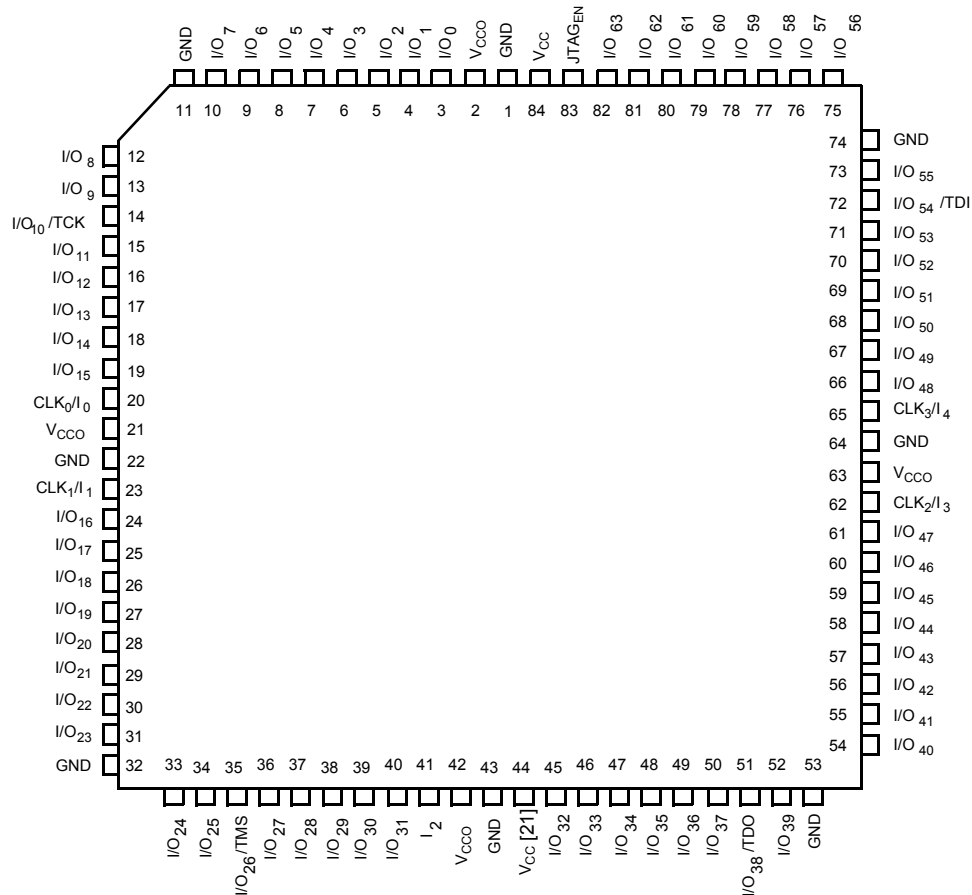
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Pin Configurations^[20] (continued)
48-ball Fine-Pitch BGA (BA50)
Top View

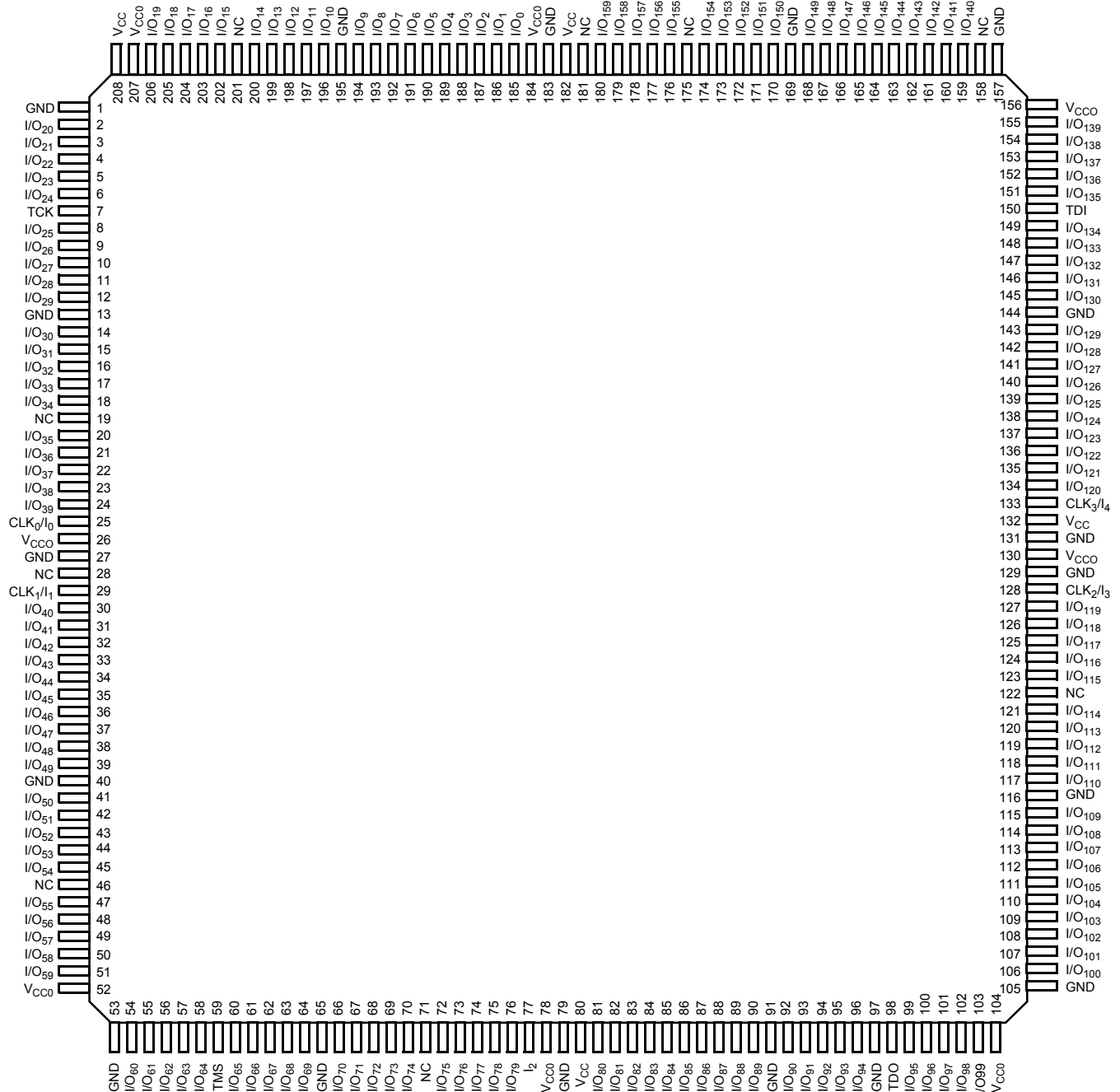
	1	2	3	4	5	6	7	8
A	I/O ₅ TCK	V _{CC}	I/O ₃	I/O ₁	I/O ₃₁	I/O ₃₀	V _{CC}	I/O ₂₇ TDI
B	V _{CC}	I/O ₄	I/O ₂	I/O ₀	I/O ₂₉	I/O ₂₈	I/O ₂₆	CLK ₁ /I ₄
C	CLK ₂ /I ₀	I/O ₇	I/O ₆	GND	GND	I/O ₂₅	I/O ₂₄	I ₃
D	JTAG _{EN}	I/O ₈	I/O ₉	GND	GND	I/O ₂₂	I/O ₂₃	CLK ₃ /I ₂
E	CLK ₀ /I ₁	I/O ₁₂	I/O ₁₁	I/O ₁₀	I/O ₁₆	I/O ₂₀	I/O ₂₁	V _{CC}
F	I/O ₁₃ TMS	V _{CC}	I/O ₁₄	I/O ₁₅	I/O ₁₇	I/O ₁₈	V _{CC}	I/O ₁₉ TDO

Note:

20. For 3.3V versions (Ultra37000V), V_{CCO} = V_{CC}.

84-lead PLCC (J83) / CLCC (Y84)
Top View

Note:

21. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations^[20] (continued)
**208-Lead PQFP (N208) / CQFP (U208)
Top View**


Pin Configurations^[20] (continued)
**292-Ball PBGA (BG292)
Top View**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O ₂₁	NC	I/O ₁₆	I/O ₁₂	I/O ₉	I/O ₇	I/O ₄	I/O ₀	I/O ₁₉₀	I/O ₁₈₉	I/O ₁₈₆	I/O ₁₈₂	NC	I/O ₁₇₈	I/O ₁₇₅	NC	NC	I/O ₁₆₉	I/O ₁₆₈	A
B	I/O ₂₃	I/O ₂₀	I/O ₁₉	I/O ₁₈	I/O ₁₅	I/O ₁₁	I/O ₈	I/O ₅	I/O ₁	I/O ₁₉₁	I/O ₁₈₇	I/O ₁₈₅	I/O ₁₈₁	NC	NC	I/O ₁₇₄	I/O ₁₇₁	I/O ₁₇₀	NC	I/O ₁₆₆	B
C	NC	NC	I/O ₂₂	NC	I/O ₁₇	I/O ₁₄	I/O ₁₀	I/O ₆	I/O ₂	NC	I/O ₁₈₈	I/O ₁₈₄	I/O ₁₈₀	I/O ₁₇₉	I/O ₁₇₆	I/O ₁₇₃	I/O ₁₇₂	I/O ₁₆₇	I/O ₁₆₅	I/O ₁₆₂	C
D	I/O ₂₄	NC	NC	GND	NC	V _{CC0}	I/O ₁₃	GND	I/O ₃	NC	V _{CC}	I/O ₁₈₃	GND	I/O ₁₇₇	V _{CC0}	NC	GND	I/O ₁₆₄	TDI	I/O ₁₆₀	D
E	I/O ₂₇	I/O ₂₆	I/O ₂₅	NC													I/O ₁₆₃	I/O ₁₆₁	I/O ₁₅₉	I/O ₁₅₆	E
F	I/O ₃₀	TCK	I/O ₂₈	V _{CC0}													V _{CC0}	I/O ₁₅₈	NC	I/O ₁₅₄	F
G	I/O ₃₃	I/O ₃₂	I/O ₃₁	I/O ₂₉													I/O ₁₅₇	I/O ₁₅₅	I/O ₁₅₃	I/O ₁₅₂	G
H	I/O ₃₅	NC	I/O ₃₄	GND	GND												GND	I/O ₁₅₁	I/O ₁₅₀	I/O ₁₄₉	H
J	I/O ₃₉	I/O ₃₈	I/O ₃₇	I/O ₃₆	GND												I/O ₁₄₈	I/O ₁₄₇	I/O ₁₄₆	I/O ₁₄₅	J
K	I/O ₄₂	I/O ₄₀	I/O ₄₁	V _{CC}	GND												I/O ₁₄₄	CLK ₃ /I ₄	NC	NC	K
L	I/O ₄₃	I/O ₄₄	I/O ₄₅	I/O ₄₆	GND												V _{CC}	CLK ₂ /I ₃	I/O ₁₄₃	NC	L
M	I/O ₄₇	CLK ₀ /I ₀	CLK ₁ /I ₁	I/O ₄₈	GND												I/O ₁₃₉	I/O ₁₄₀	I/O ₁₄₁	I/O ₁₄₂	M
N	I/O ₄₉	I/O ₅₀	I/O ₅₁	GND	GND												GND	I/O ₁₃₆	I/O ₁₃₇	I/O ₁₃₈	N
P	I/O ₅₂	I/O ₅₃	I/O ₅₅	I/O ₅₈													I/O ₁₃₁	I/O ₁₃₃	I/O ₁₃₄	I/O ₁₃₅	P
R	I/O ₅₄	I/O ₅₆	I/O ₅₉	V _{CC0}													V _{CC0}	I/O ₁₃₀	NC	I/O ₁₃₂	R
T	I/O ₅₇	I/O ₆₀	I/O ₆₂	I/O ₆₅													I/O ₁₂₄	I/O ₁₂₇	I/O ₁₂₈	I/O ₁₂₉	T
U	I/O ₆₁	I/O ₆₃	I/O ₆₆	GND	I/O ₇₆	V _{CC0}	I/O ₈₂	GND	I/O ₉₁	V _{CC}	I/O ₉₈	I/O ₁₀₂	GND	I/O ₁₁₂	V _{CC0}	NC	GND	I/O ₁₂₃	I/O ₁₂₂	I/O ₁₂₆	U
V	I/O ₆₄	I/O ₆₇	I/O ₆₉	I/O ₇₅	I/O ₇₈	I/O ₈₁	I/O ₈₅	I/O ₈₈	I/O ₉₂	I ₂	I/O ₉₇	I/O ₁₀₁	I/O ₁₀₅	I/O ₁₀₉	I/O ₁₁₃	TD0	I/O ₁₁₄	I/O ₁₁₇	I/O ₁₂₁	I/O ₁₂₅	V
W	I/O ₆₈	I/O ₇₀	I/O ₇₂	I/O ₇₄	I/O ₇₉	I/O ₈₃	I/O ₈₆	I/O ₈₉	I/O ₉₃	I/O ₉₅	I/O ₉₆	I/O ₁₀₀	I/O ₁₀₄	I/O ₁₀₇	I/O ₁₁₀	NC	NC	I/O ₁₁₅	I/O ₁₁₈	I/O ₁₂₀	W
Y	I/O ₇₁	I/O ₇₃	I/O ₇₇	TMS	I/O ₈₀	I/O ₈₄	I/O ₈₇	I/O ₉₀	I/O ₉₄	NC	NC	I/O ₉₉	I/O ₁₀₃	I/O ₁₀₆	I/O ₁₀₈	I/O ₁₁₁	NC	NC	I/O ₁₁₆	I/O ₁₁₉	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Pin Configurations^[20] (continued)

388-Lead PBGA (BG388)

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	GND	I/O ₁₉	I/O ₁₅	I/O ₁₃	I/O ₃₄	I/O ₃₁	I/O ₂₈	I/O ₂₅	I/O ₁₀	I/O ₇	I/O ₄	I/O ₁	I/O ₂₆₃	I/O ₂₆₀	I/O ₂₅₇	I/O ₂₅₄	I/O ₂₃₉	I/O ₂₃₇	I/O ₂₃₂	I/O ₂₂₉	I/O ₂₅₀	I/O ₂₄₈	I/O ₂₄₄	GND	GND
B	GND	NC	I/O ₁₈	I/O ₁₇	I/O ₁₄	I/O ₃₅	I/O ₃₂	I/O ₂₉	I/O ₂₆	I/O ₁₁	I/O ₈	I/O ₅	I/O ₂	V _{CC}	I/O ₂₆₁	I/O ₂₅₈	I/O ₂₅₅	I/O ₂₅₂	I/O ₂₃₄	I/O ₂₃₁	I/O ₂₂₈	I/O ₂₄₉	I/O ₂₄₆	I/O ₂₄₅	I/O ₂₄₀	GND
C	I/O ₂₃	I/O ₃₈	I/O ₃₇	I/O ₁₆	I/O ₁₂	I/O ₃₃	I/O ₃₀	I/O ₂₇	I/O ₂₄	I/O ₉	I/O ₆	I/O ₃	I/O ₀	I/O ₂₆₂	I/O ₂₅₉	I/O ₂₅₆	I/O ₂₅₃	I/O ₂₃₈	I/O ₂₃₅	I/O ₂₃₃	I/O ₂₃₀	I/O ₂₅₁	I/O ₂₄₇	I/O ₂₂₅	I/O ₂₂₄	I/O ₂₂₇
D	I/O ₃₉	I/O ₄₀	I/O ₃₆	NC	NC	I/O ₂₁	I/O ₂₀	V _{CCO}	V _{CCO}	NC	GND	GND	V _{CCO}	V _{CCO}	GND	GND	NC	V _{CCO}	V _{CCO}	I/O ₂₃₆	I/O ₂₄₃	NC	NC	I/O ₂₂₆	I/O ₂₂₂	I/O ₂₂₃
E	I/O ₄₂	TCK	I/O ₄₁	NC																			NC	TDI	I/O ₂₂₁	I/O ₂₂₀
F	I/O ₄₅	I/O ₄₄	I/O ₄₃	I/O ₂₂																			I/O ₂₄₂	I/O ₂₁₉	I/O ₂₁₈	I/O ₂₁₇
G	I/O ₄₈	I/O ₄₇	I/O ₄₆	I/O ₆₃																			I/O ₂₄₁	I/O ₂₁₆	I/O ₂₁₅	I/O ₂₁₄
H	I/O ₄₉	I/O ₅₀	I/O ₅₁	V _{CCO}																			V _{CCO}	I/O ₂₁₁	I/O ₂₁₂	I/O ₂₁₃
J	I/O ₅₂	I/O ₅₃	I/O ₅₄	V _{CCO}																			V _{CCO}	I/O ₂₀₈	I/O ₂₀₉	I/O ₂₁₀
K	I/O ₅₅	I/O ₅₆	I/O ₅₇	NC																			NC	I/O ₂₀₅	I/O ₂₀₆	I/O ₂₀₇
L	I/O	I/O ₅₉	I/O ₅₈	GND																			GND	I/O ₂₀₄	I/O ₁₉₇	I/O ₁₉₇
M	I/O ₆₁	I/O ₆₀	I/O	GND																			GND	I/O	I/O ₂₀₃	I/O ₂₀₂
N	I/O ₆₄	V _{CC}	I/O ₆₂	V _{CCO}																			V _{CCO}	I/O ₂₀₁	I/O ₂₀₀	I/O ₁₉₉
P	I/O ₆₅	I/O ₆₆	I/O ₆₇	V _{CCO}																			V _{CCO}	I/O ₁₉₆	V _{CC}	I/O ₁₉₈
R	I/O ₆₈	I/O ₆₉	I/O ₇₀	GND																			GND	I/O ₁₉₃	I/O ₁₉₄	I/O ₁₉₅
T	I/O ₇₁	I/O ₈₄	I/O ₈₅	GND																			GND	I/O ₁₇₈	I/O ₁₇₉	I/O ₁₉₂
U	I/O ₈₈	I/O ₈₇	I/O ₈₆	NC																			NC	I/O ₁₇₇	I/O ₁₇₆	I/O ₁₇₅
V	I/O ₉₁	I/O ₉₀	I/O ₈₉	V _{CCO}																			V _{CCO}	I/O ₁₇₄	I/O ₁₇₃	I/O ₁₇₂
W	I/O ₉₄	I/O ₉₃	I/O ₉₂	V _{CCO}																			V _{CCO}	I/O ₁₇₁	I/O ₁₇₀	I/O ₁₆₉
Y	I/O ₉₅	I/O ₇₂	I/O ₇₃	I/O ₁₁₀																			I/O ₁₅₃	I/O ₁₉₀	I/O ₁₉₁	I/O ₁₆₈
AA	I/O ₇₄	I/O ₇₅	I/O ₇₆	I/O ₁₁₁																			I/O ₁₅₂	I/O ₁₈₇	I/O ₁₈₈	I/O ₁₈₉
AB	I/O ₇₇	I/O ₇₈	I/O ₇₉	NC																			NC	I/O ₁₈₄	I/O ₁₈₅	I/O ₁₈₆
AC	I/O ₈₁	I/O ₈₀	I/O ₁₀₈	NC	NC	I/O ₁₁₂	I/O ₁₁₃	V _{CCO}	V _{CCO}	NC	GND	GND	V _{CCO}	V _{CCO}	GND	GND	NC	V _{CCO}	V _{CCO}	I/O ₁₅₀	I/O ₁₅₁	NC	NC	I/O ₁₅₅	I/O ₁₈₃	I/O ₁₈₂
AD	I/O ₁₀₉	I/O ₈₂	I/O ₈₃	I/O ₁₁₇	I/O ₉₇	I/O ₁₀₀	I/O ₁₀₂	I/O ₁₀₅	I/O ₁₂₀	I/O ₁₂₃	I/O ₁₂₆	I/O ₁₂₉	I/O	I/O ₁₃₃	I/O ₁₃₆	I/O ₁₃₉	I/O ₁₄₂	I/O ₁₅₇	I/O ₁₅₉	I/O ₁₆₁	I/O ₁₆₃	I/O ₁₆₆	I/O ₁₄₆	I/O ₁₈₀	I/O ₁₈₁	I/O ₁₅₄
AE	GND	NC	I/O ₁₁₅	I/O ₁₁₆	I/O ₁₁₉	I/O ₉₈	I/O ₁₀₁	I/O ₁₀₃	I/O ₁₀₆	I/O ₁₂₁	I/O ₁₂₄	I/O ₁₂₇	V _{CC}	I/O ₁₃₀	I/O ₁₃₄	I/O ₁₃₇	I/O ₁₄₀	I/O ₁₄₃	I/O ₁₆₀	I/O ₁₆₂	I/O ₁₆₅	I/O ₁₄₄	I/O ₁₄₇	I/O ₁₄₈	NC	GND
AF	GND	GND	I/O ₁₁₄	I/O ₁₁₈	I/O ₉₆	I/O ₉₉	TMS	I/O ₁₀₄	I/O ₁₀₇	I/O ₁₂₂	I/O ₁₂₅	I/O ₁₂₈	I/O ₁₃₁	I/O ₁₃₂	I/O ₁₃₅	I/O ₁₃₈	I/O ₁₄₁	I/O ₁₅₆	I/O ₁₅₈	TDO	I/O ₁₆₄	I/O ₁₆₇	I/O ₁₄₅	I/O ₁₄₉	GND	GND

Pin Configurations^[20] (continued)
400-Ball Fine-Pitch BGA (BB400)
Top View

A	GND	GND	NC	I/O ₁₇	I/O ₁₆	I/O ₁₄	I/O ₂₉	V _{CC}	I/O ₁₁	GND	GND	I/O ₂₅₇	V _{CC}	I/O ₂₃₉	I/O ₂₃₃	I/O ₂₃₂	I/O ₂₃₀	NC	GND	GND
B	GND	GND	GND	NC	I/O ₁₅	I/O ₁₃	I/O ₂₈	V _{CC}	I/O ₁₀	GND	GND	I/O ₂₅₆	V _{CC}	I/O ₂₃₈	I/O ₂₃₁	I/O ₂₂₉	NC	GND	GND	GND
C	NC	GND	GND	GND	I/O ₂₀	I/O ₁₂	I/O ₂₇	V _{CC}	I/O ₉	GND	GND	I/O ₂₅₅	V _{CC}	I/O ₂₃₇	I/O ₂₂₈	I/O ₂₄₅	GND	GND	GND	NC
D	I/O ₄₄	NC	GND	I/O ₂₁	I/O ₁₉	I/O ₁₈	I/O ₂₆	I/O ₂₅	I/O ₈	GND	GND	I/O ₂₅₄	I/O ₂₃₅	I/O ₂₃₆	I/O ₂₅₁	I/O ₂₄₄	I/O ₂₄₃	GND	NC	I/O ₂₂₇
E	I/O ₄₆	I/O ₄₃	I/O ₂₃	I/O ₂₂	NC	I/O ₃₅	I/O ₃₄	I/O ₂₄	I/O ₇	I/O ₄	I/O ₂₆₃	I/O ₂₅₃	I/O ₂₃₄	I/O ₂₅₀	I/O ₂₄₈	NC	I/O ₂₄₁	I/O ₂₄₂	I/O ₂₂₅	I/O ₂₂₆
F	I/O ₄₇	I/O ₄₅	I/O ₄₂	I/O ₄₁	I/O ₄₀	NC	I/O ₃₃	I/O ₃₂	I/O ₆	I/O ₃	I/O ₂₆₂	I/O ₂₅₂	I/O ₂₄₉	I/O ₂₄₇	I/O ₂₂₀	I/O ₂₂₁	I/O ₂₄₀	I/O ₂₂₂	I/O ₂₂₃	I/O ₂₂₄
G	I/O ₅₃	I/O ₅₂	I/O ₅₁	I/O ₅₀	I/O ₃₉	I/O ₃₈	I/O ₃₇	I/O ₃₁	I/O ₅	I/O ₂	I/O ₂₆₁	V _{CC}	I/O ₂₄₆	I/O ₂₁₇	I/O ₂₁₈	I/O ₂₁₉	I/O ₂₁₂	I/O ₂₁₃	I/O ₂₁₄	I/O ₂₁₅
H	V _{CC}	V _{CC}	V _{CC}	I/O ₄₉	I/O ₄₈	I/O ₃₆	TCK	V _{CC}	I/O ₃₀	I/O ₁	I/O ₂₅₉	I/O ₂₆₀	V _{CC}	TDI	I/O ₂₁₆	I/O ₂₁₀	I/O ₂₁₁	V _{CC}	V _{CC}	V _{CC}
J	I/O ₅₉	I/O ₅₈	I/O ₅₇	I/O ₅₆	I/O ₅₅	I/O ₅₄	V _{CC}	I/O ₆₂	I/O ₆₀	I/O ₀	I/O ₂₅₈	I/O ₂₀₂	I/O ₂₀₃	CLK ₃ /I ₄	I/O ₂₀₄	I/O ₂₀₅	I/O ₂₀₆	I/O ₂₀₇	I/O ₂₀₈	I/O ₂₀₉
K	GND	GND	GND	GND	I/O ₆₅	I/O ₆₄	CLK ₀ /I ₀	I/O ₆₃	I/O ₆₁	GND	GND	I/O ₁₉₈	I/O ₁₉₉	CLK ₂ /I ₃	I/O ₂₀₀	I/O ₂₀₁	GND	GND	GND	GND
L	GND	GND	GND	GND	I/O ₆₉	I/O ₆₈	NC	I/O ₆₇	I/O ₆₆	GND	GND	I/O ₁₉₃	I/O ₁₉₅	I ₂	I/O ₁₉₆	I/O ₁₉₇	GND	GND	GND	GND
M	I/O ₈₉	I/O ₈₈	I/O ₈₇	I/O ₈₆	I/O ₈₅	I/O ₈₄	CLK ₁ /I ₁	I/O ₇₁	I/O ₇₀	I/O ₁₂₆	I/O ₁₃₂	I/O ₁₉₂	I/O ₁₉₄	V _{CC}	I/O ₁₇₄	I/O ₁₇₅	I/O ₁₇₆	I/O ₁₇₇	I/O ₁₇₈	I/O ₁₇₉
N	V _{CC}	V _{CC}	V _{CC}	I/O ₉₁	I/O ₉₀	I/O ₇₂	TMS	V _{CC}	I/O ₁₂₈	I/O ₁₂₇	I/O ₁₃₃	I/O ₁₆₂	V _{CC}	TDO	I/O ₁₈₀	I/O ₁₆₈	I/O ₁₆₉	V _{CC}	V _{CC}	V _{CC}
P	I/O ₉₅	I/O ₉₄	I/O ₉₃	I/O ₉₂	I/O ₇₅	I/O ₇₄	I/O ₇₃	I/O ₁₁₄	V _{CC}	I/O ₁₂₉	I/O ₁₃₄	I/O ₁₃₇	I/O ₁₆₃	I/O ₁₈₁	I/O ₁₈₂	I/O ₁₈₃	I/O ₁₇₀	I/O ₁₇₁	I/O ₁₇₂	I/O ₁₇₃
R	I/O ₉₀	I/O ₇₉	I/O ₇₈	I/O ₁₀₈	I/O ₇₇	I/O ₇₆	I/O ₁₁₅	I/O ₁₁₇	I/O ₁₂₀	I/O ₁₃₀	I/O ₁₃₅	I/O ₁₃₈	I/O ₁₆₄	I/O ₁₆₅	NC	I/O ₁₈₄	I/O ₁₈₅	I/O ₁₈₆	I/O ₁₈₉	I/O ₁₉₁
T	I/O ₈₂	I/O ₈₁	I/O ₁₁₀	I/O ₁₀₉	NC	I/O ₁₁₆	I/O ₁₁₈	I/O ₁₀₂	I/O ₁₂₁	I/O ₁₃₁	I/O ₁₃₆	I/O ₁₃₉	I/O ₁₅₆	I/O ₁₆₆	I/O ₁₆₇	NC	I/O ₁₅₄	I/O ₁₅₅	I/O ₁₈₇	I/O ₁₉₀
U	I/O ₈₃	NC	GND	I/O ₁₁₁	I/O ₁₁₂	I/O ₁₁₉	I/O ₁₀₄	I/O ₁₀₃	I/O ₁₂₂	GND	GND	I/O ₁₄₀	I/O ₁₅₇	I/O ₁₅₈	I/O ₁₅₀	I/O ₁₅₁	I/O ₁₅₃	GND	NC	I/O ₁₈₈
V	NC	GND	GND	GND	I/O ₁₁₃	I/O ₉₆	I/O ₁₀₅	V _{CC}	I/O ₁₂₃	GND	GND	I/O ₁₄₁	V _{CC}	I/O ₁₅₉	I/O ₁₄ 4	I/O ₁₅₂	GND	GND	GND	NC
W	GND	GND	GND	NC	I/O ₉₇	I/O ₉₉	I/O ₁₀₆	V _{CC}	I/O ₁₂₄	GND	GND	I/O ₁₄₂	V _{CC}	I/O ₁₆₀	I/O ₁₄₅	I/O ₁₄₇	NC	GND	GND	GND
Y	GND	GND	NC	I/O ₉₈	I/O ₁₀₀	I/O ₁₀₁	I/O ₁₀₇	V _{CC}	I/O ₁₂₅	GND	GND	I/O ₁₄₃	V _{CC}	I/O ₁₆₁	I/O ₁₄₆	I/O ₁₄₈	I/O ₁₄₉	NC	GND	GND

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-125BGC	BG388	388-Ball Plastic Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

3.3V Ordering Information

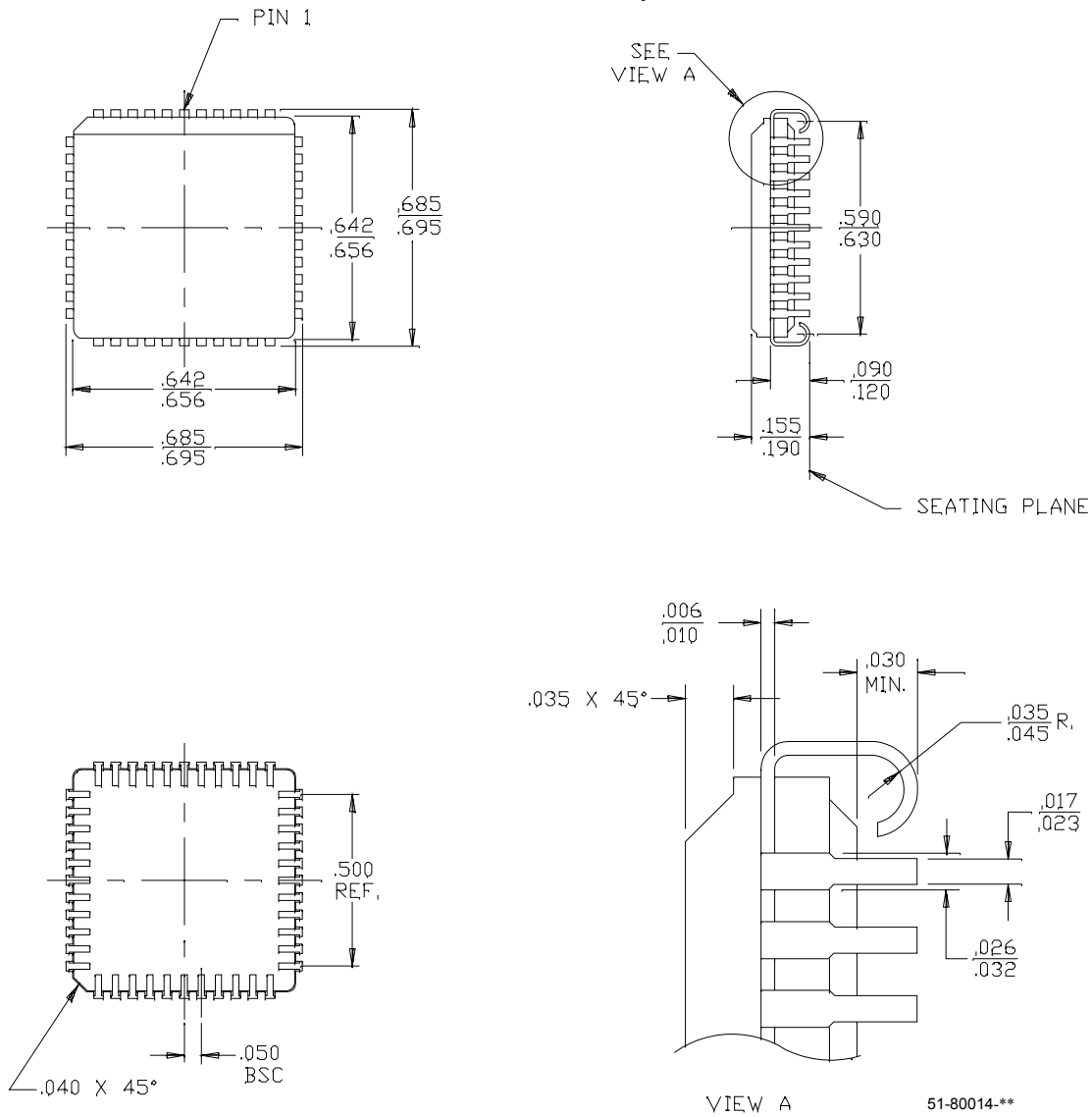
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-143BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAI	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP44-100JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	

3.3V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

Package Diagrams (continued)

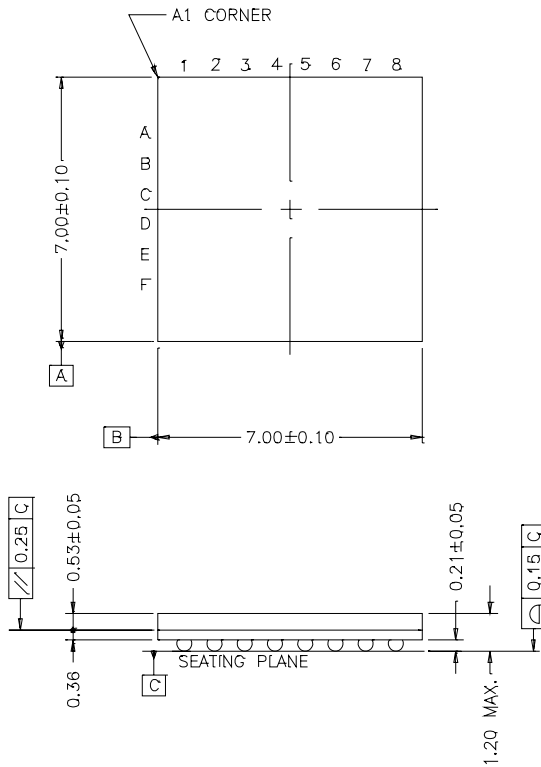
44-Lead Ceramic Leaded Chip Carrier Y67



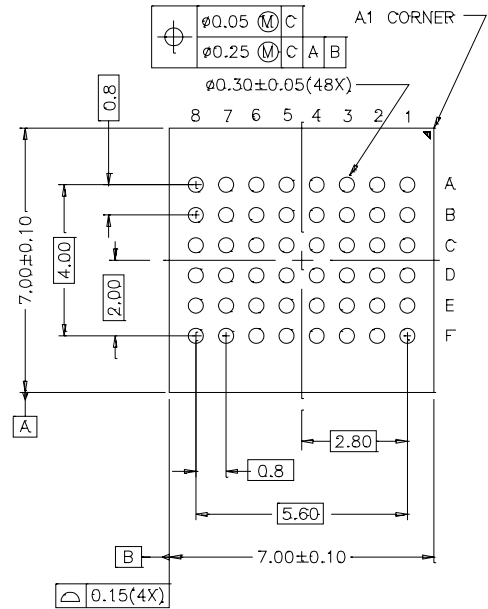
Package Diagrams (continued)

48-Ball (7.0 mm x 7.0 mm x 1.2 mm, 0.80 pitch) Thin BGA BA48D

TOP VIEW



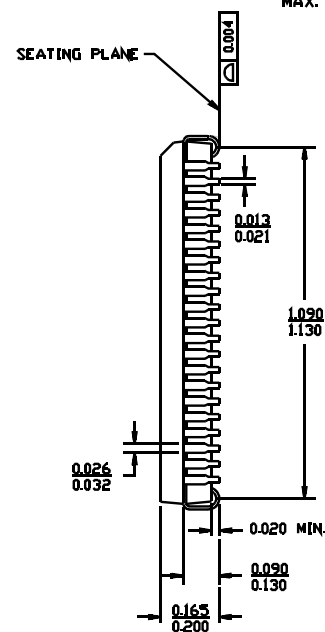
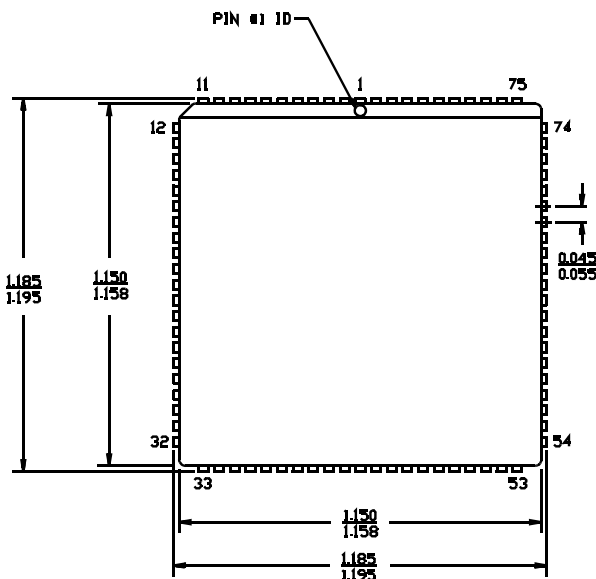
BOTTOM VIEW



51-85109-°C

84-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J83

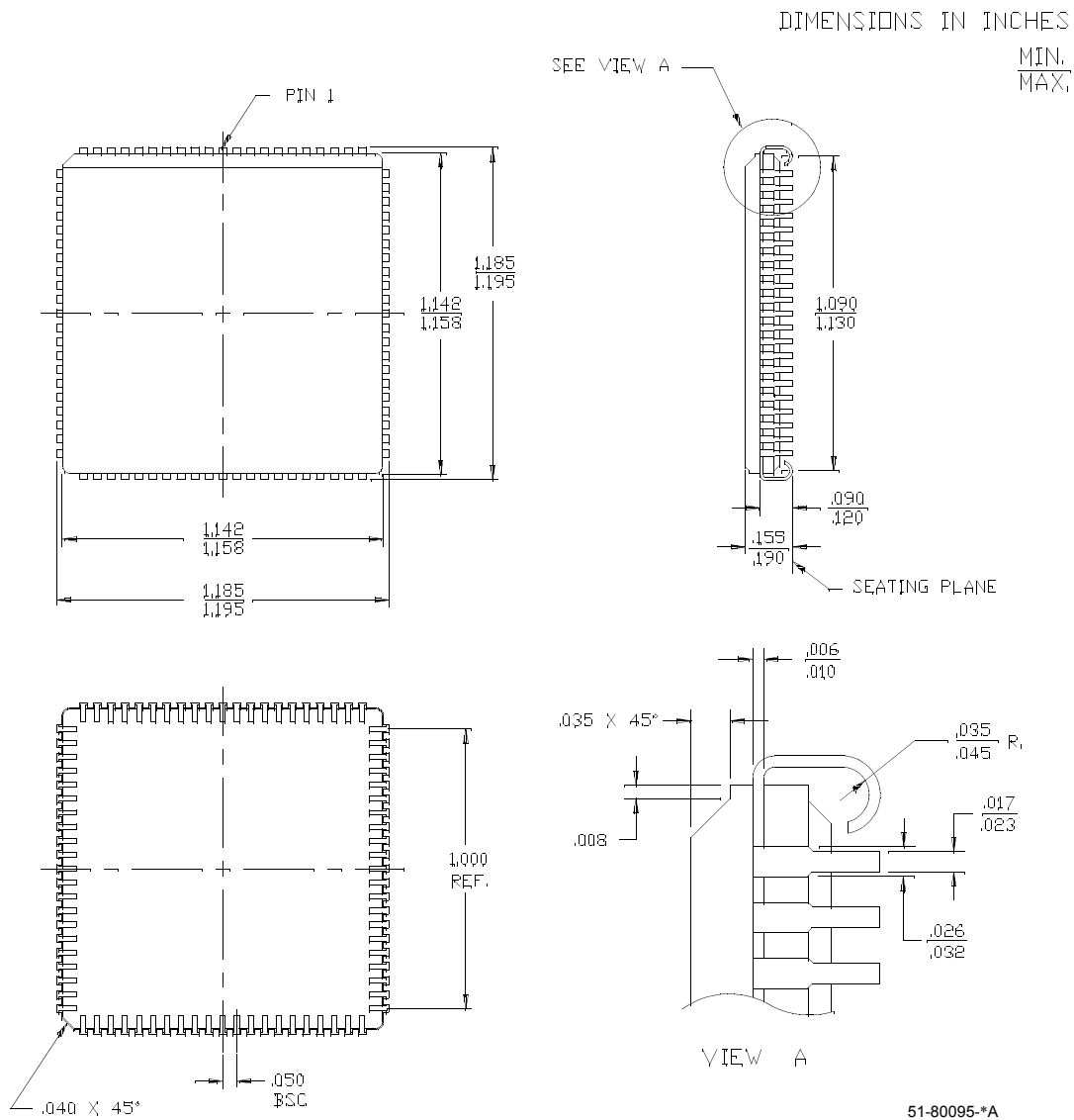
DIMENSIONS IN INCHES MIN. MAX.



51-85006-°A

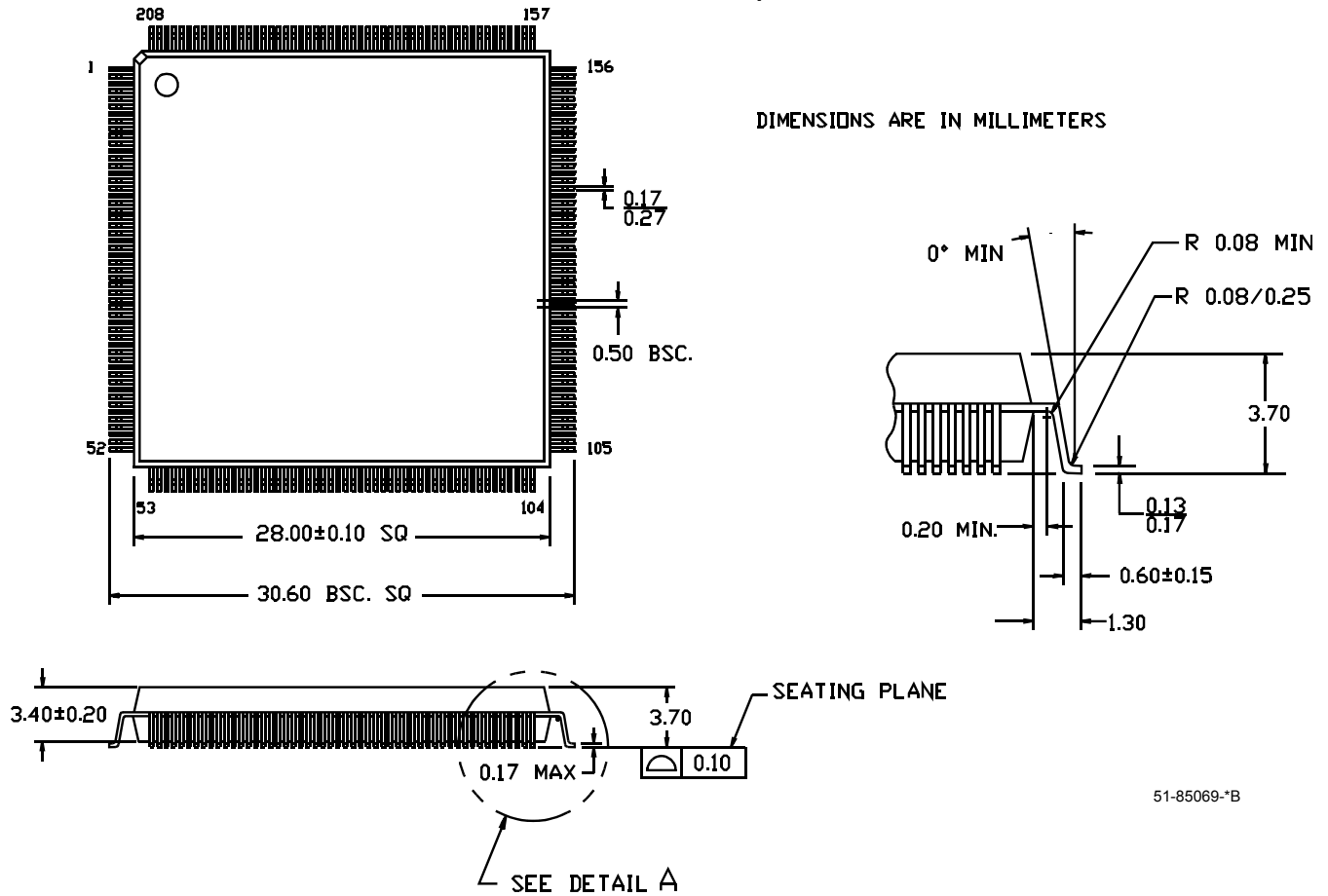
Package Diagrams (continued)

84-Lead Ceramic Leaded Chip Carrier Y84



Package Diagrams (continued)

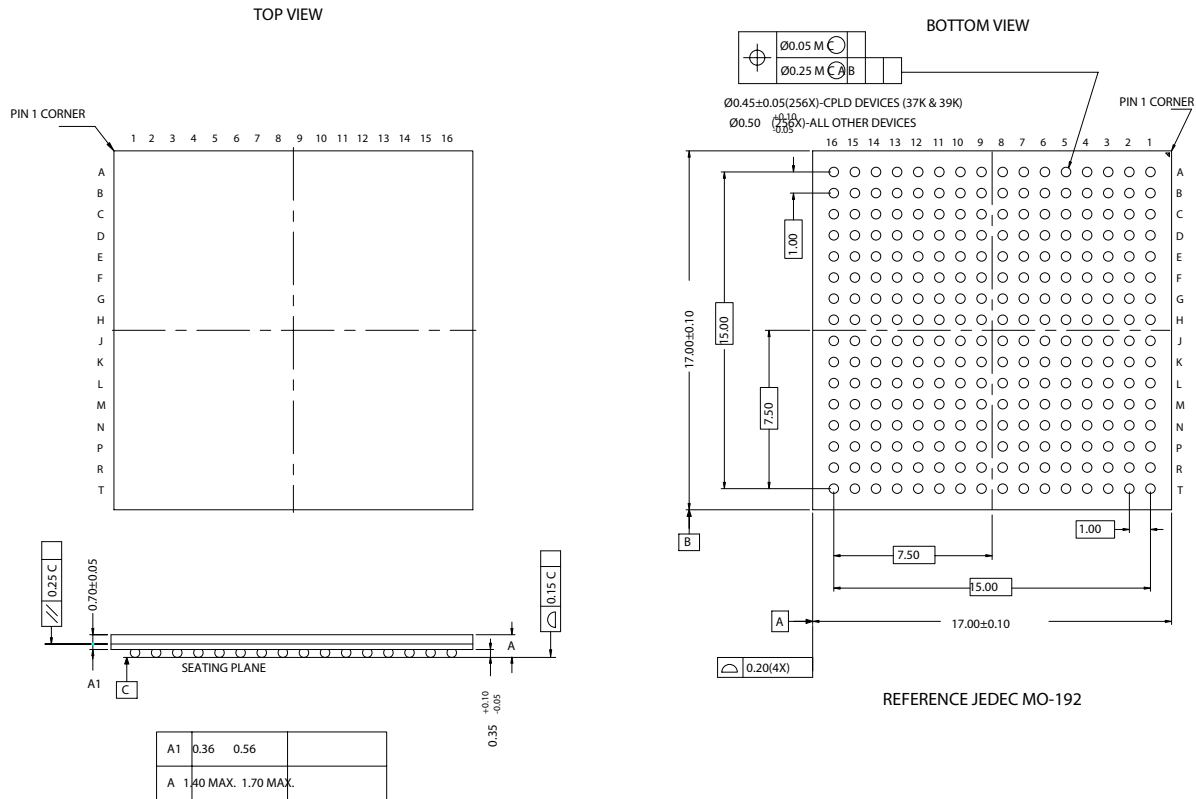
208-Lead Plastic Quad Flatpack N208



51-85069-*B

Package Diagrams (continued)

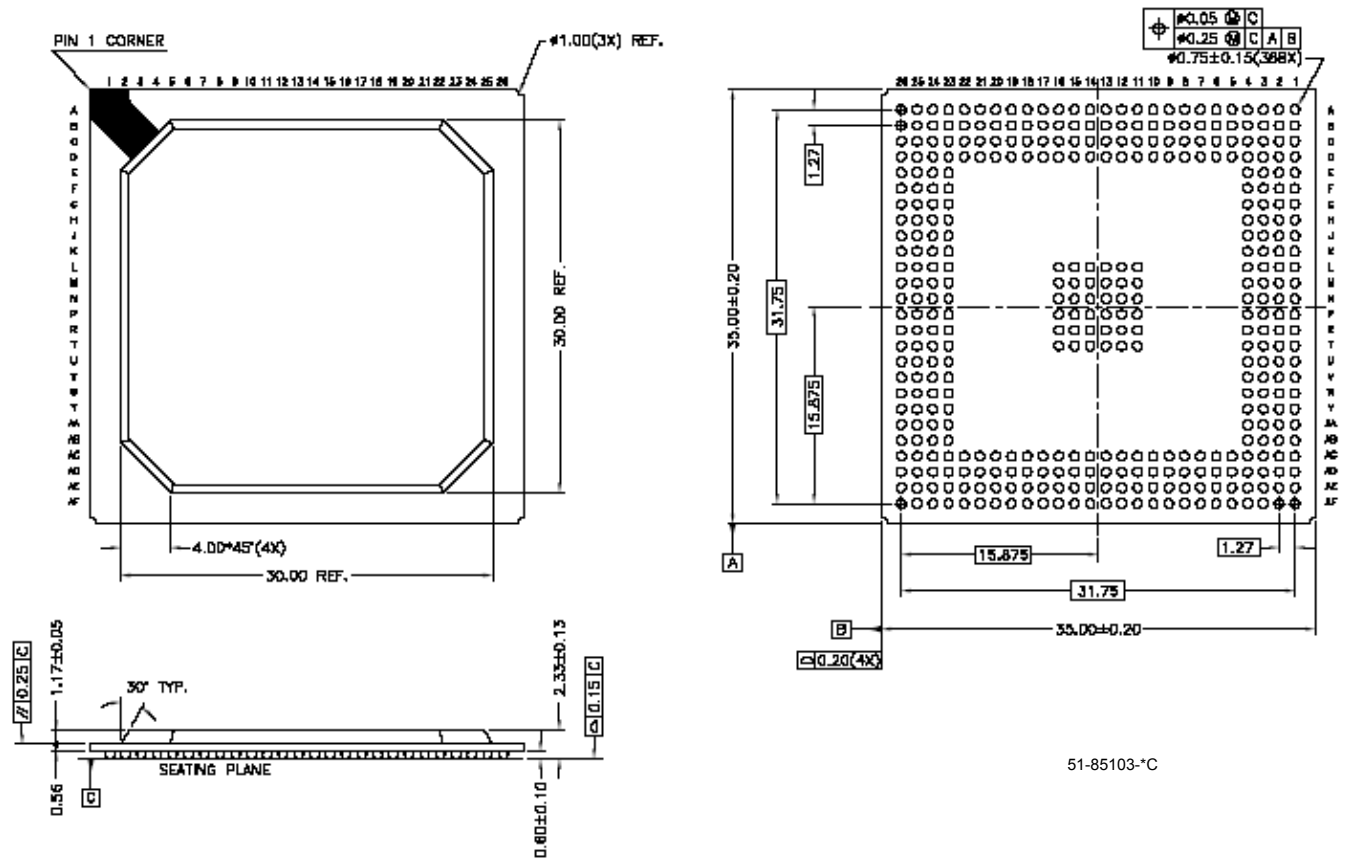
256-Ball FBGA (17 x 17 mm) BB256



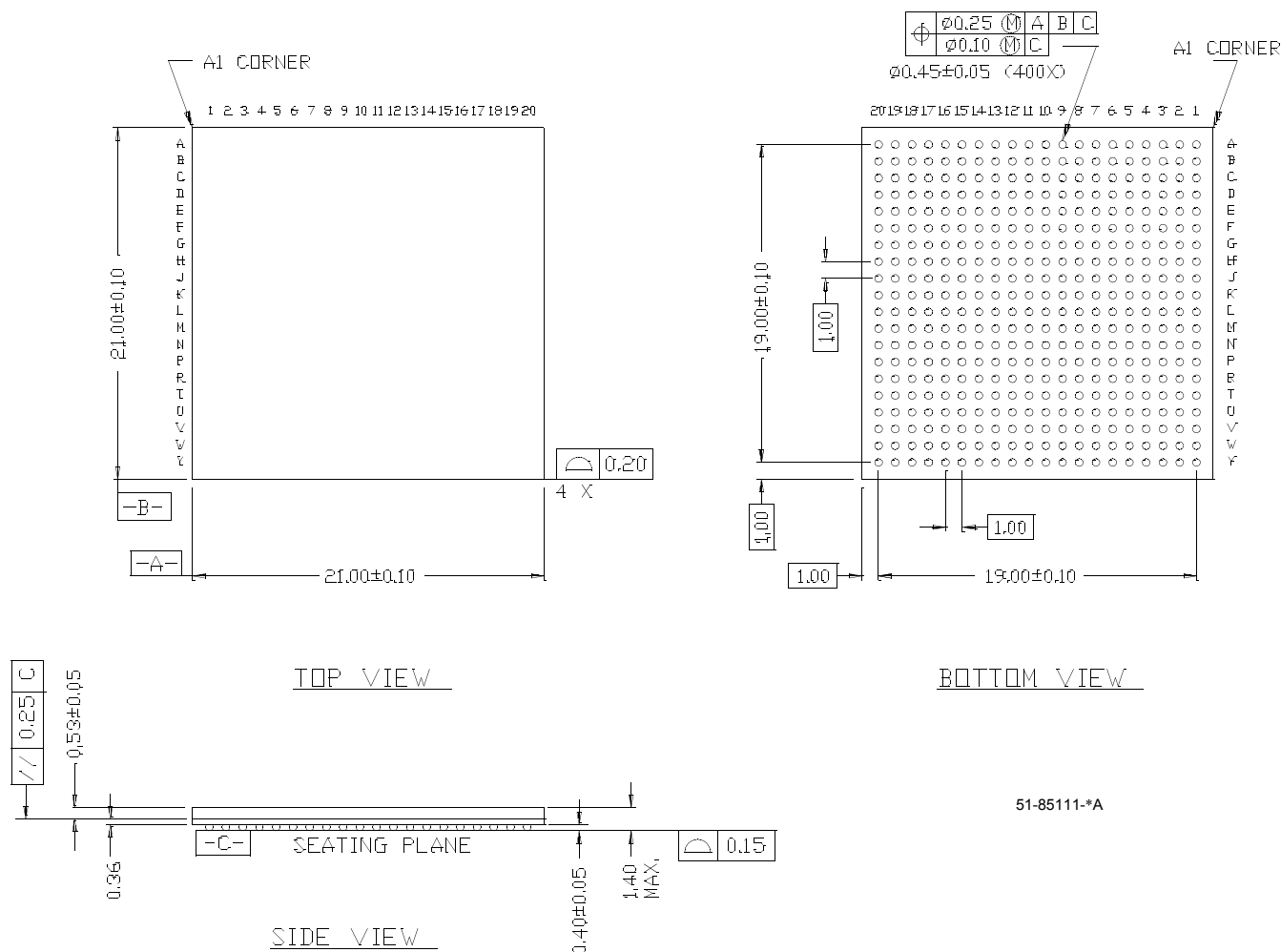
51-85108-7F

Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388



51-85103-°C

Package Diagrams (continued)
400-Ball FBGA (21 x 21 x 1.4 mm) BB400


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