Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	37
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37032vp44-100ac

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

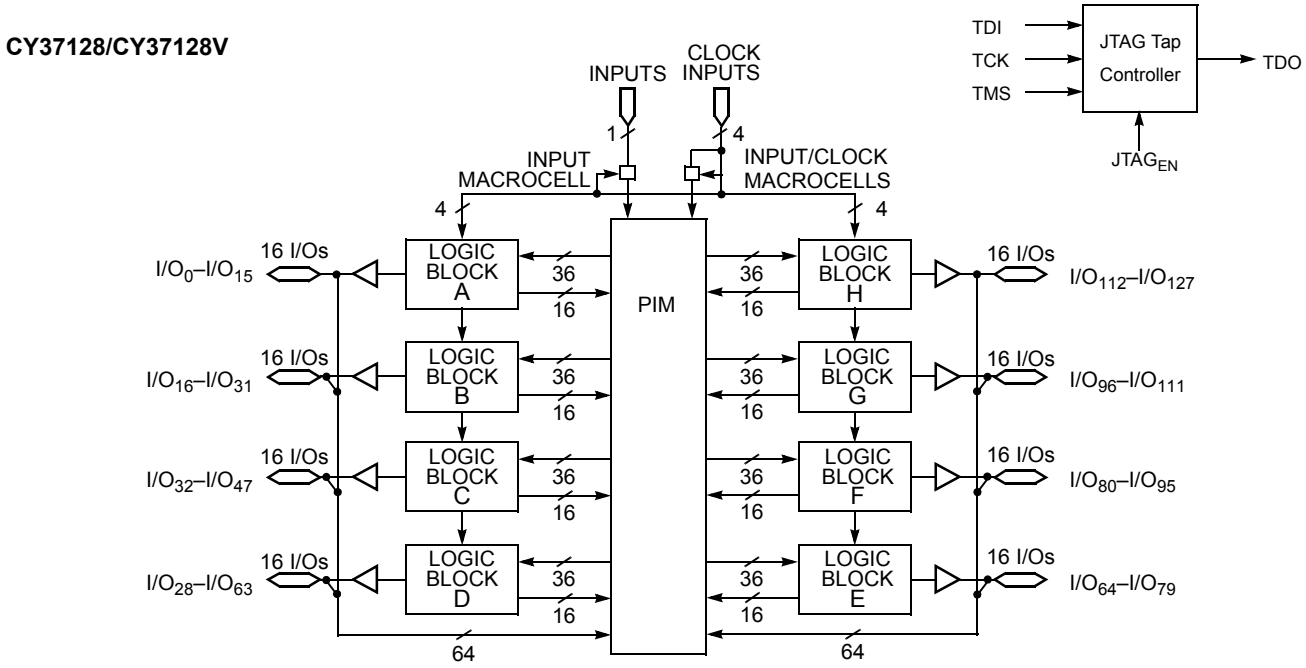
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

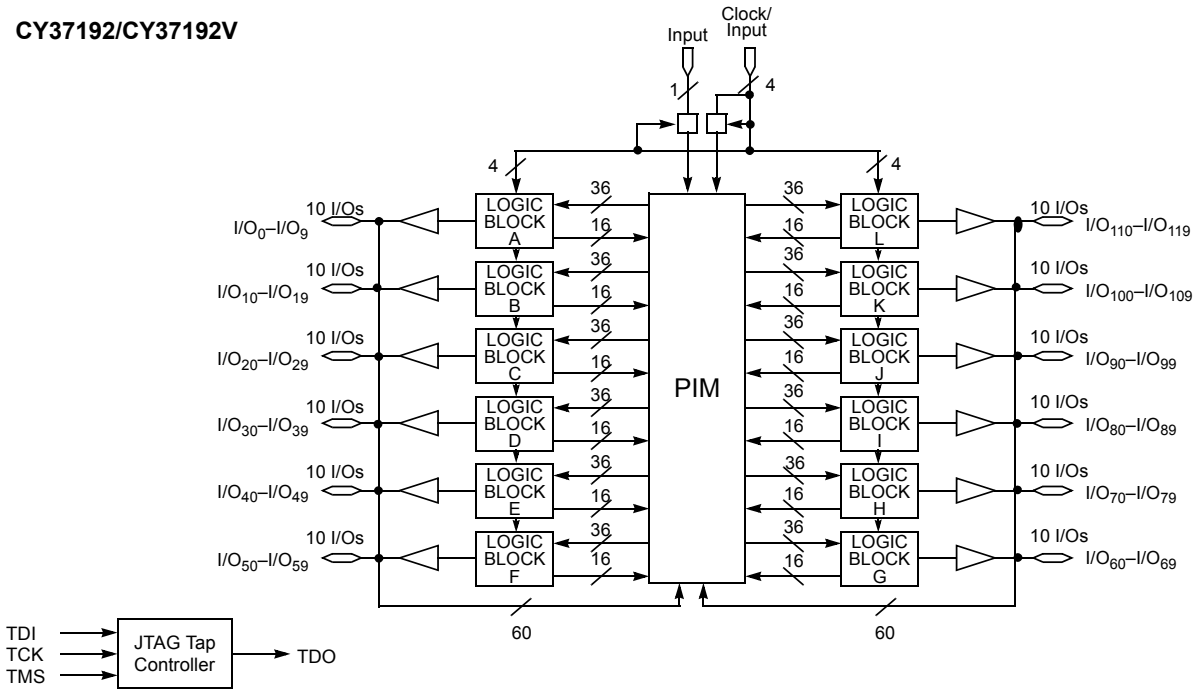
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams (continued)

CY37128/CY37128V

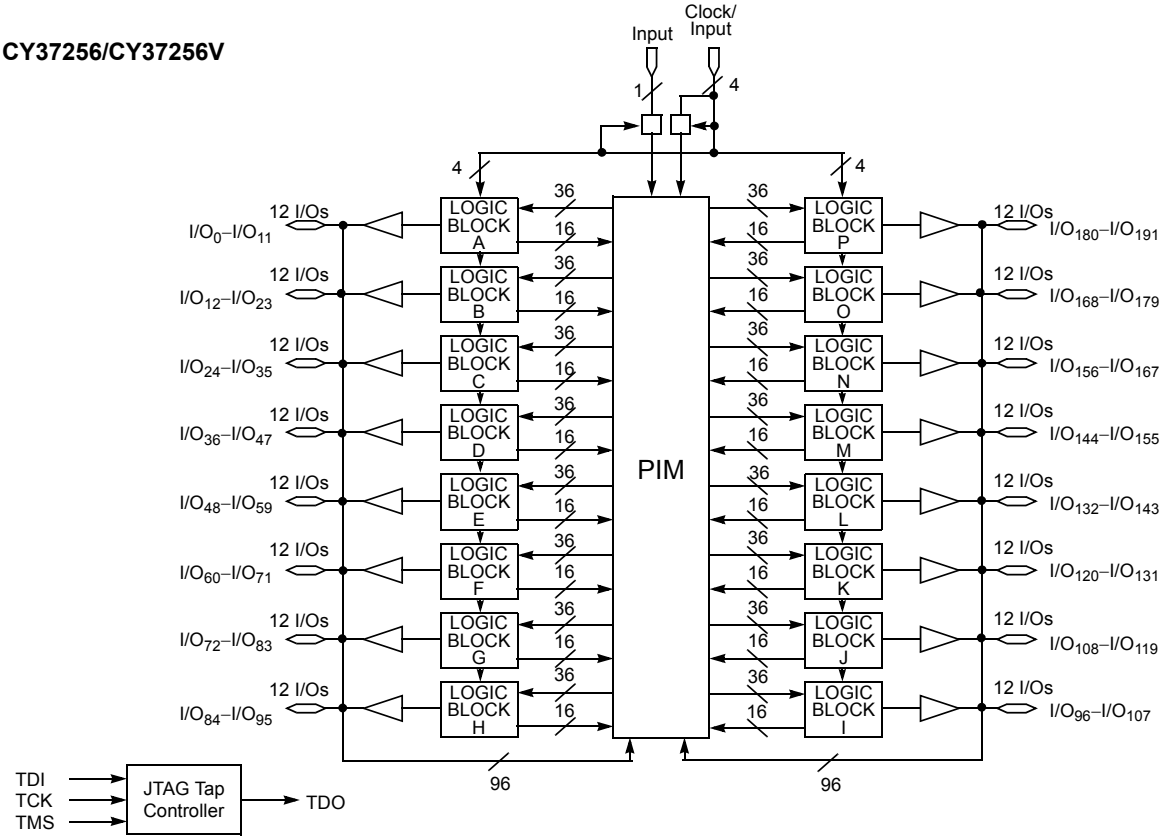


CY37192/CY37192V



Logic Block Diagrams (continued)

CY37256/CY37256V



Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual-Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

3.3V Device Characteristics Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 3.0 to 3.6V

Current into Outputs ..... 8 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}[10]
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Notes:
9. Dual pins are I/O with JTAG pins.
10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V± 0.16V.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

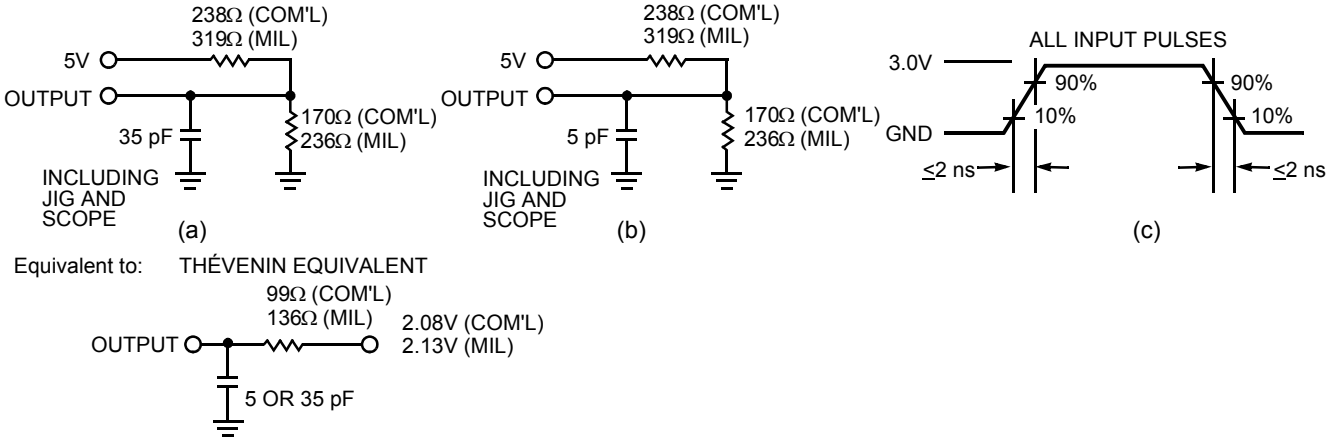
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

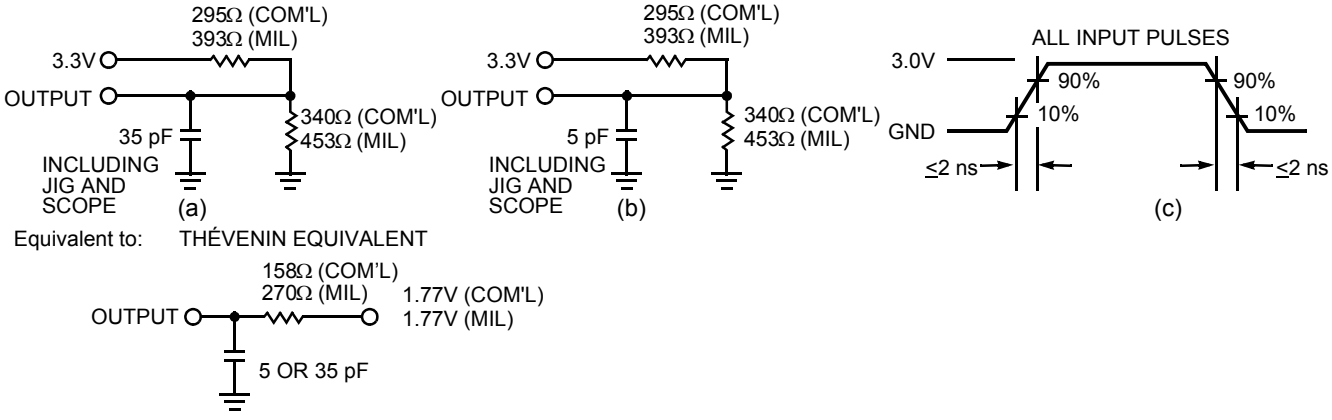
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

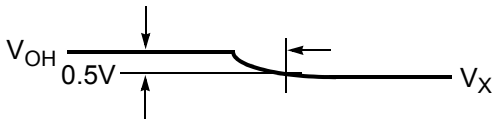
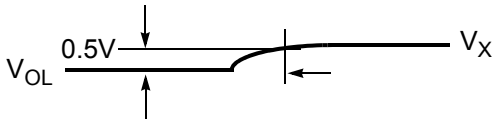
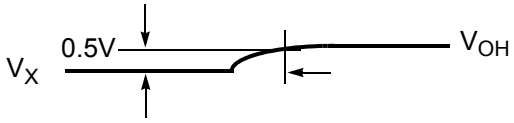
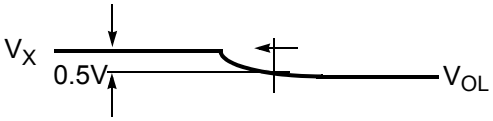
AC Characteristics

5.0V AC Test Loads and Waveforms



3.3V AC Test Loads and Waveforms



Parameter[11]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Switching Characteristics Over the Operating Range [12]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t_{PD}[13, 14, 15]	Input to Combinatorial Output	ns
t_{PDL}[13, 14, 15]	Input to Output Through Transparent Input or Output Latch	ns
t_{PDLL}[13, 14, 15]	Input to Output Through Transparent Input and Output Latches	ns
t_{EA}[13, 14, 15]	Input to Output Enable	ns
t_{ER}[11, 13]	Input to Output Disable	ns
Input Register Parameters		
t_{WL}	Clock or Latch Enable Input LOW Time[8]	ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	ns
t_{IS}	Input Register or Latch Set-up Time	ns
t_{IH}	Input Register or Latch Hold Time	ns
t_{ICO}[13, 14, 15]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t_{ICOL}[13, 14, 15]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t_{CO}[14, 15]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output	ns
t_S[13]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_H	Register or Latch Data Hold Time	ns
t_{CO2}[13, 14, 15]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t_{SCS}[13]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	ns
t_{SL}[13]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns

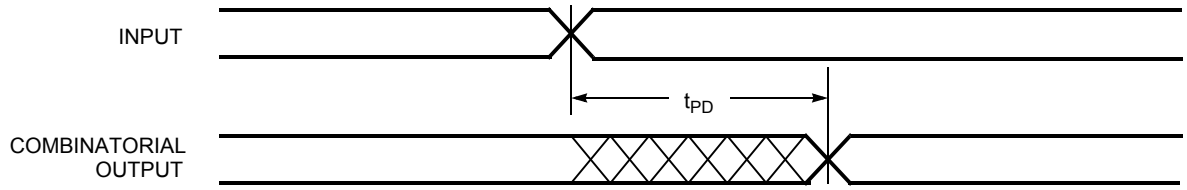
Notes:
11. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
12. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
13. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
14. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
15. When V_{CCO} = 3.3V, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range (continued)[12]

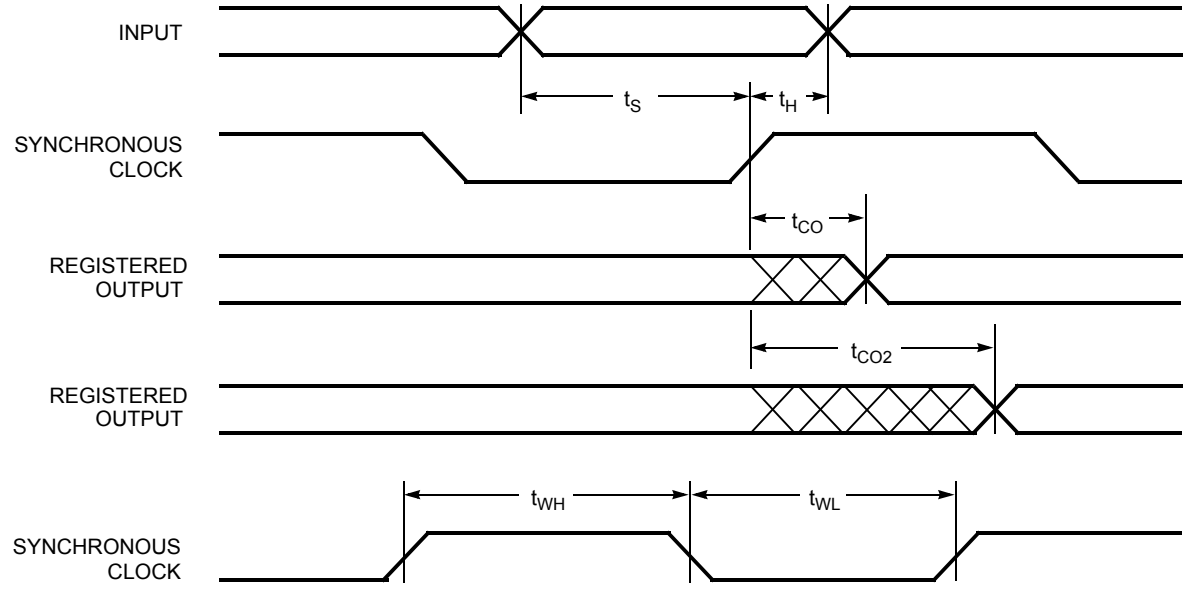
Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RO}[13, 14, 15]		12		13		13		14		15		18		21		26	ns
t_{PW}	8		8		8		8		10		12		15		20		ns
t_{PR}[13]	10		10		10		10		12		14		17		22		ns
t_{PO}[13, 14, 15]		12		13		13		14		15		18		21		26	ns
User Option Parameters																	
t_{LP}		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{SLEW}		3		3		3		3		3		3		3		3	ns
$t_{3.3IO}$[19]		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
JTAG Timing Parameters																	
$t_{S\ JTAG}$	0		0		0		0		0		0		0		0		ns
$t_{H\ JTAG}$	20		20		20		20		20		20		20		20		ns
$t_{CO\ JTAG}$		20		20		20		20		20		20		20		20	ns
f_{JTAG}		20		20		20		20		20		20		20		20	MHz

Switching Waveforms

Combinatorial Output



Registered Output with Synchronous Clocking

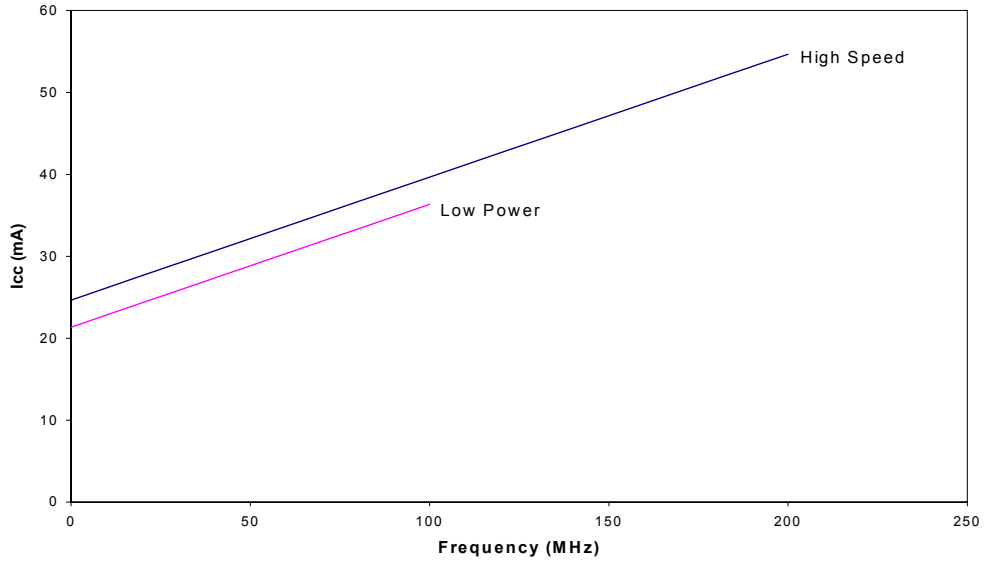


Note:
19. Only applicable to the 5V devices.

Power Consumption

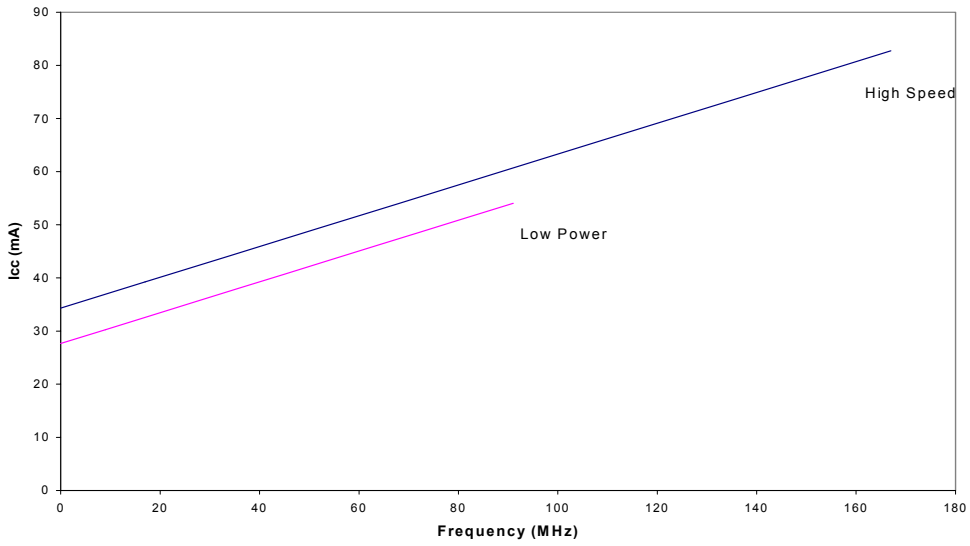
Typical 5.0V Power Consumption

CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

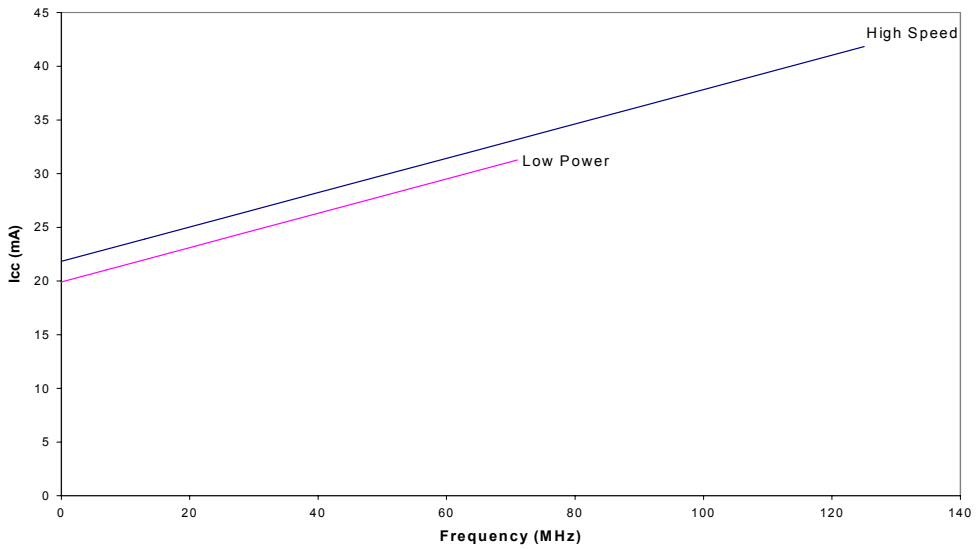
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

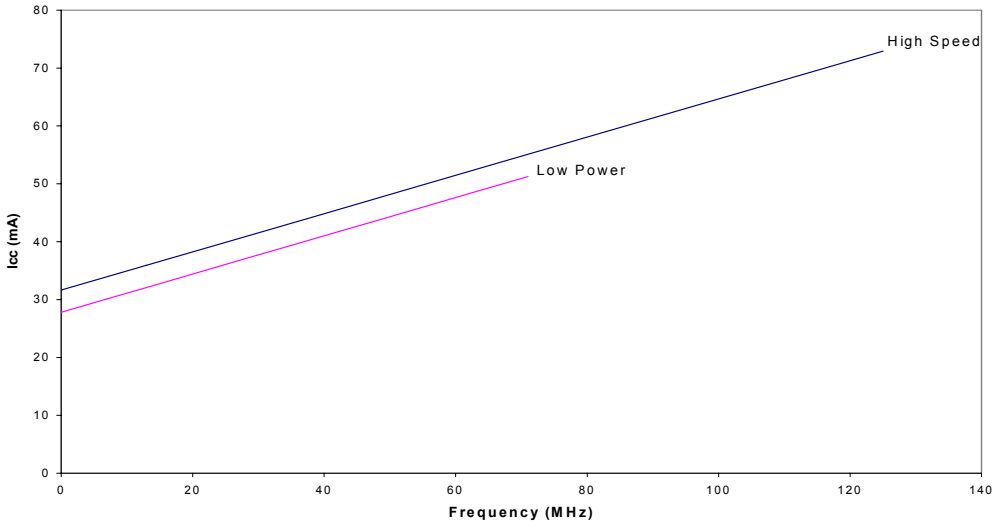
Typical 3.3V Power Consumption (continued)

CY37064V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

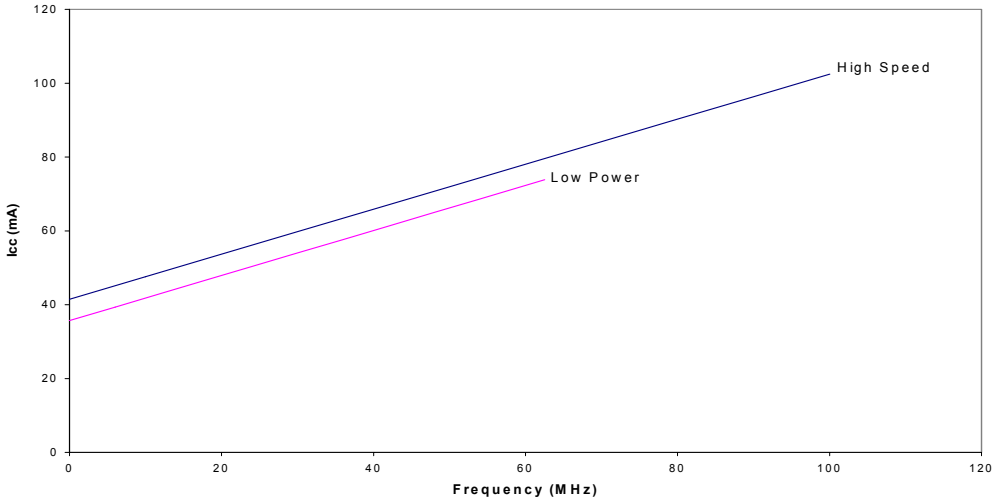
CY37128V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

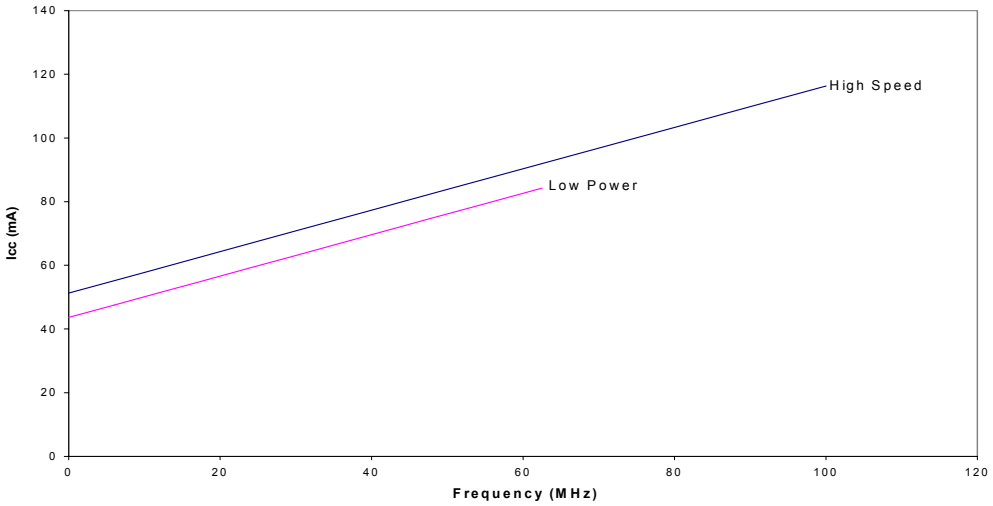
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

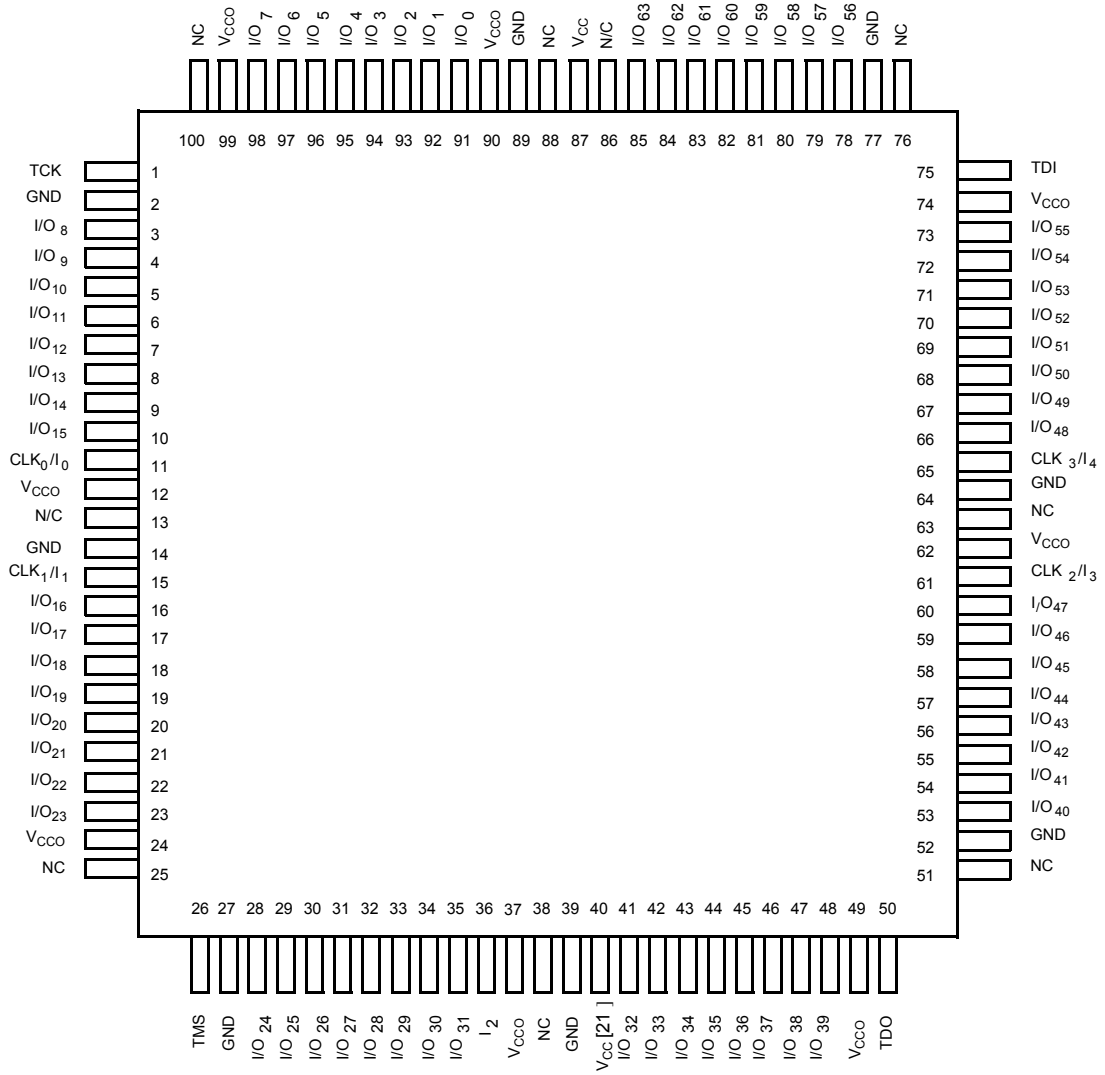
CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

Pin Configurations[20] (continued)

100-lead TQFP (A100)
Top View



Pin Configurations[20] (continued)

256-Ball Fine-Pitch BGA (BB256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	I/O_{26}	I/O_{24}	I/O_{20}	V_{CC}	I/O_{11}	GND	GND	I/O_{186}	V_{CC}	I/O_{177}	I/O_{172}	I/O_{167}	GND	GND
B	GND	I/O_{27}	I/O_{25}	I/O_{23}	I/O_{19}	I/O_{15}	I/O_{10}	GND	GND	I/O_{185}	I/O_{181}	I/O_{176}	I/O_{171}	I/O_{166}	I/O_{165}	GND
C	I/O_{29}	I/O_{28}	NC	I/O_{22}	I/O_{18}	I/O_{14}	I/O_{9}	I/O_{4}	I/O_{191}	I/O_{184}	I/O_{180}	I/O_{175}	I/O_{170}	NC	I/O_{163}	I/O_{164}
D	I/O_{32}	I/O_{31}	I/O_{30}	NC	I/O_{17}	I/O_{13}	I/O_{8}	I/O_{3}	I/O_{190}	I/O_{183}	I/O_{179}	I/O_{174}	I/O_{169}	I/O_{160}	I/O_{161}	I/O_{162}
E	I/O_{35}	I/O_{34}	I/O_{33}	I/O_{21}	I/O_{16}	I/O_{12}	I/O_{7}	I/O_{2}	I/O_{189}	V_{CC}	I/O_{178}	I/O_{173}	I/O_{168}	I/O_{157}	I/O_{158}	I/O_{159}
F	V_{CC}	I/O_{38}	I/O_{37}	I/O_{36}	TCK	V_{CC}	I/O_{6}	I/O_{1}	I/O_{188}	I/O_{182}	V_{CC}	TDI	I/O_{154}	I/O_{155}	I/O_{156}	V_{CC}
G	I/O_{43}	I/O_{42}	I/O_{41}	I/O_{40}	V_{CC}	I/O_{39}	I/O_{5}	I/O_{0}	I/O_{187}	I/O_{148}	I/O_{149}	CLK_3 /I_4	I/O_{150}	I/O_{151}	I/O_{152}	I/O_{153}
H	GND	GND	I/O_{47}	I/O_{46}	CLK_0 /I_0	I/O_{45}	I/O_{44}	GND	GND	I/O_{144}	I/O_{145}	CLK_2 /I_3	I/O_{146}	I/O_{147}	GND	GND
J	GND	GND	I/O_{51}	I/O_{50}	NC	I/O_{49}	I/O_{48}	GND	GND	I/O_{140}	I/O_{141}	I_2	I/O_{142}	I/O_{143}	GND	GND
K	I/O_{57}	I/O_{56}	I/O_{55}	I/O_{54}	CLK_1 /I_1	I/O_{53}	I/O_{52}	I/O_{91}	I/O_{96}	I/O_{101}	I/O_{135}	V_{CC}	I/O_{136}	I/O_{137}	I/O_{138}	I/O_{139}
L	V_{CC}	I/O_{60}	I/O_{59}	I/O_{58}	TMS	V_{CC}	I/O_{86}	I/O_{92}	I/O_{97}	I/O_{102}	V_{CC}	TDO	I/O_{132}	I/O_{133}	I/O_{134}	V_{CC}
M	I/O_{63}	I/O_{62}	I/O_{61}	I/O_{72}	I/O_{77}	I/O_{82}	V_{CC}	I/O_{93}	I/O_{98}	I/O_{103}	I/O_{108}	I/O_{112}	I/O_{117}	I/O_{129}	I/O_{130}	I/O_{131}
N	I/O_{66}	I/O_{65}	I/O_{64}	I/O_{73}	I/O_{78}	I/O_{83}	I/O_{87}	I/O_{94}	I/O_{99}	I/O_{104}	I/O_{109}	I/O_{113}	NC	I/O_{126}	I/O_{127}	I/O_{128}
P	I/O_{68}	I/O_{67}	NC	I/O_{74}	I/O79	I/O_{84}	I/O_{88}	I/O_{95}	I/O_{100}	I/O_{105}	I/O_{110}	I/O_{114}	I/O_{118}	NC	I/O_{124}	I/O_{125}
R	GND	I/O_{69}	I/O_{70}	I/O_{75}	I/O_{80}	I/O_{85}	I/O_{89}	GND	GND	I/O_{106}	I/O_{111}	I/O_{115}	I/O_{119}	I/O_{121}	I/O_{123}	GND
T	GND	GND	I/O_{71}	I/O_{76}	I/O_{81}	V_{CC}	I/O_{90}	GND	GND	I/O_{107}	V_{CC}	I/O_{116}	I/O_{120}	I/O_{122}	GND	GND

3.3V Ordering Information (continued)

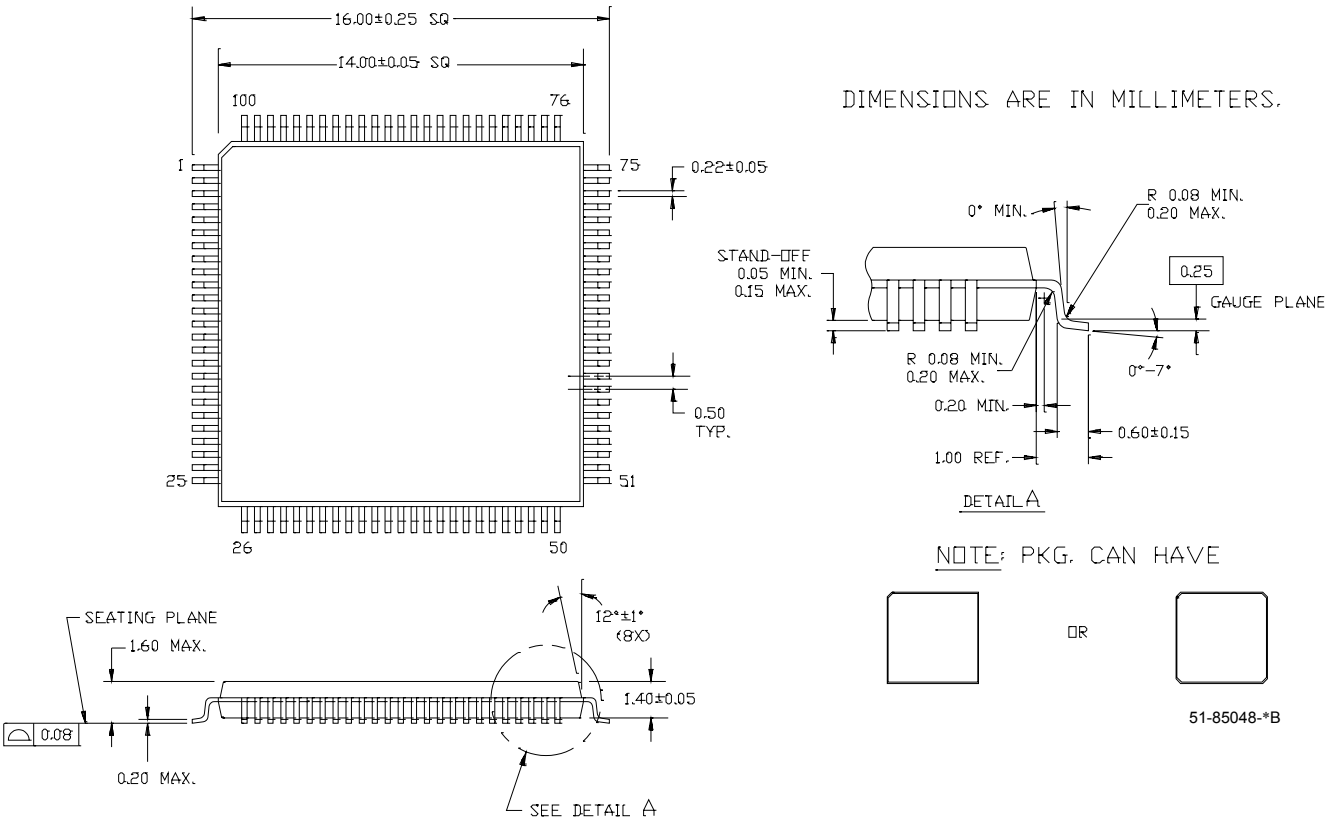
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	143	CY37064VP44-143AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-143BAC	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-143AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-143AXC	A100	100-Lead Lead Free Thin Quad Flatpack	
		CY37064VP100-143BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
	100	CY37064VP44-100AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-100BAC	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100AXC	A100	100-Lead Lead Free Thin Quad Flatpack	
		CY37064VP100-100BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37064VP44-100AI	A44	44-Lead Thin Quad Flatpack	Industrial
		CY37064VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-100BAI	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100BBI	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100AI	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100AXI	A100	100-Lead Lead Free Thin Quad Flatpack	
		5962-9952001QYA	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
128	125	CY37128VP100-125AC	A100	100-Lead Thin Quad Flat Pack	Commercial
		CY37128VP100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-125BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37128VP160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	83	CY37128VP100-83AC	A100	100-Lead Thin Quad Flat Pack	Commercial
		CY37128VP100-83AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-83AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83AI	A100	100-Lead Thin Quad Flat Pack	Industrial
		CY37128VP100-83AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83BBI	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-83AI	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		5962-9952201QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	100	CY37192VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37192VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial

3.3V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

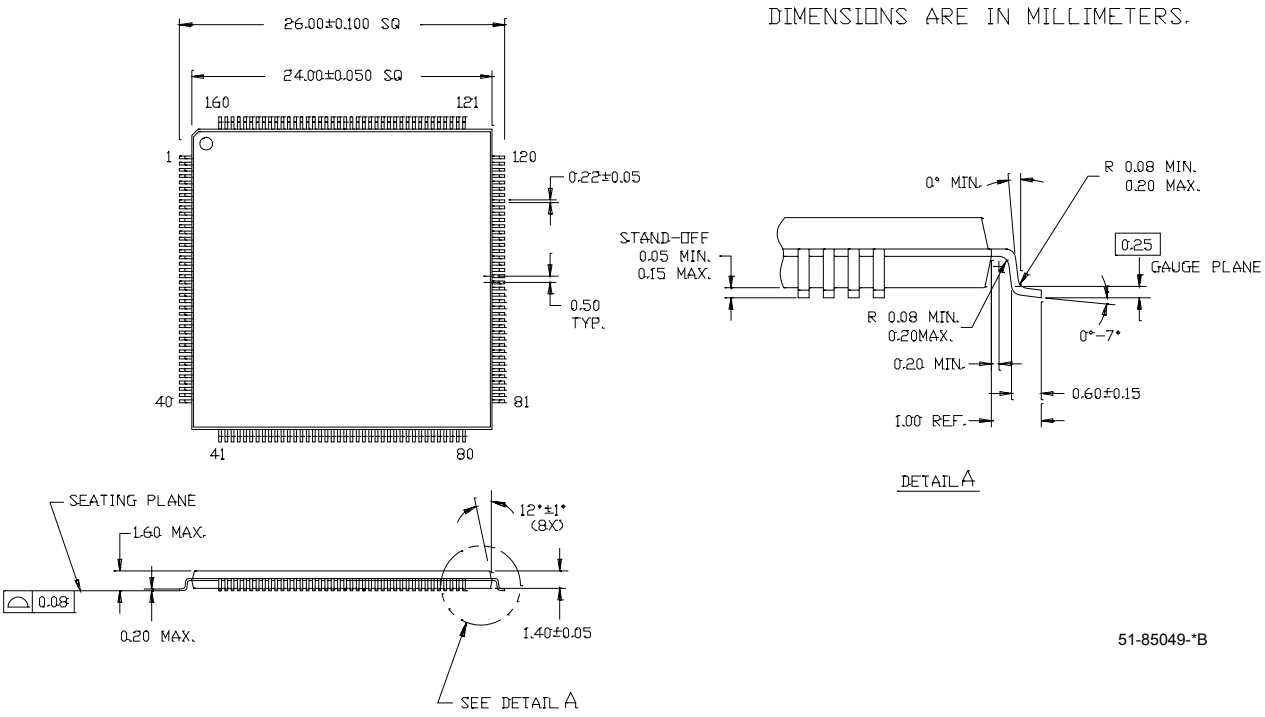
Package Diagrams (continued)

100-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (TQFP) A100



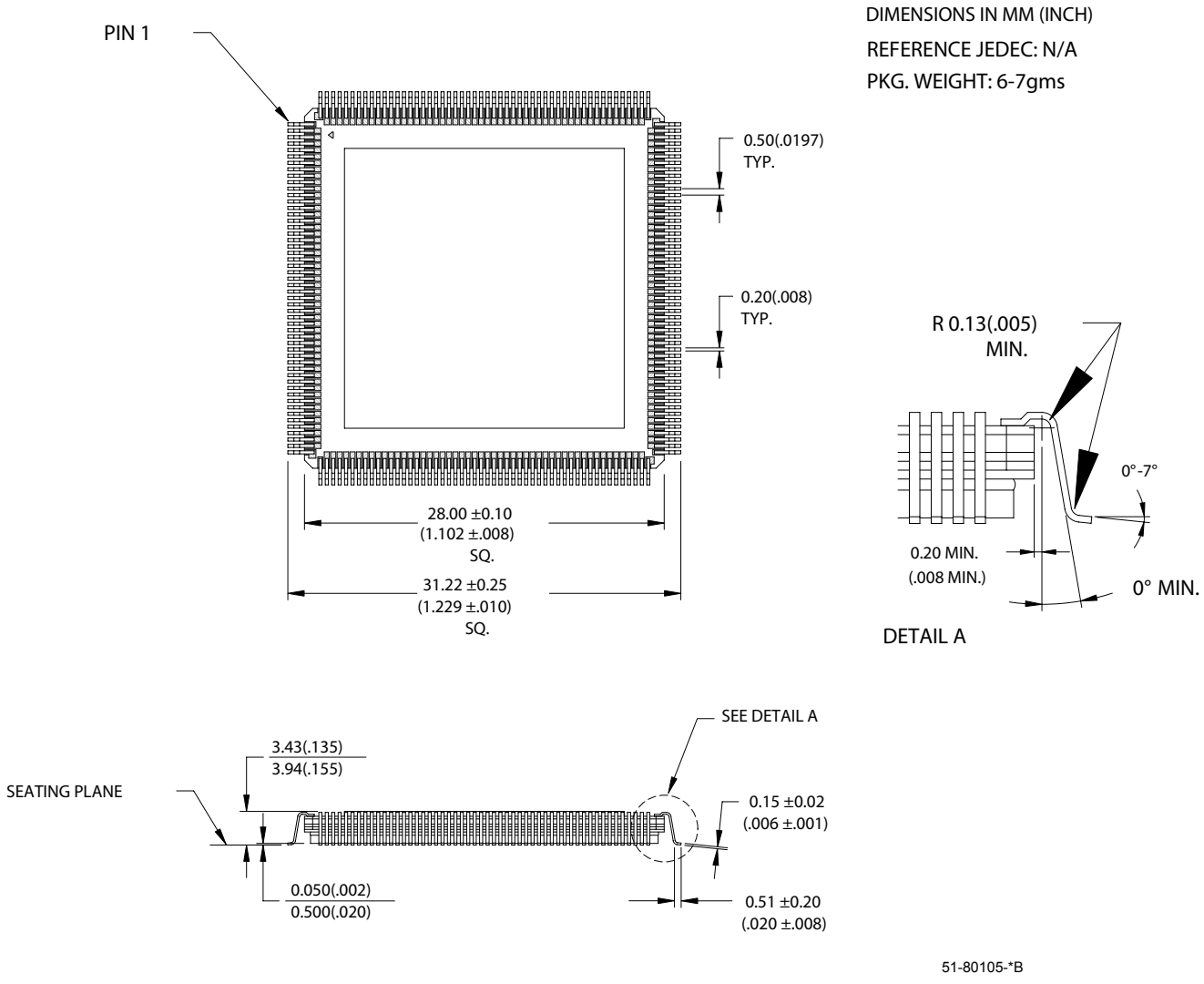
Package Diagrams (continued)

160-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (24 x 24 x 1.4 mm) (TQFP) A160



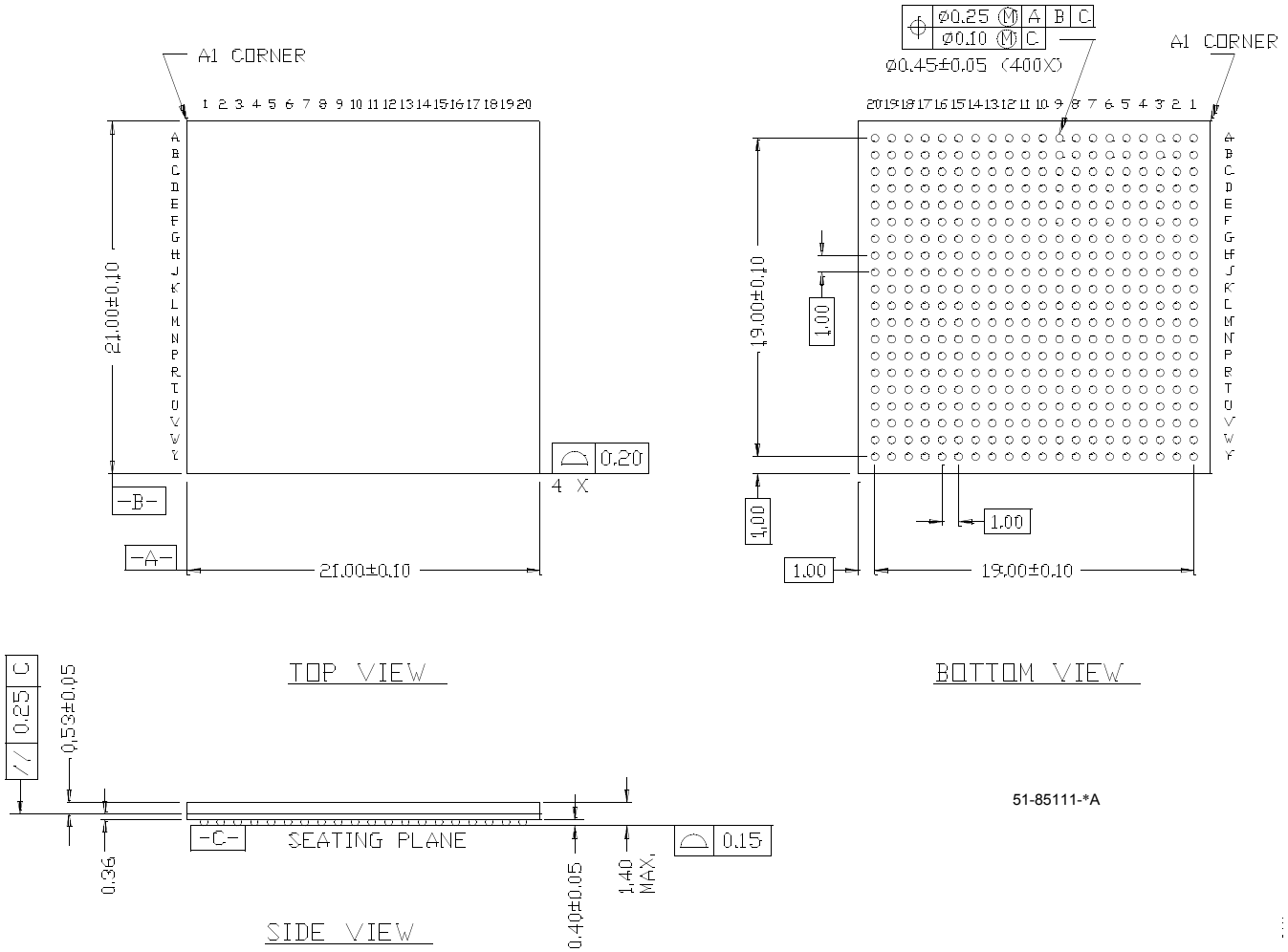
Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208



Package Diagrams (continued)

400-Ball FBGA (21 x 21 x 1.4 mm) BB400



Addendum

3.3V Operating Range

(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.16V

Document History Page

Document Title: Ultra37000 CPLD Family 5V, 3.3V, ISR™ High-Performance CPLDs Document Number: 38-03007				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106272	04/18/01	SZV	Change from Spec number: 38-00475 to 38-03007
*A	124942	03/21/03	OOR	Updated 3.3V V_{CC} requirements for –144 speeds Added an Addendum
*B	126262	05/09/03	TEH	Changed pinout for CY37128V BB100 package
*C	128125	07/16/03	HOM	Obsoleted following 3.3V PLCC packaged devices: CY37032VP44-143JC CY37032VP44-100JC CY37032VP44-100JI CY37064VP44-143JC CY37064VP84-143JC CY37064VP44-100JC CY37064VP84-100JC CY37064VP44-100JI CY37064VP84-100JI CY37128VP84-125JC CY37128VP84-83JC CY37128VP84-83JI
*D	282709	See ECN	YDT	Changed package diagrams and labels for consistency Added Lead (Pb)-free logo on first page, as well as a note in Features Added Lead (Pb)-free package diagram labels Added Lead-free Parts to Ordering Information CY37032P44-200AXC, CY37032P44-200JXC, CY37032P44-154AXI, CY37032P44-154JXI, CY37032P44-125AXC, CY37032P44-125JXC, CY37064P44-200AXC, CY37064P44-200JXC, CY37064P100-200AXC, CY37064P44-154AXI, CY37064P44-154JXI, CY37064P44-125AXC, CY37064P44-125JXC, CY37064P100-125AXC, CY37064P44-125AXI, CY37064P100-125AXI, CY37128P84-167JXC, CY37128P100-167AXC, CY37128P160-167AXC, CY37128P84-125JXC, CY37128P100-125AXC, CY37128P160-125AXC, CY37128P84-125JXI, CY37128P100-125AXI, CY37128P160-125AXI, CY37128P84-100JXC, CY37128P100-100AXC, CY37128P160-100AXC, CY37128P100-100AXI, CY37192P160-154AXC, CY37192P160-125AXC, CY37192P160-125AXI, CY37192P160-83AXC, CY37192P160-83AXI, CY37256P160-154AXC, CY37256P160-125AXC, CY37256P160-125AXI, CY37256P160-83AXC, CY37256P160-83AXI, CY37032VP44-143AXC, CY37032VP44-100AXC, CY37032VP44-100AXI, CY37032VP44-100JXI, CY37064VP44-143AXC, CY37064VP100-143AXC, CY37064VP44-100AXC, CY37064VP100-100AXC, CY37064VP44-100AXI, CY37064VP100-100AXI, CY37128VP100-125AXC, CY37128VP160-125AXC, CY37128VP160-125AXI, CY37128VP100-83AXC, CY37128VP160-83AXC, CY37128VP100-83AXI, CY37128VP160-83AXI, CY37192VP160-100AXC, CY37192VP160-66AXC, CY37256VP160-100AXC, CY37256VP160-100AXI, CY37256VP160-66AXC
*E	321635	See ECN	PCX	Added Package Diagram BG292 Updated all PBGA package type information (BG292 & BG388)