Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) Flash
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	69
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37064p100-125axi

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V					X		X	
CY37192V						X		X
CY37256V						X		X
CY37384V							X	X
CY37512V							X	X

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead CLCC	48-Lead FBGA	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	256-Lead FBGA	388-Lead PBGA	400-Lead FBGA
CY37032V	37		37											
CY37064V	37	37	37		69	69								
CY37128V				69	69	85	133							
CY37192V							125							
CY37256V							133	133	165		197	197		
CY37384V									165		197			
CY37512V									165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The PIM consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*® and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note *Understanding Bus-Hold—A Feature of Cypress CPLDs*.

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.
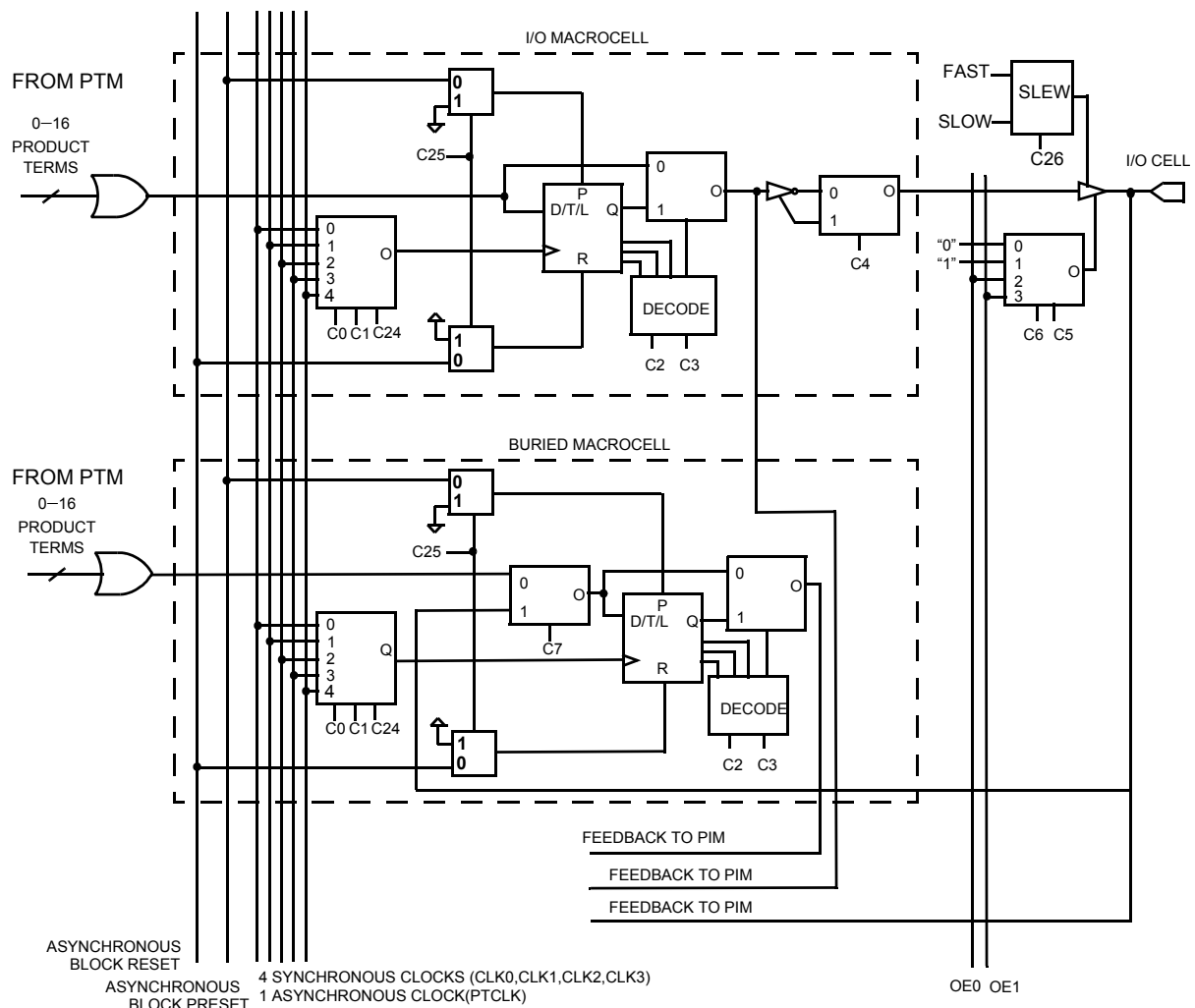

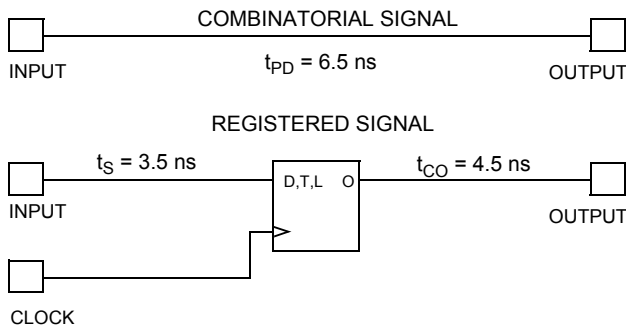**Figure 2. I/O and Buried Macrocells**

Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.
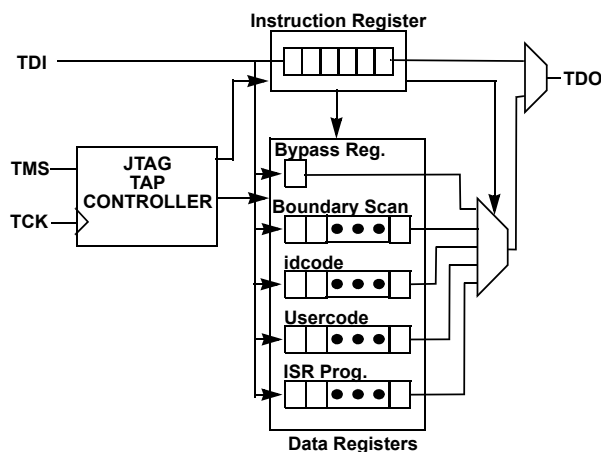

Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing

resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC, *Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual-Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

3.3V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied..–55°C to +125°C

Supply Voltage to Ground Potential ....–0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State...–0.5V to +7.0V

DC Input Voltage ....–0.5V to +7.0V

DC Program Voltage... 3.0 to 3.6V

Current into Outputs .... 8 mA

Static Discharge Voltage...> 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current...> 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}[10]
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	μA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	μA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		μA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		μA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	μA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	μA

Notes:
9. Dual pins are I/O with JTAG pins.
10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V± 0.16V.

Switching Waveforms (continued)

Latched Input and Output
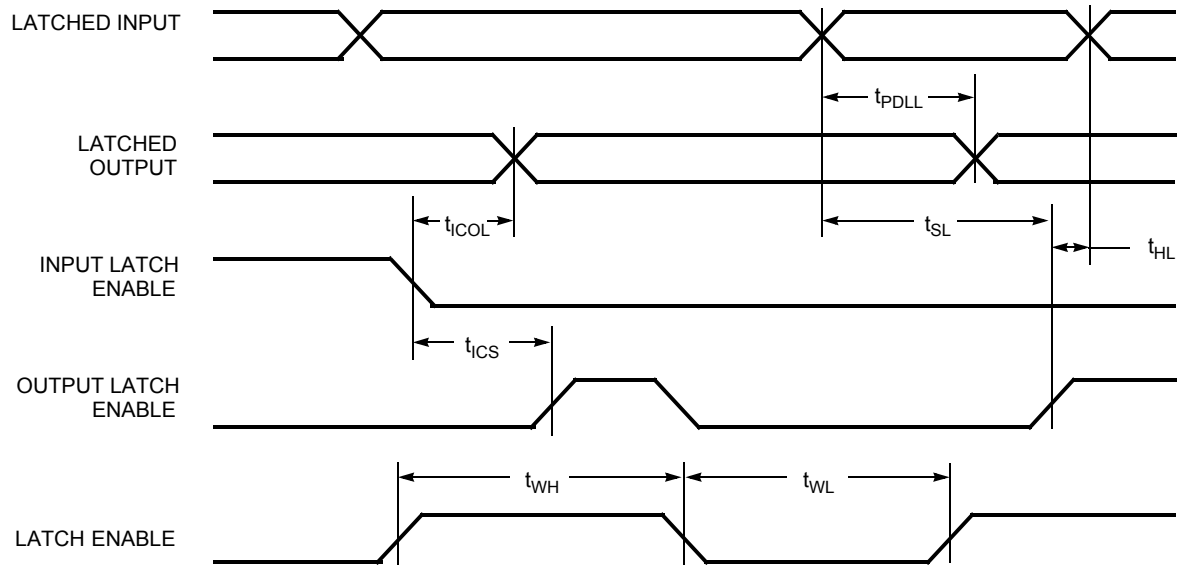
Asynchronous Reset
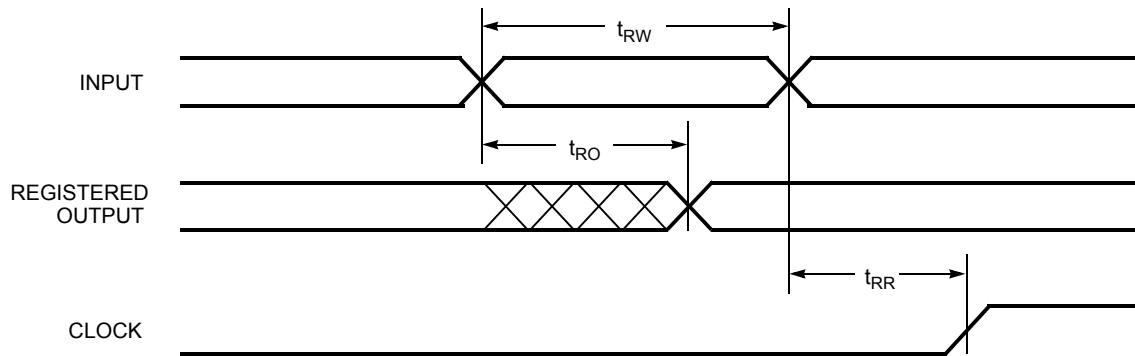
Asynchronous Preset
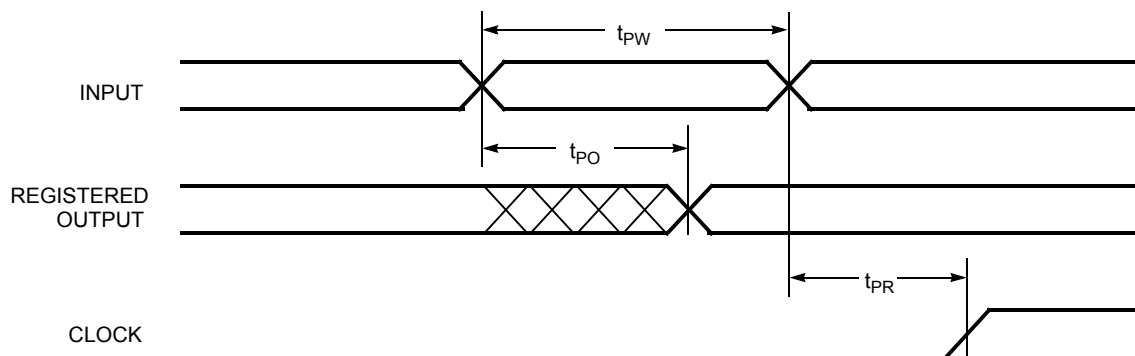
Output Enable/Disable
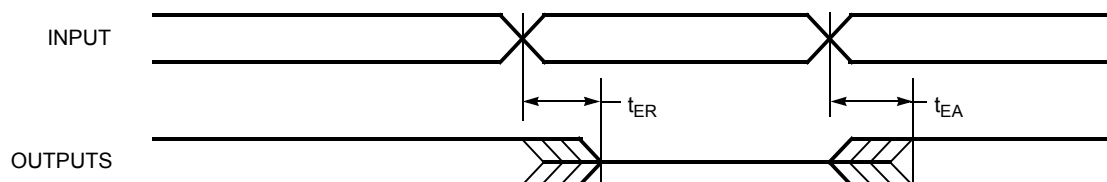
Typical 3.3V Power Consumption (continued)
CY37192V
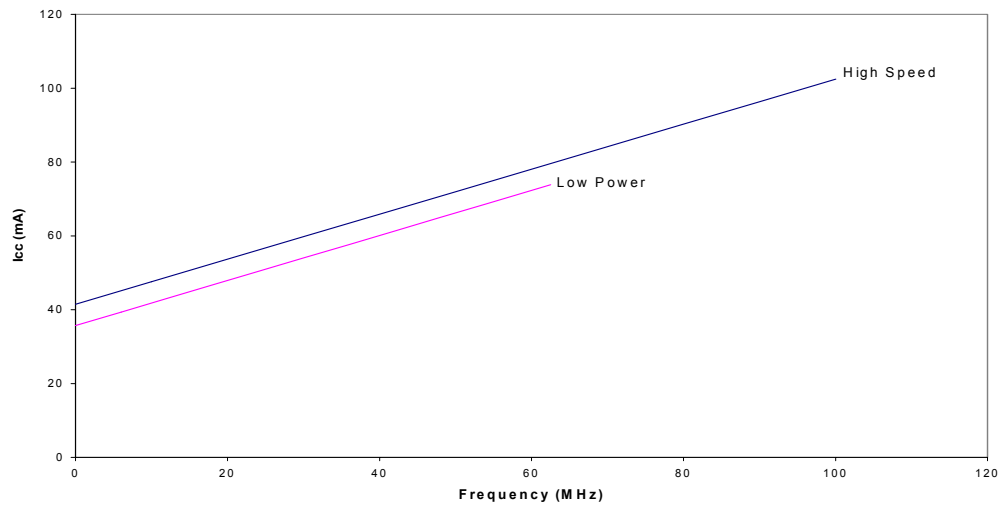
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
$V_{CC} = 3.3V$, T_A = Room Temperature

CY37256V
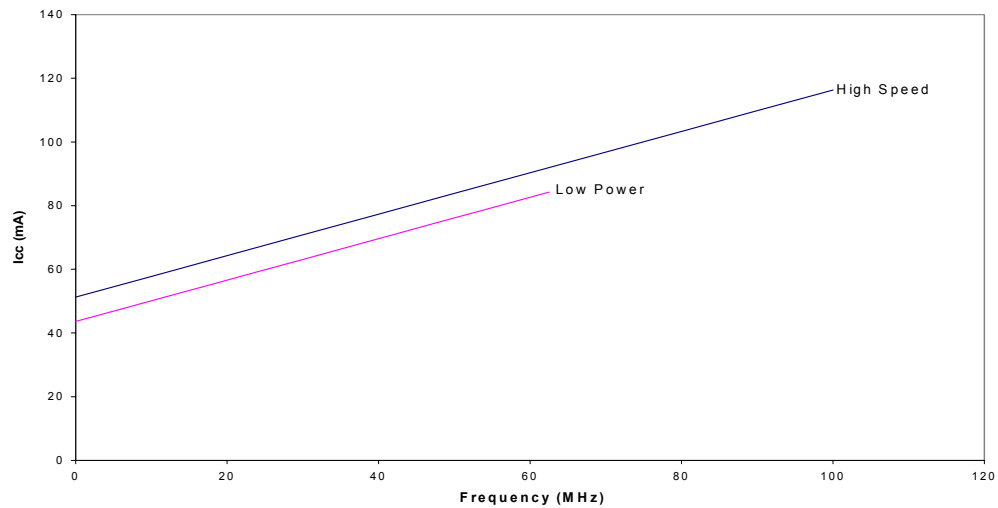
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
$V_{CC} = 3.3V$, T_A = Room Temperature

Pin Configurations[20] (continued)

48-ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O$_5$ TCK	V$_{CC}$	I/O$_3$	I/O$_1$	I/O$_{31}$	I/O$_{30}$	V$_{CC}$	I/O$_{27}$ TDI
B	V$_{CC}$	I/O$_4$	I/O$_2$	I/O$_0$	I/O$_{29}$	I/O$_{28}$	I/O$_{26}$	CLK$_1$/ I$_4$
C	CLK$_2$/ I$_0$	I/O$_7$	I/O$_6$	GND	GND	I/O$_{25}$	I/O$_{24}$	I$_3$
D	JTAG$_{EN}$	I/O$_8$	I/O$_9$	GND	GND	I/O$_{22}$	I/O$_{23}$	CLK$_3$/ I$_2$
E	CLK$_0$/ I$_1$	I/O$_{12}$	I/O$_{11}$	I/O$_{10}$	I/O$_{16}$	I/O$_{20}$	I/O$_{21}$	V$_{CC}$
F	I/O$_{13}$ TMS	V$_{CC}$	I/O$_{14}$	I/O$_{15}$	I/O$_{17}$	I/O$_{18}$	V$_{CC}$	I/O$_{19}$ TDO

Note:
20. For 3.3V versions (Ultra37000V), V$_{CCO}$ = V$_{CC}$.

84-lead PLCC (J83) / CLCC (Y84)
Top View

Top row (pins 11–1, 84–56):
GND (11), I/O$_7$ (10), I/O$_6$ (9), I/O$_5$ (8), I/O$_4$ (7), I/O$_3$ (6), I/O$_2$ (5), I/O$_1$ (4), I/O$_0$ (3), V$_{CCO}$ (2), GND (1), V$_{CC}$ (84), JTAG$_{EN}$ (83), I/O$_{63}$ (82), I/O$_{62}$ (81), I/O$_{61}$ (80), I/O$_{60}$ (79), I/O$_{59}$ (78), I/O$_{58}$ (77), I/O$_{57}$ (76), I/O$_{56}$ (75)

Left side:
I/O$_8$ (12), I/O$_9$ (13), I/O$_{10}$ /TCK (14), I/O$_{11}$ (15), I/O$_{12}$ (16), I/O$_{13}$ (17), I/O$_{14}$ (18), I/O$_{15}$ (19), CLK$_0$/I$_0$ (20), V$_{CCO}$ (21), GND (22), CLK$_1$/I$_1$ (23), I/O$_{16}$ (24), I/O$_{17}$ (25), I/O$_{18}$ (26), I/O$_{19}$ (27), I/O$_{20}$ (28), I/O$_{21}$ (29), I/O$_{22}$ (30), I/O$_{23}$ (31), GND (32)

Right side:
GND (74), I/O$_{55}$ (73), I/O$_{54}$ /TDI (72), I/O$_{53}$ (71), I/O$_{52}$ (70), I/O$_{51}$ (69), I/O$_{50}$ (68), I/O$_{49}$ (67), I/O$_{48}$ (66), CLK$_3$/I$_4$ (65), GND (64), V$_{CCO}$ (63), CLK$_2$/I$_3$ (62), I/O$_{47}$ (61), I/O$_{46}$ (60), I/O$_{45}$ (59), I/O$_{44}$ (58), I/O$_{43}$ (57), I/O$_{42}$ (56), I/O$_{41}$ (55), I/O$_{40}$ (54)

Bottom row (pins 33–53):
I/O$_{24}$ (33), I/O$_{25}$ (34), I/O$_{26}$ /TMS (35), I/O$_{27}$ (36), I/O$_{28}$ (37), I/O$_{29}$ (38), I/O$_{30}$ (39), I/O$_{31}$ (40), I$_2$ (41), V$_{CCO}$ (42), GND (43), V$_{CC}$ [21] (44), I/O$_{32}$ (45), I/O$_{33}$ (46), I/O$_{34}$ (47), I/O$_{35}$ (48), I/O$_{36}$ (49), I/O$_{37}$ (50), I/O$_{38}$ /TDO (51), I/O$_{39}$ (52), GND (53)

Note:
21. This pin is a N/C, but Cypress recommends that you connect it to V$_{CC}$ to ensure future compatibility.

Pin Configurations[20] (continued)

100-ball Fine-Pitch BGA (BB100) for CY37064V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	NC	I/O_7	I/O_5	I/O_2	I/O_{62}	I/O_{60}	I/O_{58}	I/O_{57}	I/O_{56}
B	I/O_9	I/O_8	I/O_6	I/O_4	I/O_1	I/O_{63}	V_{CC}	I/O_{59}	I/O_{55}	NC
C	I/O_{10}	TCK	V_{CC}	I/O_3	NC	NC	I/O_{61}	V_{CC}	TDI	I/O_{54}
D	I/O_{11}	NC	I/O_{12}	I/O_{13}	I/O_0	NC	I/O_{51}	I/O_{52}	CLK_3/I_4	I/O_{53}
E	I/O_{14}	CLK_0/I_0	I/O_{15}	NC	GND	GND	I/O_{48}	I/O_{49}	CLK_2/I_3	I/O_{50}
F	I/O_{17}	NC	NC	I/O_{16}	GND	GND	NC	NC	I_2	I/O_{47}
G	I/O_{22}	CLK_1/I_1	I/O_{21}	I/O_{19}	I/O_{18}	I/O_{46}	I/O_{45}	I/O_{44}	NC	I/O_{43}
H	I/O_{23}	TMS	V_{CC}	I/O_{20}	NC	I/O_{32}	I/O_{42}	V_{CC}	TDO	I/O_{41}
J	NC	I/O_{26}	I/O_{28}	NC	I/O_{31}	I/O_{33}	I/O_{35}	I/O_{37}	I/O_{39}	I/O_{40}
K	I/O_{24}	I/O_{25}	I/O_{27}	I/O_{29}	I/O_{30}	I/O_{34}	I/O_{36}	I/O_{38}	NC	NC

100-ball Fine-Pitch BGA (BB100) for CY37128V
Top View

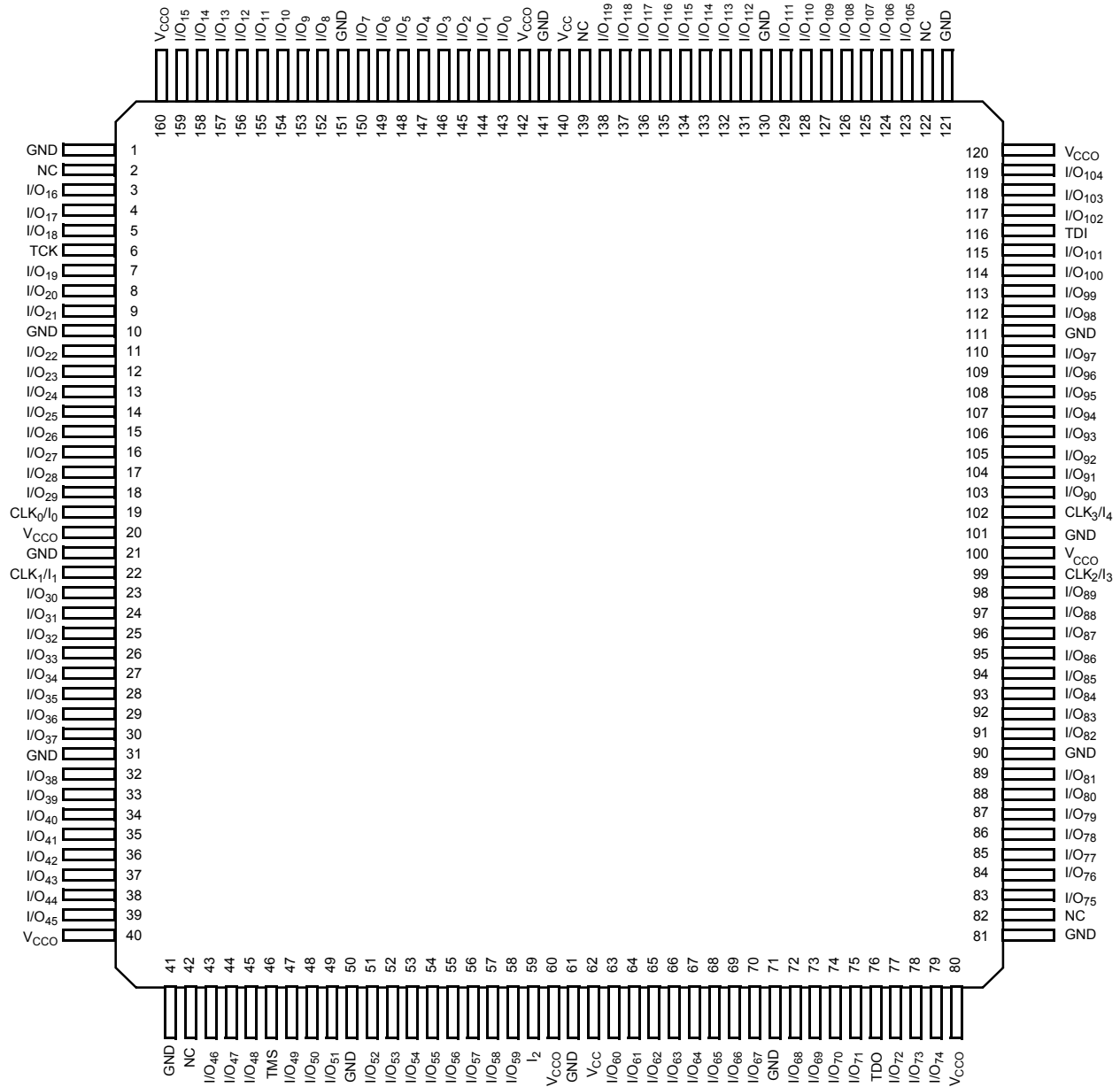|	1	2	3	4	5	6	7	8	9	10
A	NC	I/O_9	I/O_8	I/O_6	I/O_3	I/O_{76}	I/O_{74}	I/O_{72}	I/O_{71}	I/O_{70}
B	I/O_{11}	I/O_{10}	I/O_7	I/O_5	I/O_2	I/O_{77}	V_{CC}	I/O_{73}	I/O_{68}	I/O_{69}
C	I/O_{12}	I/O_{13} TCK	V_{CC}	I/O_4	I/O_1	I/O_{78}	I/O_{75}	V_{CC}	I/O_{67} TDI	I/O_{66}
D	I/O_{14}	NC	I/O_{15}	I/O_{16}	I/O_0	I/O_{79}	I/O_{63}	I/O_{64}	CLK_3/I_4	I/O_{65}
E	I/O_{17}	CLK_0/I_0	I/O_{18}	I/O_{19}	GND	GND	I/O_{60}	I/O_{61}	CLK_2/I_3	I/O_{62}
F	I/O_{22}	JTAG EN	I/O_{21}	I/O_{20}	GND	GND	I/O_{59}	I/O_{58}	I_2	I/O_{57}
G	I/O_{27}	CLK_1/I_1	I/O_{26}	I/O_{24}	I/O_{23}	I/O_{56}	I/O_{55}	I/O_{54}	NC	I/O_{53}
H	I/O_{28}	I/O_{33} TMS	V_{CC}	I/O_{25}	I/O_{39}	I/O_{40}	I/O_{52}	V_{CC}	I/O_{47} TDO	I/O_{51}
J	I/O_{29}	I/O_{32}	I/O_{35}	V_{CC}	I/O_{38}	I/O_{41}	I/O_{43}	I/O_{45}	I/O_{48}	I/O_{50}
K	I/O_{30}	I/O_{31}	I/O_{34}	I/O_{36}	I/O_{37}	I/O_{42}	I/O_{44}	I/O_{46}	I/O_{49}	NC

LEAD-FREE

Pin Configurations[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View

Top pins (left to right, 160–121):
V_{CCO}, I/O15, I/O14, I/O13, I/O12, I/O11, I/O10, I/O9, I/O8, GND, I/O7, I/O6, I/O5, I/O4, I/O3, I/O2, I/O1, I/O0, V_{CCO}, GND, V_{CC}, NC, I/O119, I/O118, I/O117, I/O116, I/O115, I/O114, I/O113, I/O112, GND, I/O111, I/O110, I/O109, I/O108, I/O107, I/O106, I/O105, NC, GND

Left side (pins 1–40):
Pin	Signal
1	GND
2	NC
3	I/O16
4	I/O17
5	I/O18
6	TCK
7	I/O19
8	I/O20
9	I/O21
10	GND
11	I/O22
12	I/O23
13	I/O24
14	I/O25
15	I/O26
16	I/O27
17	I/O28
18	I/O29
19	CLK0/I0
20	V_{CCO}
21	GND
22	CLK1/I1
23	I/O30
24	I/O31
25	I/O32
26	I/O33
27	I/O34
28	I/O35
29	I/O36
30	I/O37
31	GND
32	I/O38
33	I/O39
34	I/O40
35	I/O41
36	I/O42
37	I/O43
38	I/O44
39	I/O45
40	V_{CCO}

Right side (pins 120–81):
Pin	Signal
120	V_{CCO}
119	I/O104
118	I/O103
117	I/O102
116	TDI
115	I/O101
114	I/O100
113	I/O99
112	I/O98
111	GND
110	I/O97
109	I/O96
108	I/O95
107	I/O94
106	I/O93
105	I/O92
104	I/O91
103	I/O90
102	CLK3/I4
101	GND
100	V_{CCO}
99	CLK2/I3
98	I/O89
97	I/O88
96	I/O87
95	I/O86
94	I/O85
93	I/O84
92	I/O83
91	I/O82
90	GND
89	I/O81
88	I/O80
87	I/O79
86	I/O78
85	I/O77
84	I/O76
83	I/O75
82	NC
81	GND

Bottom pins (left to right, 41–80):
GND, NC, I/O46, I/O47, I/O48, TMS, I/O49, I/O50, I/O51, GND, I/O52, I/O53, I/O54, I/O55, I/O56, I/O57, I/O58, I/O59, I2, V_{CCO}, GND, V_{CC}, I/O60, I/O61, I/O62, I/O63, I/O64, I/O65, I/O66, I/O67, GND, I/O68, I/O69, I/O70, I/O71, TDO, I/O72, I/O73, I/O74, V_{CCO}

Pin Configurations[20] (continued)

292-Ball PBGA (BG292)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O_{21}	NC	I/O_{16}	I/O_{12}	I/O_9	I/O_7	I/O_4	I/O_0	I/O_{190}	I/O_{189}	I/O_{186}	I/O_{182}	NC	I/O_{178}	I/O_{175}	NC	NC	I/O_{169}	I/O_{168}	A
B	I/O_{23}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{15}	I/O_{11}	I/O_8	I/O_5	I/O_1	I/O_{191}	I/O_{187}	I/O_{185}	I/O_{181}	NC	NC	I/O_{174}	I/O_{171}	I/O_{170}	NC	I/O_{166}	B
C	NC	NC	I/O_{22}	NC	I/O_{17}	I/O_{14}	I/O_{10}	I/O_6	I/O_2	NC	I/O_{188}	I/O_{184}	I/O_{180}	I/O_{179}	I/O_{176}	I/O_{173}	I/O_{172}	I/O_{167}	I/O_{165}	I/O_{162}	C
D	I/O_{24}	NC	NC	GND	NC	V_{CCO}	I/O_{13}	GND	I/O_3	NC	V_{CC}	I/O_{183}	GND	I/O_{177}	V_{CCO}	NC	GND	I/O_{164}	TDI	I/O_{160}	D
E	I/O_{27}	I/O_{26}	I/O_{25}	NC													I/O_{163}	I/O_{161}	I/O_{159}	I/O_{156}	E
F	I/O_{30}	TCK	I/O_{28}	V_{CCO}													V_{CCO}	I/O_{158}	NC	I/O_{154}	F
G	I/O_{33}	I/O_{32}	I/O_{31}	I/O_{29}													I/O_{157}	I/O_{155}	I/O_{153}	I/O_{152}	G
H	I/O_{35}	NC	I/O_{34}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{151}	I/O_{150}	I/O_{149}	H
J	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{36}				GND	GND	GND	GND	GND	GND				I/O_{148}	I/O_{147}	I/O_{146}	I/O_{145}	J
K	I/O_{42}	I/O_{40}	I/O_{41}	V_{CC}				GND	GND	GND	GND	GND	GND				I/O_{144}	CLK_3/I_4	NC	NC	K
L	I/O_{43}	I/O_{44}	I/O_{45}	I/O_{46}				GND	GND	GND	GND	GND	GND				V_{CC}	CLK_2/I_3	I/O_{143}	NC	L
M	I/O_{47}	CLK_0/I_0	CLK_1/I_1	I/O_{48}				GND	GND	GND	GND	GND	GND				I/O_{139}	I/O_{140}	I/O_{141}	I/O_{142}	M
N	I/O_{49}	I/O_{50}	I/O_{51}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{136}	I/O_{137}	I/O_{138}	N
P	I/O_{52}	I/O_{53}	I/O_{55}	I/O_{58}													I/O_{131}	I/O_{133}	I/O_{134}	I/O_{135}	P
R	I/O_{54}	I/O_{56}	I/O_{59}	V_{CCO}													V_{CCO}	I/O_{130}	NC	I/O_{132}	R
T	I/O_{57}	I/O_{60}	I/O_{62}	I/O_{65}													I/O_{124}	I/O_{127}	I/O_{128}	I/O_{129}	T
U	I/O_{61}	I/O_{63}	I/O_{66}	GND	I/O_{76}	V_{CCO}	I/O_{82}	GND	I/O_{91}	V_{CC}	I/O_{98}	I/O_{102}	GND	I/O_{112}	V_{CCO}	NC	GND	I/O_{123}	I/O_{122}	I/O_{126}	U
V	I/O_{64}	I/O_{67}	I/O_{69}	I/O_{75}	I/O_{78}	I/O_{81}	I/O_{85}	I/O_{88}	I/O_{92}	I_2	I/O_{97}	I/O_{101}	I/O_{105}	I/O_{109}	I/O_{113}	TDO	I/O_{114}	I/O_{117}	I/O_{121}	I/O_{125}	V
W	I/O_{68}	I/O_{70}	I/O_{72}	I/O_{74}	I/O_{79}	I/O_{83}	I/O_{86}	I/O_{89}	I/O_{93}	I/O_{95}	I/O_{96}	I/O_{100}	I/O_{104}	I/O_{107}	I/O_{110}	NC	NC	I/O_{115}	I/O_{118}	I/O_{120}	W
Y	I/O_{71}	I/O_{73}	I/O_{77}	TMS	I/O_{80}	I/O_{84}	I/O_{87}	I/O_{90}	I/O_{94}	NC	NC	I/O_{99}	I/O_{103}	I/O_{106}	I/O_{108}	I/O_{111}	NC	NC	I/O_{116}	I/O_{119}	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Ordering Information

CY 37 512 V P400 - 83 BB X C

Cypress Semiconductor ID

Family Type
37 = Ultra37000 Family

Macrocell Density
 32 = 32 Macrocells 256 = 256 Macrocells
 64 = 64 Macrocells 384 = 384 Macrocells
128 = 128 Macrocells   512 = 512
Macrocells
192 = 192 Macrocells

Operating Reference Voltage
V = 3.3V Supply Voltage
(5.0V if not specified)

Pin Count
P44 = 44 Leads
P48 = 48 Leads
P84 = 84 Leads
P100 = 100 Leads
P160 = 160 Leads
P208 = 208 Leads
P256 = 256 Leads
P352 = 352 Leads
P400 = 400 Leads

Operating Conditions
Commercial   0°C to +70°C
Industrial -40°C to +85°C
Military   -55°C to +125°C

Lead Free
X   Lead Free

Package Type
A = Thin Quad Flat Pack (TQFP)
U = Ceramic Quad Flat Pack (CQFP)
N = Plastic Quad Flat Pack (PQFP)
NT = Thermally Enhanced Plastic Quad Flat Pack
     (EQFP)
J = Plastic Leaded Chip Carrier (PLCC)
Y = Ceramic Leaded Chip Carrier (CLCC)
BG = Plastic Ball Grid Array (PBGA)
BA = Fine-Pitch Ball Grid Array (FBGA)
     0.8mm Lead Pitch
BB = Fine-Pitch Ball Grid Array (FBGA)
     1.0mm Lead Pitch

Speed
                        125 = 125 MHz
200 = 200 MHz   100 = 100 MHz
167 = 167 MHz   83 = 83 MHz
154 = 154 MHz   66 = 66 MHz
143 = 143 MHz

5.0V Ordering Information

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	200	CY37032P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-200AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-200JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
	154	CY37032P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
	125	CY37032P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37032P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
64	200	CY37064P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-200AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-200JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-200JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-200AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-200AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-125BGC	BG388	388-Ball Plastic Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

3.3V Ordering Information

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-143BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAI	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP44-100JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	

3.3V Ordering Information (continued)

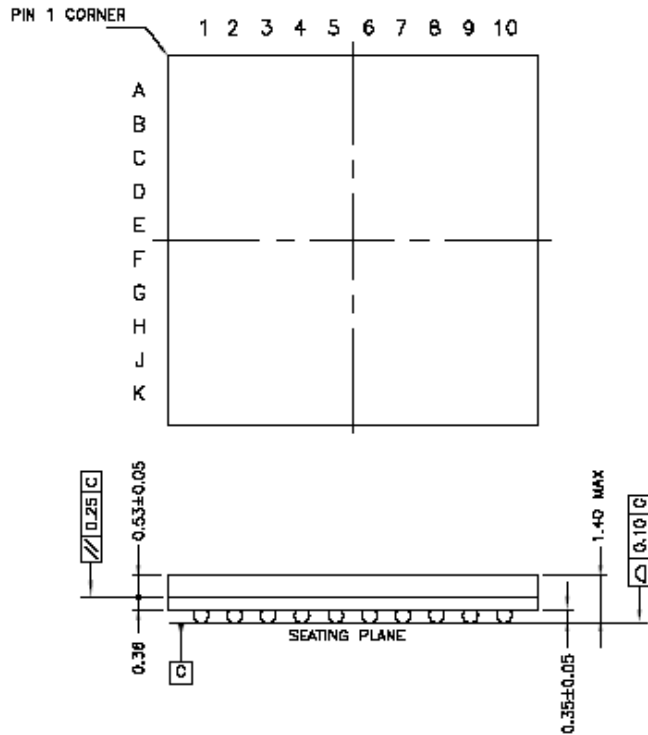| Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	143	CY37064VP44-143AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-143BAC	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-143AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-143AXC	A100	100-Lead Lead Free Thin Quad Flatpack	
		CY37064VP100-143BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
	100	CY37064VP44-100AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-100BAC	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100AXC	A100	100-Lead Lead Free Thin Quad Flatpack	
		CY37064VP100-100BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37064VP44-100AI	A44	44-Lead Thin Quad Flatpack	Industrial
		CY37064VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-100BAI	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100BBI	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100AI	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100AXI	A100	100-Lead Lead Free Thin Quad Flatpack	
		5962-9952001QYA	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
128	125	CY37128VP100-125AC	A100	100-Lead Thin Quad Flat Pack	Commercial
		CY37128VP100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-125BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37128VP160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	83	CY37128VP100-83AC	A100	100-Lead Thin Quad Flat Pack	Commercial
		CY37128VP100-83AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-83AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83AI	A100	100-Lead Thin Quad Flat Pack	Industrial
		CY37128VP100-83AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83BBI	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-83AI	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		5962-9952201QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	100	CY37192VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37192VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial

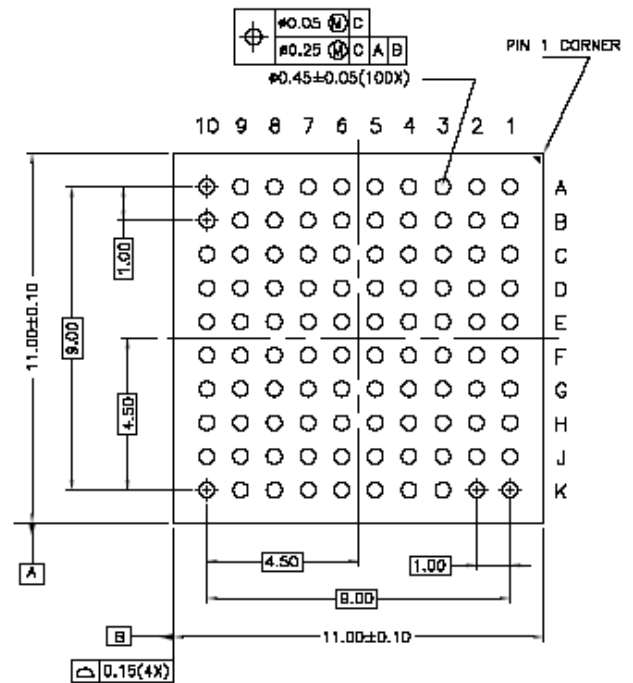## Package Diagrams (continued)

44-Lead Ceramic Leaded Chip Carrier Y67

PIN 1

.685
.695

.642
.656

.642
.656

.685
.695

SEE VIEW A

.590
.630

.090
.120

.155
.190

SEATING PLANE

.500
REF.

.050
BSC

.040 X 45°

.006
.010

.035 X 45°

.030
MIN.

.035
.045 R.

.017
.023

.026
.032

VIEW A

51-80014-**
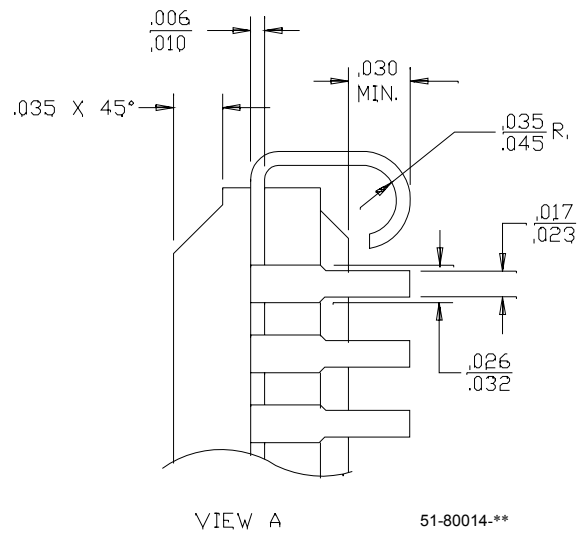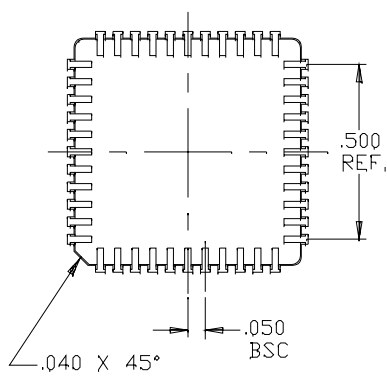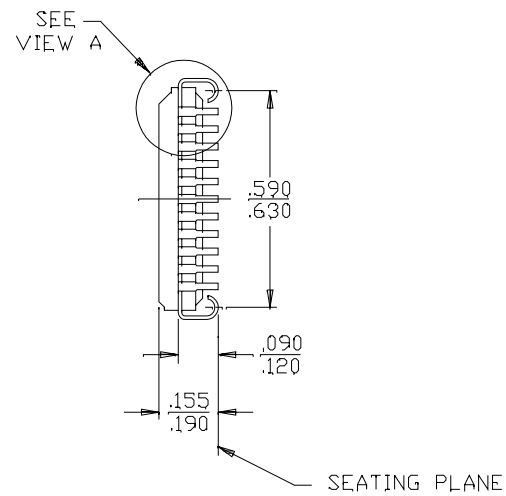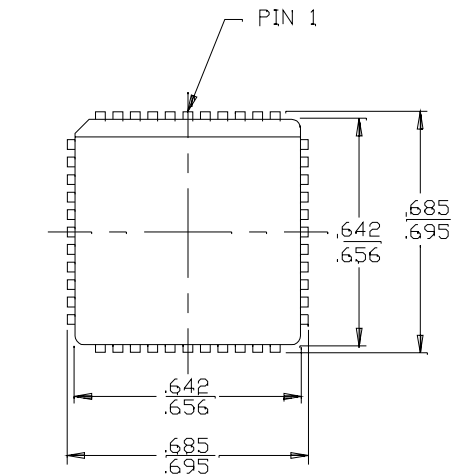
Package Diagrams (continued)

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100
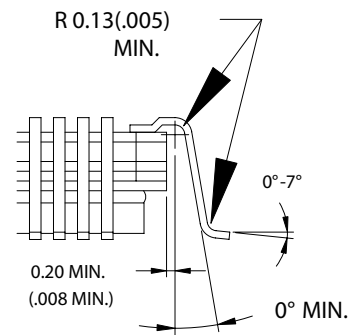

51-85107-*B

Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208
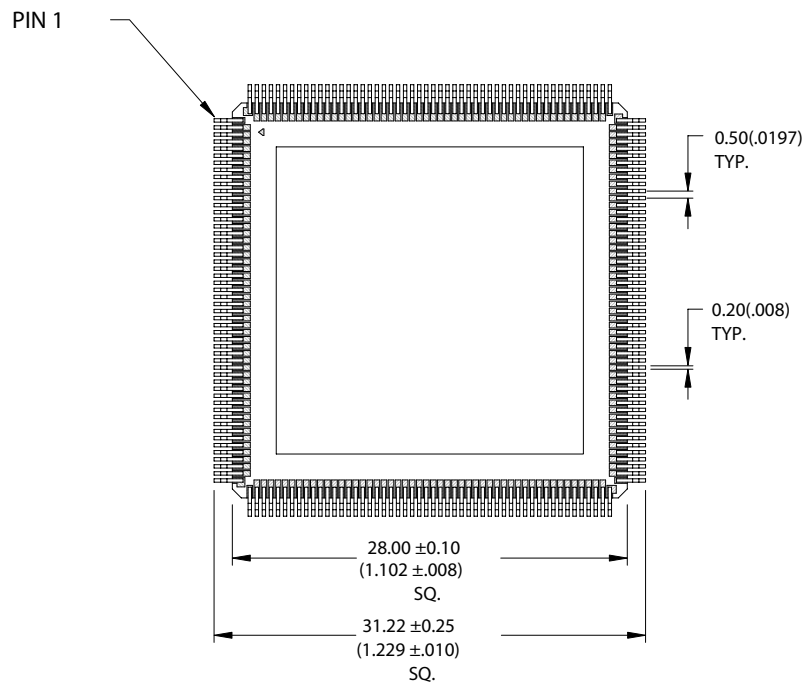
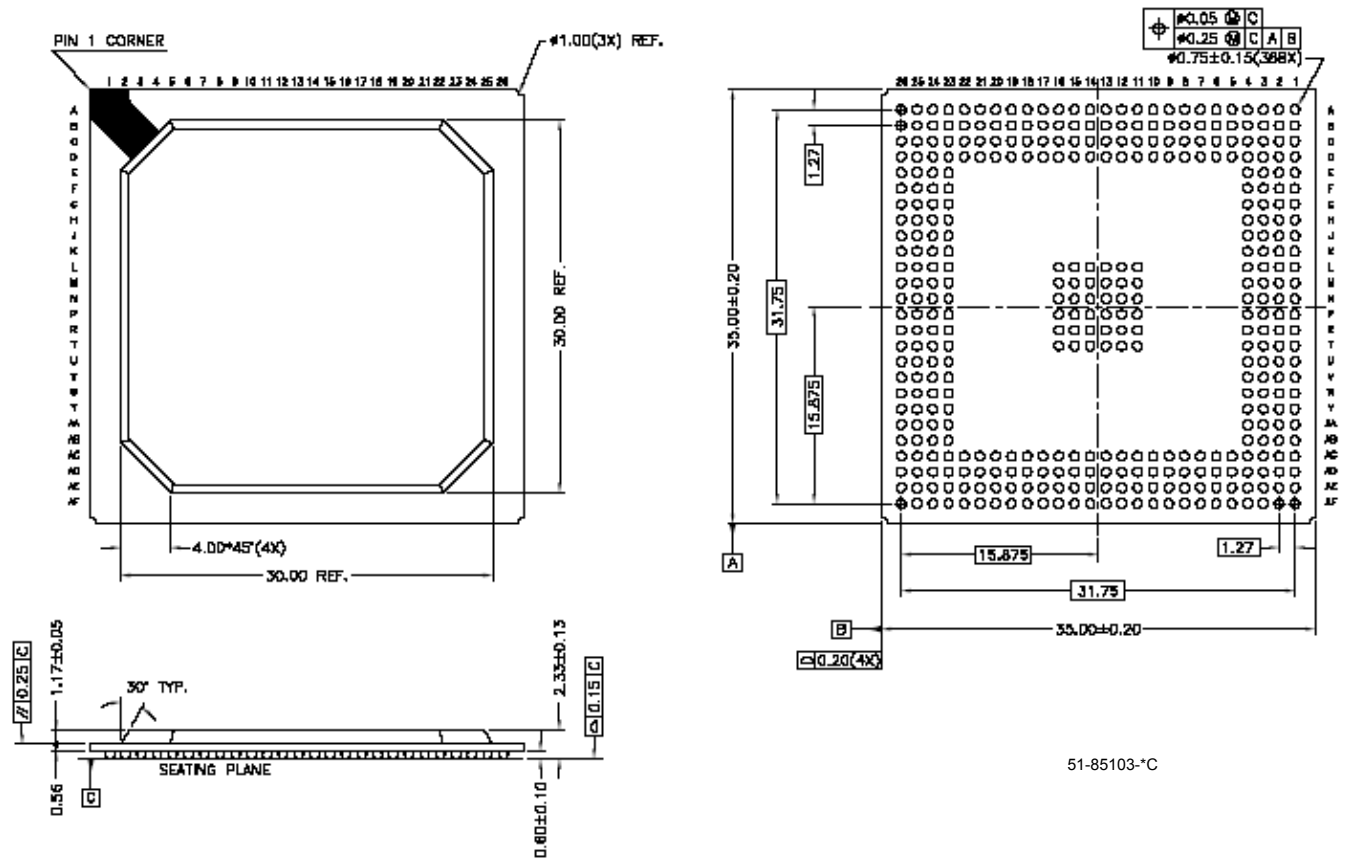DIMENSIONS IN MM (INCH)

REFERENCE JEDEC: N/A

PKG. WEIGHT: 6-7gms

PIN 1

0.50(.0197)
TYP.

0.20(.008)
TYP.

28.00 ±0.10
(1.102 ±.008)
SQ.

31.22 ±0.25
(1.229 ±.010)
SQ.

R 0.13(.005)
MIN.

0°-7°

0.20 MIN.
(.008 MIN.)

0° MIN.

DETAIL A

SEE DETAIL A

3.43(.135)
3.94(.155)

SEATING PLANE

0.15 ±0.02
(.006 ±.001)

0.050(.002)
0.500(.020)

0.51 ±0.20
(.020 ±.008)
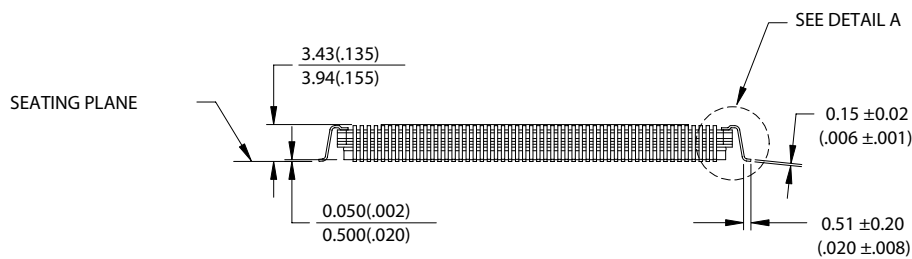
51-80105-*B

Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388

51-85103-*C

Package Diagrams (continued)

400-Ball FBGA (21 x 21 x 1.4 mm) BB400

TOP VIEW

BOTTOM VIEW

SIDE VIEW

51-85111-*A
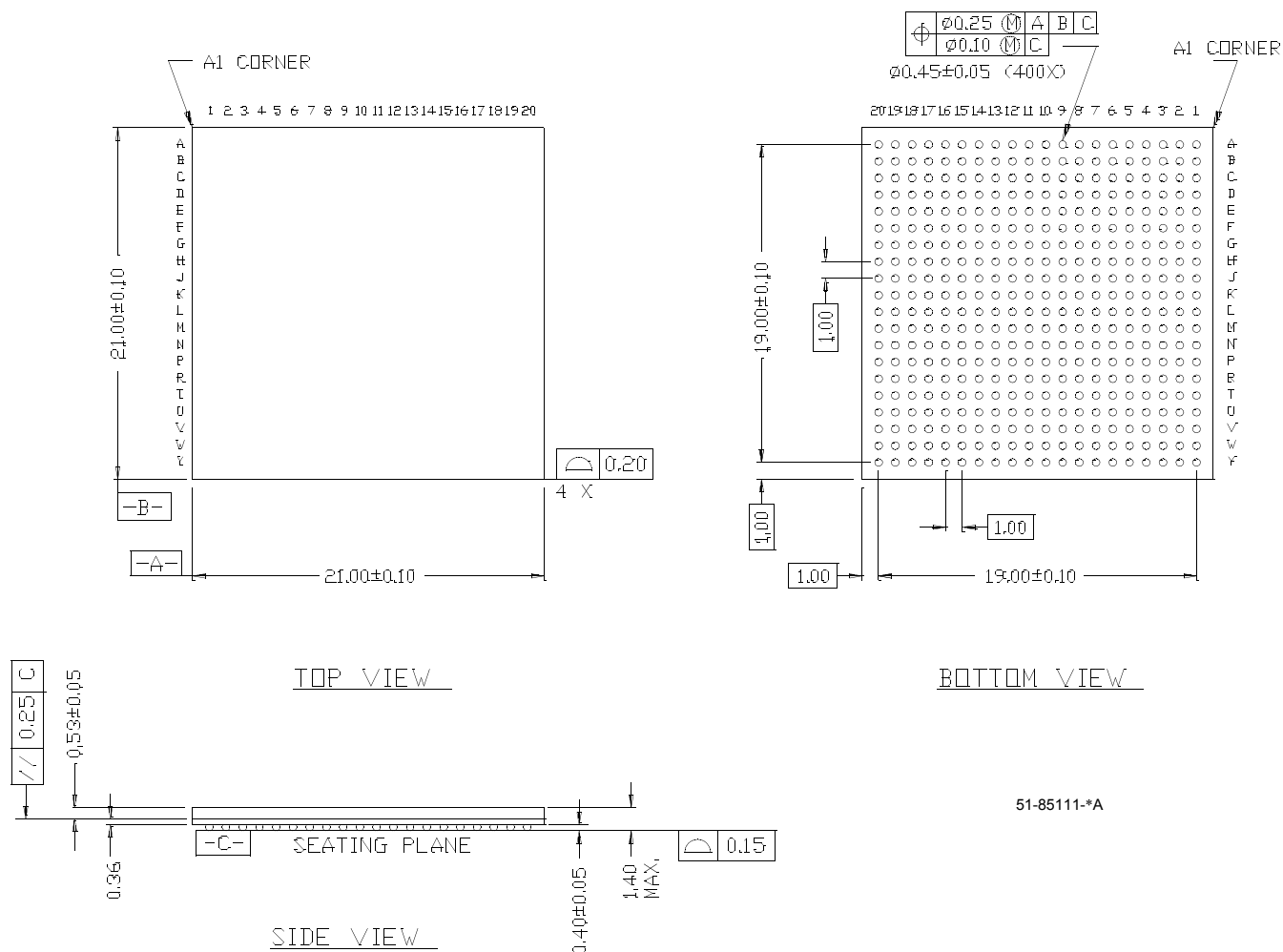
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Addendum

3.3V Operating Range

(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.16V

Document History Page

Document Title: Ultra37000 CPLD Family 5V, 3.3V, ISR™ High-Performance CPLDs
Document Number: 38-03007

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106272	04/18/01	SZV	Change from Spec number: 38-00475 to 38-03007
*A	124942	03/21/03	OOR	Updated 3.3V V_{CC} requirements for –144 speeds Added an Addendum
*B	126262	05/09/03	TEH	Changed pinout for CY37128V BB100 package
*C	128125	07/16/03	HOM	Obsoleted following 3.3V PLCC packaged devices: CY37032VP44-143JC CY37032VP44-100JC CY37032VP44-100JI CY37064VP44-143JC CY37064VP84-143JC CY37064VP44-100JC CY37064VP84-100JC CY37064VP44-100JI CY37064VP84-100JI CY37128VP84-125JC CY37128VP84-83JC CY37128VP84-83JI
*D	282709	See ECN	YDT	Changed package diagrams and labels for consistency Added Lead (Pb)-free logo on first page, as well as a note in Features Added Lead (Pb)-free package diagram labels Added Lead-free Parts to Ordering Information CY37032P44-200AXC, CY37032P44-200JXC, CY37032P44-154AXI, CY37032P44-154JXI, CY37032P44-125AXC, CY37032P44-125JXC, CY37064P44-200AXC, CY37064P44-200JXC, CY37064P100-200AXC, CY37064P44-154AXI, CY37064P44-154JXI, CY37064P44-125AXC, CY37064P44-125JXC, CY37064P100-125AXC, CY37064P44-125AXI, CY37064P100-125AXI, CY37128P84-167JXC, CY37128P100-167AXC, CY37128P160-167AXC, CY37128P84-125JXC, CY37128P100-125AXC, CY37128P160-125AXC, CY37128P84-125JXI, CY37128P100-125AXI, CY37128P160-125AXI, CY37128P84-100JXC, CY37128P100-100AXC, CY37128P160-100AXC, CY37128P100-100AXI, CY37192P160-154AXC, CY37192P160-125AXC, CY37192P160-125AXI, CY37192P160-83AXC, CY37192P160-83AXI, CY37256P160-154AXC, CY37256P160-125AXC, CY37256P160-125AXI, CY37256P160-83AXC, CY37256P160-83AXI, CY37032VP44-143AXC, CY37032VP44-100AXC, CY37032VP44-100AXI, CY37032VP44-100JXI, CY37064VP44-143AXC, CY37064VP100-143AXC, CY37064VP44-100AXC, CY37064VP100-100AXC, CY37064VP44-100AXI, CY37064VP100-100AXI, CY37128VP100-125AXC, CY37128VP160-125AXC, CY37128VP160-125AXI, CY37128VP100-83AXC, CY37128VP160-83AXC, CY37128VP100-83AXI, CY37128VP160-83AXI, CY37192VP160-100AXC, CY37192VP160-66AXC, CY37256VP160-100AXC, CY37256VP160-100AXI, CY37256VP160-66AXC
*E	321635	See ECN	PCX	Added Package Diagram BG292 Updated all PBGA package type information (BG292 & BG388)