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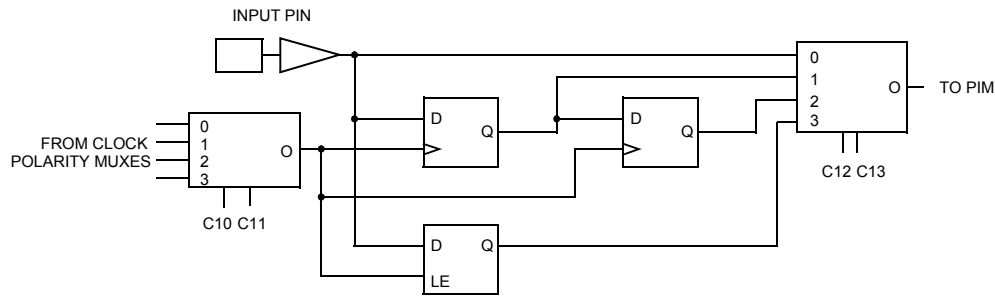
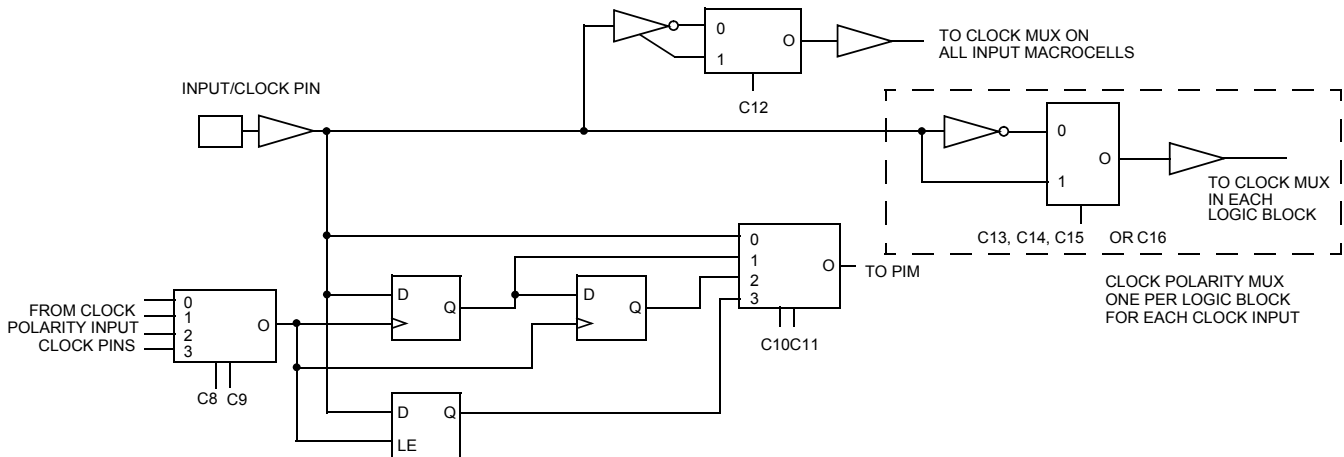
Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	6 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	69
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37064p100-200axct


Figure 3. Input Macrocell

Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

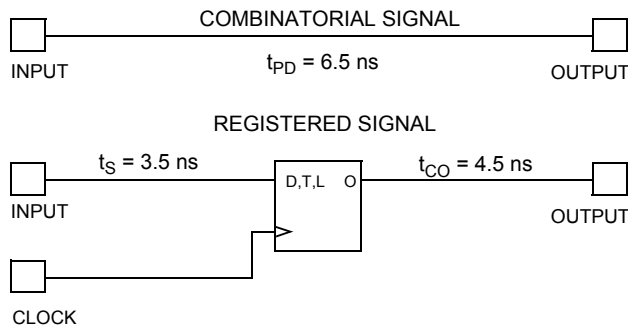


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in Figure 6.

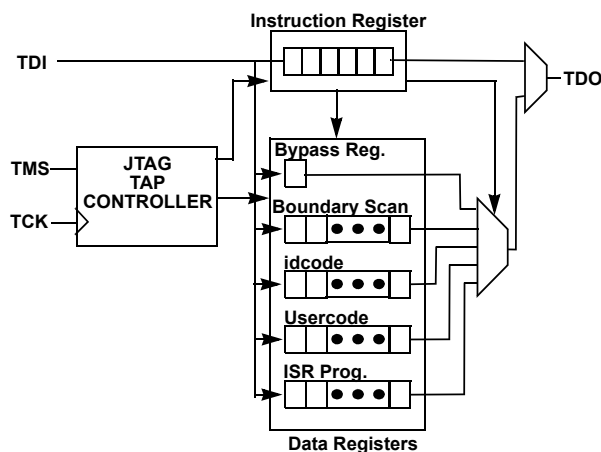


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing

resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the Warp for PC, Warp for UNIX, Warp Professional and Warp Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although Warp is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

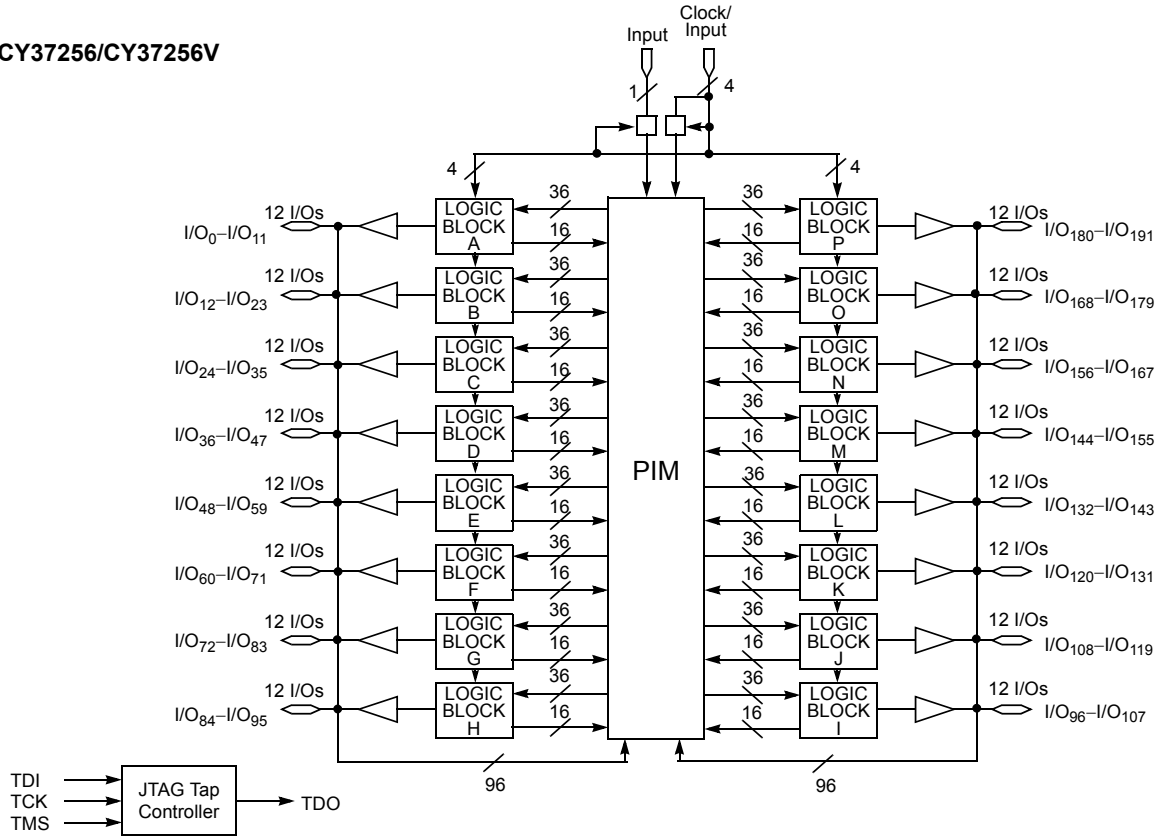
Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

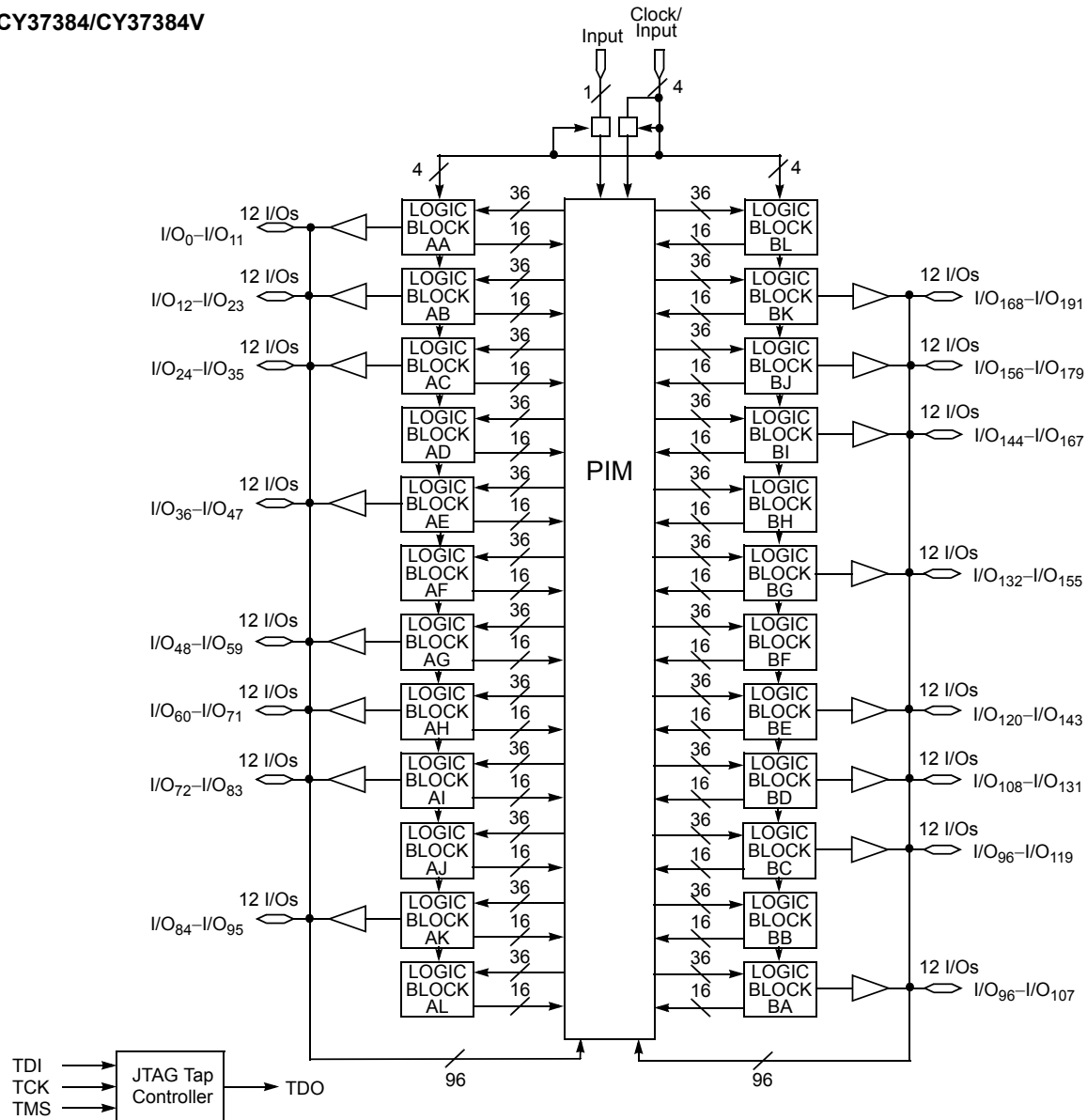
Logic Block Diagrams (continued)

CY37256/CY37256V



Logic Block Diagrams (continued)

CY37384/CY37384V



Inductance^[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$	2	5	2	8	5	8	9	11	nH

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	10	pF
C_{CLK}	Clock Signal Capacitance	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	12	pF
C_{DP}	Dual-Function Pins ^[9]	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	16	pF

Endurance Characteristics^[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions ^[2]	1,000	10,000	Cycles

3.3V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature $-65^\circ C$ to $+150^\circ C$

Ambient Temperature with

Power Applied $-55^\circ C$ to $+125^\circ C$

Supply Voltage to Ground Potential $-0.5V$ to $+4.6V$

DC Voltage Applied to Outputs

in High-Z State $-0.5V$ to $+7.0V$

DC Input Voltage $-0.5V$ to $+7.0V$

DC Program Voltage 3.0 to $3.6V$

Current into Outputs 8 mA

Static Discharge Voltage $> 2001V$
(per MIL-STD-883, Method 3015)

Latch-up Current $> 200\text{ mA}$

Operating Range^[2]

Range	Ambient Temperature ^[2]	Junction Temperature	V_{CC} ^[10]
Commercial	$0^\circ C$ to $+70^\circ C$	$0^\circ C$ to $+90^\circ C$	$3.3V \pm 0.3V$
Industrial	$-40^\circ C$ to $+85^\circ C$	$-40^\circ C$ to $+105^\circ C$	$3.3V \pm 0.3V$
Military ^[3]	$-55^\circ C$ to $+125^\circ C$	$-55^\circ C$ to $+130^\circ C$	$3.3V \pm 0.3V$

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -4\text{ mA (Com'I)}^{[4]}$ $I_{OH} = -3\text{ mA (Mil)}^{[4]}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $I_{OL} = 8\text{ mA (Com'I)}^{[4]}$ $I_{OL} = 6\text{ mA (Mil)}^{[4]}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs ^[7]	2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs ^[7]	-0.5	0.8	V
I_{IX}	Input Load Current	$V_I = \text{GND OR } V_{CC}$, Bus-Hold Disabled	-10	10	μA
I_{OZ}	Output Leakage Current	$V_O = \text{GND or } V_{CC}$, Output Disabled, Bus-Hold Disabled	-50	50	μA
I_{OS}	Output Short Circuit Current ^[5, 8]	$V_{CC} = \text{Max.}$, $V_{OUT} = 0.5V$	-30	-160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	$V_{CC} = \text{Min.}$, $V_{IL} = 0.8V$	+75		μA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	$V_{CC} = \text{Min.}$, $V_{IH} = 2.0V$	-75		μA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	$V_{CC} = \text{Max.}$		+500	μA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	$V_{CC} = \text{Max.}$		-500	μA

Notes:

9. Dual pins are I/O with JTAG pins.

10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is $3.3V \pm 0.16V$.

Inductance^[5]

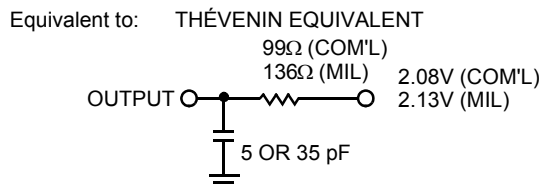
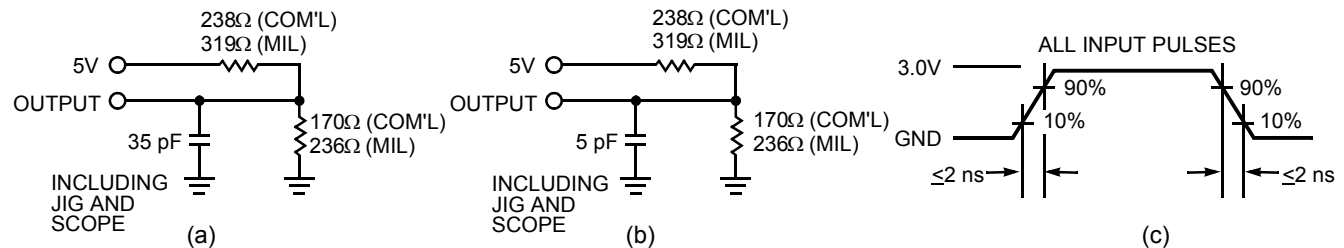
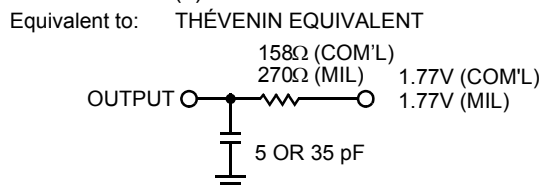
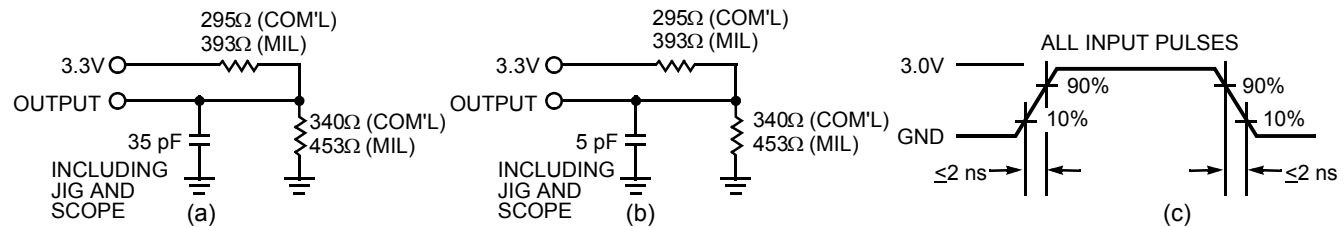
Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	$V_{IN} = 3.3V$ at $f = 1\text{ MHz}$	2	5	2	8	5	8	9	11	nH

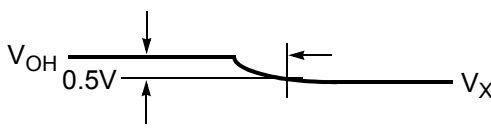
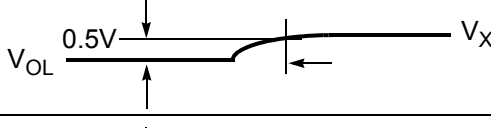
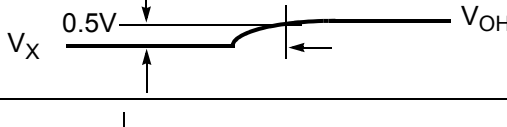
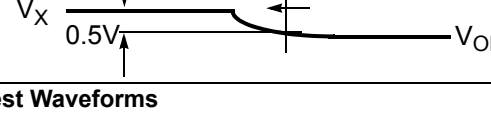
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{IN} = 3.3V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	8	pF
C_{CLK}	Clock Signal Capacitance	$V_{IN} = 3.3V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	12	pF
C_{DP}	Dual Functional Pins ^[9]	$V_{IN} = 3.3V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	16	pF

Endurance Characteristics^[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions ^[2]	1,000	10,000	Cycles

AC Characteristics
5.0V AC Test Loads and Waveforms

3.3V AC Test Loads and Waveforms


Parameter ^[11]	V _X	Output Waveform—Measurement Level
t _{ER} (-)	1.5V	
t _{ER} (+)	2.6V	
t _{EA} (+)	1.5V	
t _{EA} (-)	V _{the}	

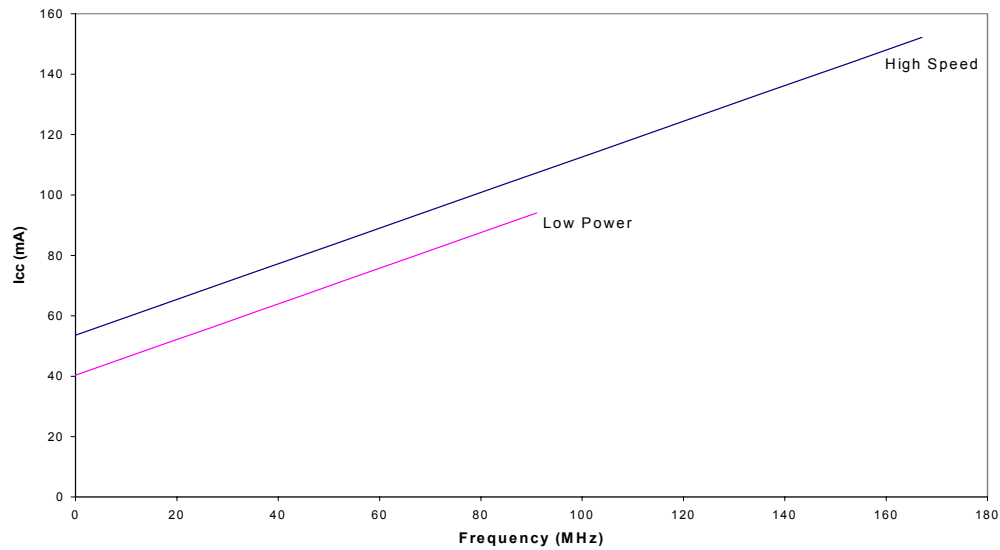
(d) Test Waveforms

Switching Characteristics Over the Operating Range ^[12]

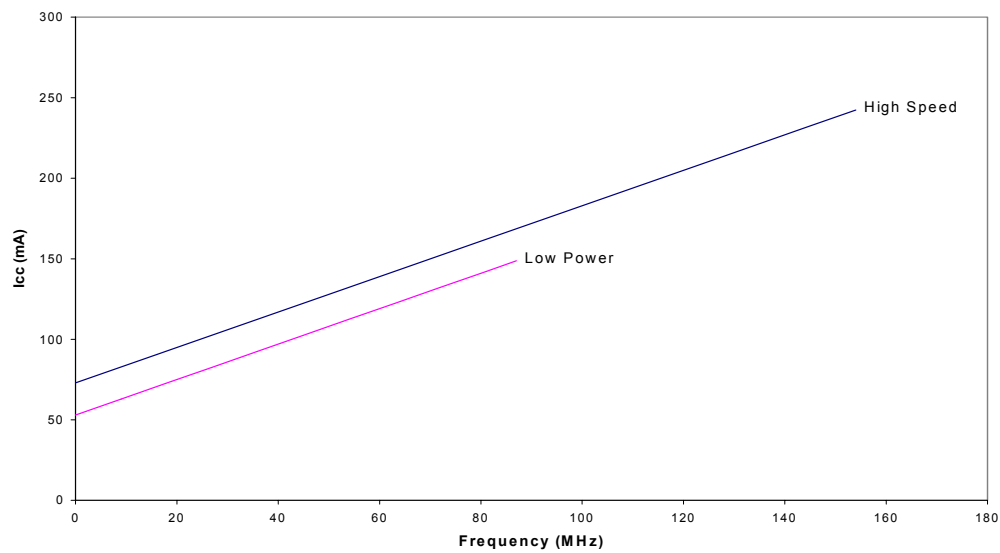
Parameter	Description	Unit
Combinatorial Mode Parameters		
t _{PD} ^[13, 14, 15]	Input to Combinatorial Output	ns
t _{PDL} ^[13, 14, 15]	Input to Output Through Transparent Input or Output Latch	ns
t _{PDLL} ^[13, 14, 15]	Input to Output Through Transparent Input and Output Latches	ns
t _{EA} ^[13, 14, 15]	Input to Output Enable	ns
t _{ER} ^[11, 13]	Input to Output Disable	ns
Input Register Parameters		
t _{WL}	Clock or Latch Enable Input LOW Time ^[8]	ns
t _{WH}	Clock or Latch Enable Input HIGH Time ^[8]	ns
t _{IS}	Input Register or Latch Set-up Time	ns
t _{IH}	Input Register or Latch Hold Time	ns
t _{CO} ^[13, 14, 15]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t _{COL} ^[13, 14, 15]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t _{CO} ^[14, 15]	Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output	ns
t _S ^[13]	Set-Up Time from Input to Sync. Clk (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	ns
t _H	Register or Latch Data Hold Time	ns
t _{CO2} ^[13, 14, 15]	Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t _{SCS} ^[13]	Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable (Through Logic Array)	ns
t _{SL} ^[13]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	ns

Notes:

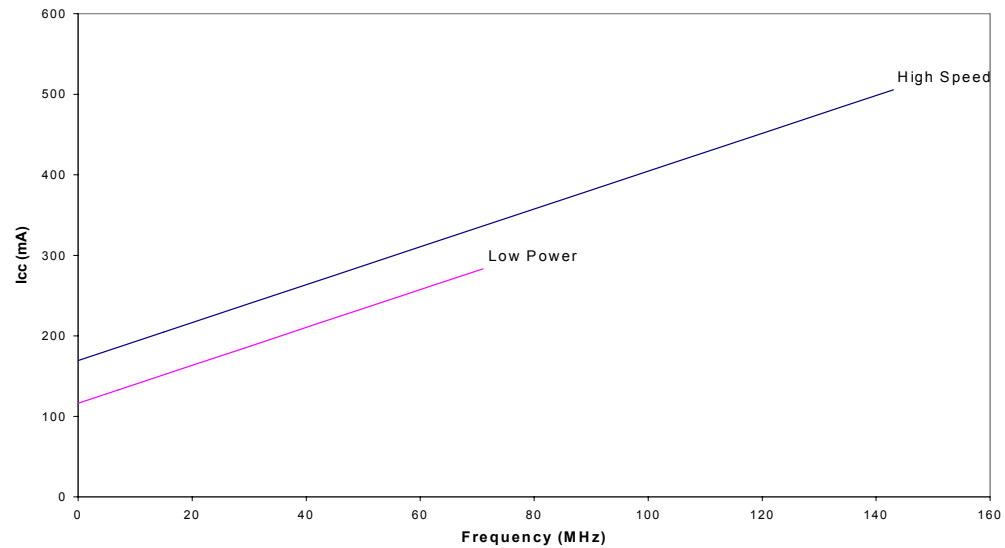
11. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
12. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
13. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
14. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
15. When V_{CCO} = 3.3V, add t_{3.3IO} to this spec.

Typical 5.0V Power Consumption (continued)
CY37128


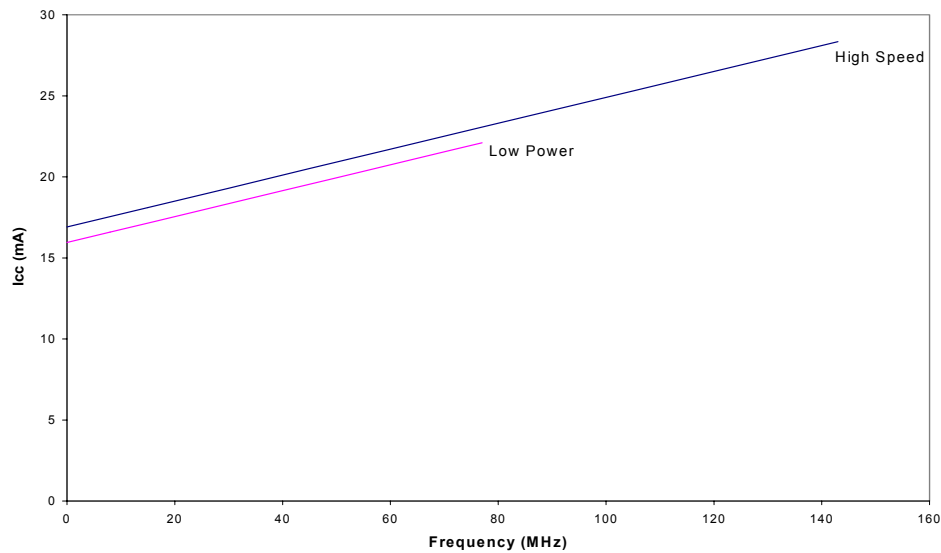
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

CY37192


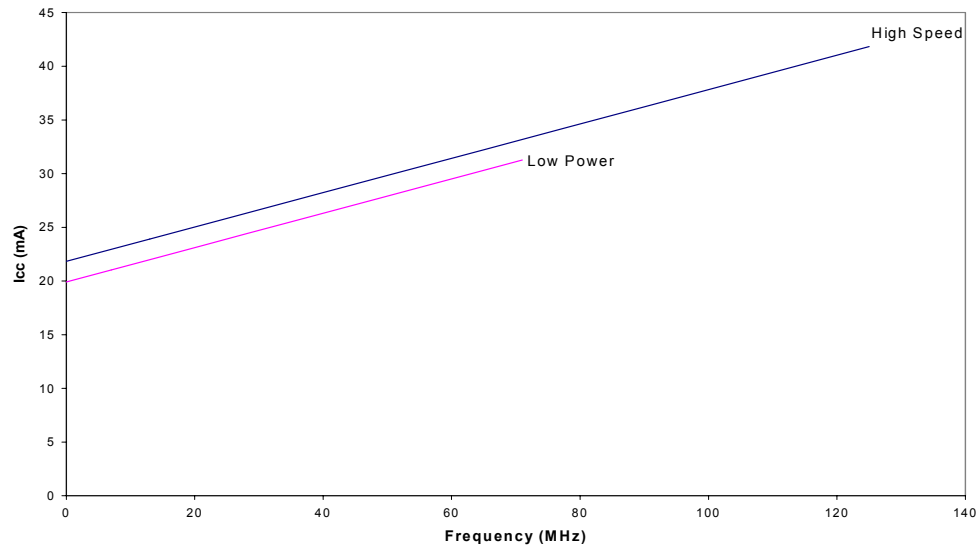
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Typical 5.0V Power Consumption (continued)
CY37512


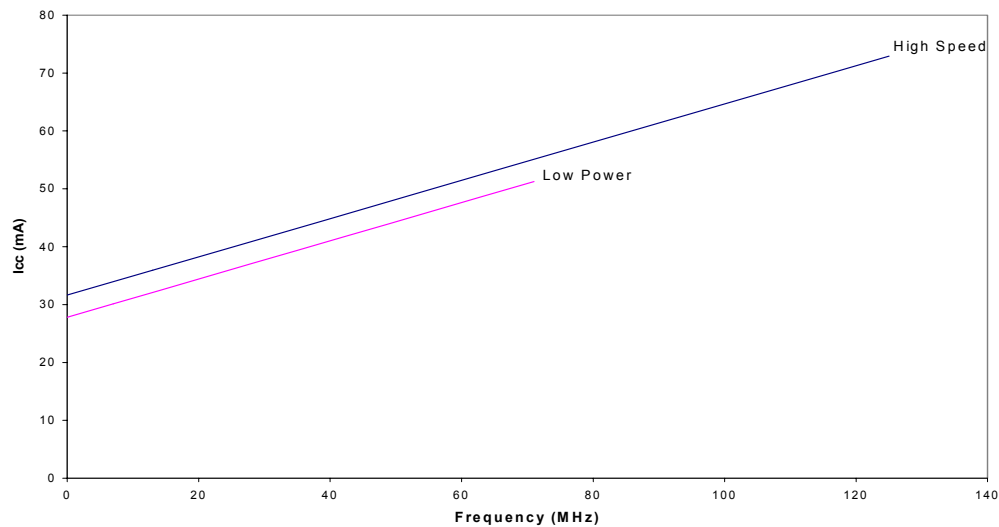
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Typical 3.3V Power Consumption
CY37032V


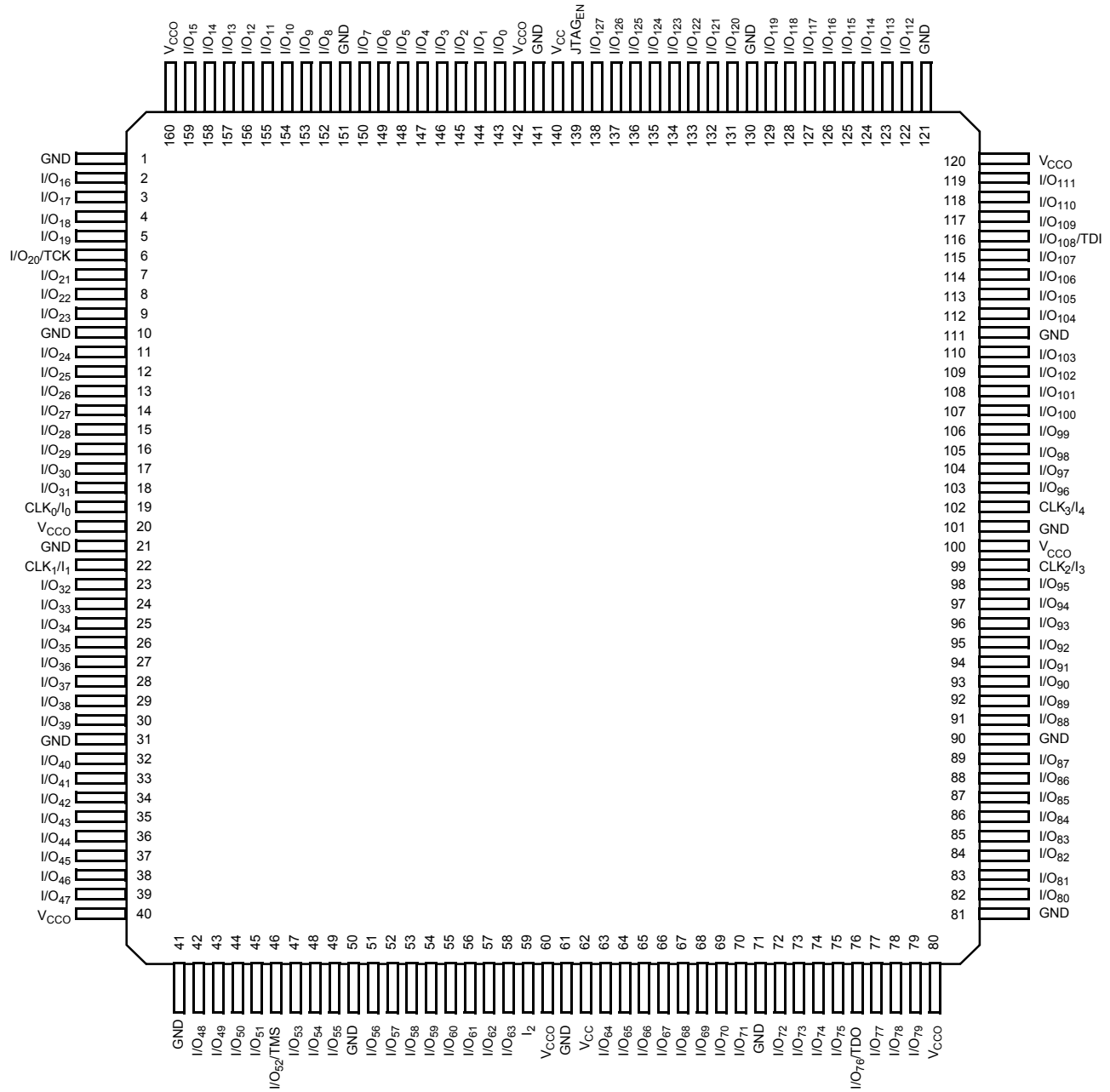
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

Typical 3.3V Power Consumption (continued)
CY37064V


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

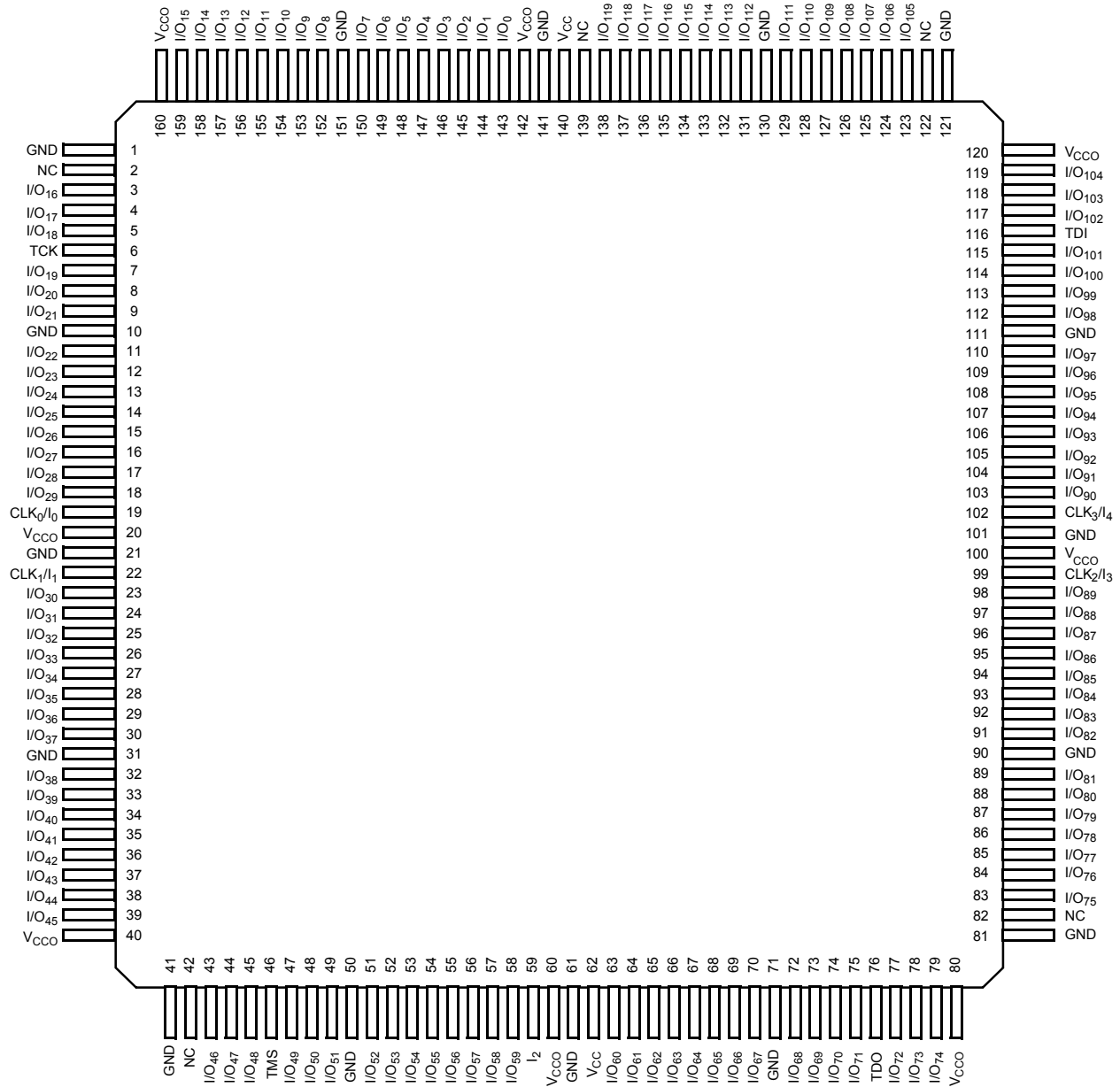
CY37128V


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

Pin Configurations^[20] (continued)
**160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View**


Pin Configurations^[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations^[20] (continued)
**292-Ball PBGA (BG292)
Top View**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O ₂₁	NC	I/O ₁₆	I/O ₁₂	I/O ₉	I/O ₇	I/O ₄	I/O ₀	I/O ₁₉₀	I/O ₁₈₉	I/O ₁₈₆	I/O ₁₈₂	NC	I/O ₁₇₈	I/O ₁₇₅	NC	NC	I/O ₁₆₉	I/O ₁₆₈	A
B	I/O ₂₃	I/O ₂₀	I/O ₁₉	I/O ₁₈	I/O ₁₅	I/O ₁₁	I/O ₈	I/O ₅	I/O ₁	I/O ₁₉₁	I/O ₁₈₇	I/O ₁₈₅	I/O ₁₈₁	NC	NC	I/O ₁₇₄	I/O ₁₇₁	I/O ₁₇₀	NC	I/O ₁₆₆	B
C	NC	NC	I/O ₂₂	NC	I/O ₁₇	I/O ₁₄	I/O ₁₀	I/O ₆	I/O ₂	NC	I/O ₁₈₈	I/O ₁₈₄	I/O ₁₈₀	I/O ₁₇₉	I/O ₁₇₆	I/O ₁₇₃	I/O ₁₇₂	I/O ₁₆₇	I/O ₁₆₅	I/O ₁₆₂	C
D	I/O ₂₄	NC	NC	GND	NC	V _{CC0}	I/O ₁₃	GND	I/O ₃	NC	V _{CC}	I/O ₁₈₃	GND	I/O ₁₇₇	V _{CC0}	NC	GND	I/O ₁₆₄	TDI	I/O ₁₆₀	D
E	I/O ₂₇	I/O ₂₆	I/O ₂₅	NC													I/O ₁₆₃	I/O ₁₆₁	I/O ₁₅₉	I/O ₁₅₆	E
F	I/O ₃₀	TCK	I/O ₂₈	V _{CC0}													V _{CC0}	I/O ₁₅₈	NC	I/O ₁₅₄	F
G	I/O ₃₃	I/O ₃₂	I/O ₃₁	I/O ₂₉													I/O ₁₅₇	I/O ₁₅₅	I/O ₁₅₃	I/O ₁₅₂	G
H	I/O ₃₅	NC	I/O ₃₄	GND	GND												GND	I/O ₁₅₁	I/O ₁₅₀	I/O ₁₄₉	H
J	I/O ₃₉	I/O ₃₈	I/O ₃₇	I/O ₃₆	GND												I/O ₁₄₈	I/O ₁₄₇	I/O ₁₄₆	I/O ₁₄₅	J
K	I/O ₄₂	I/O ₄₀	I/O ₄₁	V _{CC}	GND												I/O ₁₄₄	CLK ₃ /I ₄	NC	NC	K
L	I/O ₄₃	I/O ₄₄	I/O ₄₅	I/O ₄₆	GND												V _{CC}	CLK ₂ /I ₃	I/O ₁₄₃	NC	L
M	I/O ₄₇	CLK ₀ /I ₀	CLK ₁ /I ₁	I/O ₄₈	GND												I/O ₁₃₉	I/O ₁₄₀	I/O ₁₄₁	I/O ₁₄₂	M
N	I/O ₄₉	I/O ₅₀	I/O ₅₁	GND	GND												GND	I/O ₁₃₆	I/O ₁₃₇	I/O ₁₃₈	N
P	I/O ₅₂	I/O ₅₃	I/O ₅₅	I/O ₅₈													I/O ₁₃₁	I/O ₁₃₃	I/O ₁₃₄	I/O ₁₃₅	P
R	I/O ₅₄	I/O ₅₆	I/O ₅₉	V _{CC0}													V _{CC0}	I/O ₁₃₀	NC	I/O ₁₃₂	R
T	I/O ₅₇	I/O ₆₀	I/O ₆₂	I/O ₆₅													I/O ₁₂₄	I/O ₁₂₇	I/O ₁₂₈	I/O ₁₂₉	T
U	I/O ₆₁	I/O ₆₃	I/O ₆₆	GND	I/O ₇₆	V _{CC0}	I/O ₈₂	GND	I/O ₉₁	V _{CC}	I/O ₉₈	I/O ₁₀₂	GND	I/O ₁₁₂	V _{CC0}	NC	GND	I/O ₁₂₃	I/O ₁₂₂	I/O ₁₂₆	U
V	I/O ₆₄	I/O ₆₇	I/O ₆₉	I/O ₇₅	I/O ₇₈	I/O ₈₁	I/O ₈₅	I/O ₈₈	I/O ₉₂	I ₂	I/O ₉₇	I/O ₁₀₁	I/O ₁₀₅	I/O ₁₀₉	I/O ₁₁₃	TD0	I/O ₁₁₄	I/O ₁₁₇	I/O ₁₂₁	I/O ₁₂₅	V
W	I/O ₆₈	I/O ₇₀	I/O ₇₂	I/O ₇₄	I/O ₇₉	I/O ₈₃	I/O ₈₆	I/O ₈₉	I/O ₉₃	I/O ₉₅	I/O ₉₆	I/O ₁₀₀	I/O ₁₀₄	I/O ₁₀₇	I/O ₁₁₀	NC	NC	I/O ₁₁₅	I/O ₁₁₈	I/O ₁₂₀	W
Y	I/O ₇₁	I/O ₇₃	I/O ₇₇	TMS	I/O ₈₀	I/O ₈₄	I/O ₈₇	I/O ₉₀	I/O ₉₄	NC	NC	I/O ₉₉	I/O ₁₀₃	I/O ₁₀₆	I/O ₁₀₈	I/O ₁₁₁	NC	NC	I/O ₁₁₆	I/O ₁₁₉	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
128	167	CY37128P84-167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-167JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-167AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-167AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-167AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-167AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	125	CY37128P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-125JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P84-125JXI	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-125AI	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		5962-9952102QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
	100	CY37128P84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-100JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-100AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-100AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-100AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128P84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-100AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-100AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-100AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952101QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	154	CY37192P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-154AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	125	CY37192P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37192P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	83	CY37192P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37192P160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	

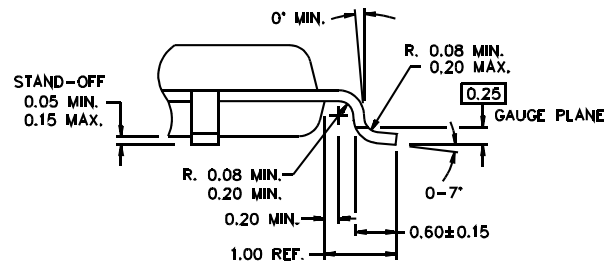
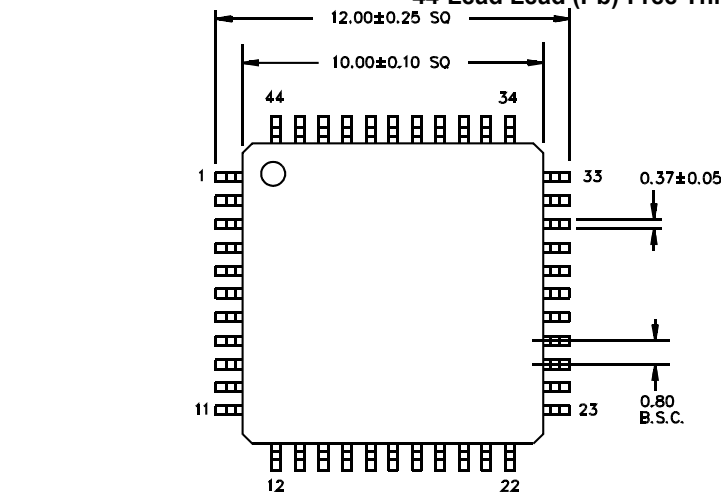
3.3V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

Package Diagrams

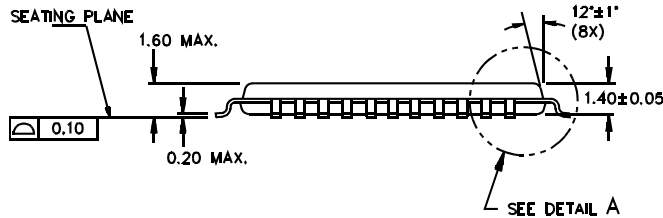
44-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack A44

DIMENSIONS ARE IN MILLIMETERS



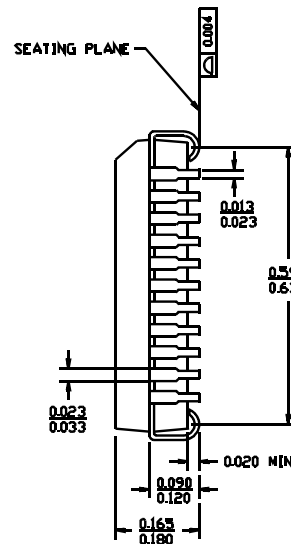
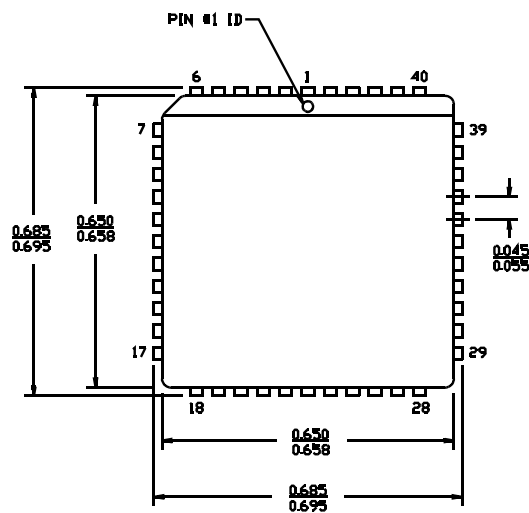
DETAIL A

51-85064-*B



44-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J67

DIMENSIONS IN INCHES MIN. MAX.



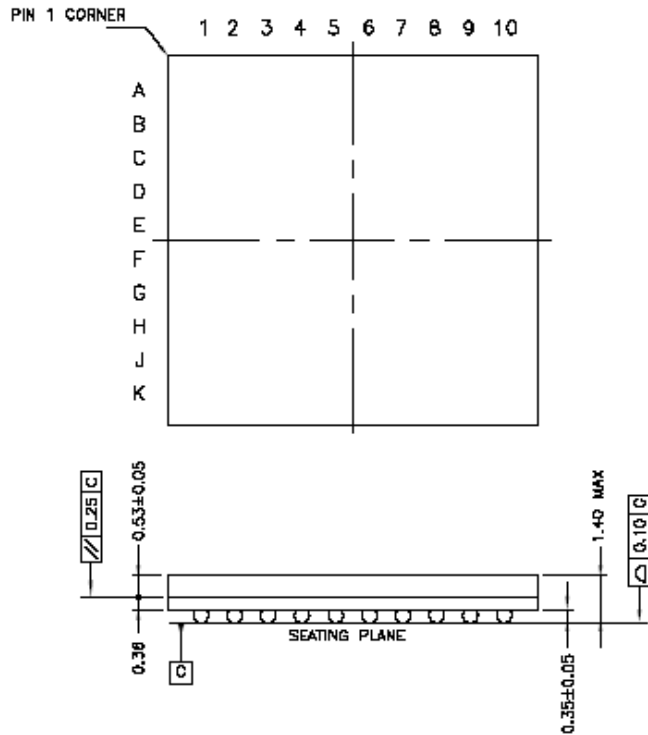
51-85003-*A



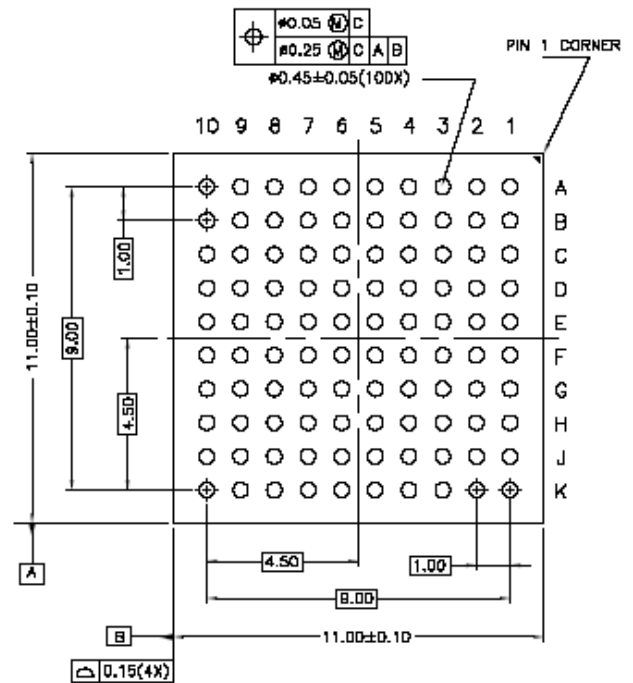
Package Diagrams (continued)

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100

TOP VIEW



BOTTOM VIEW



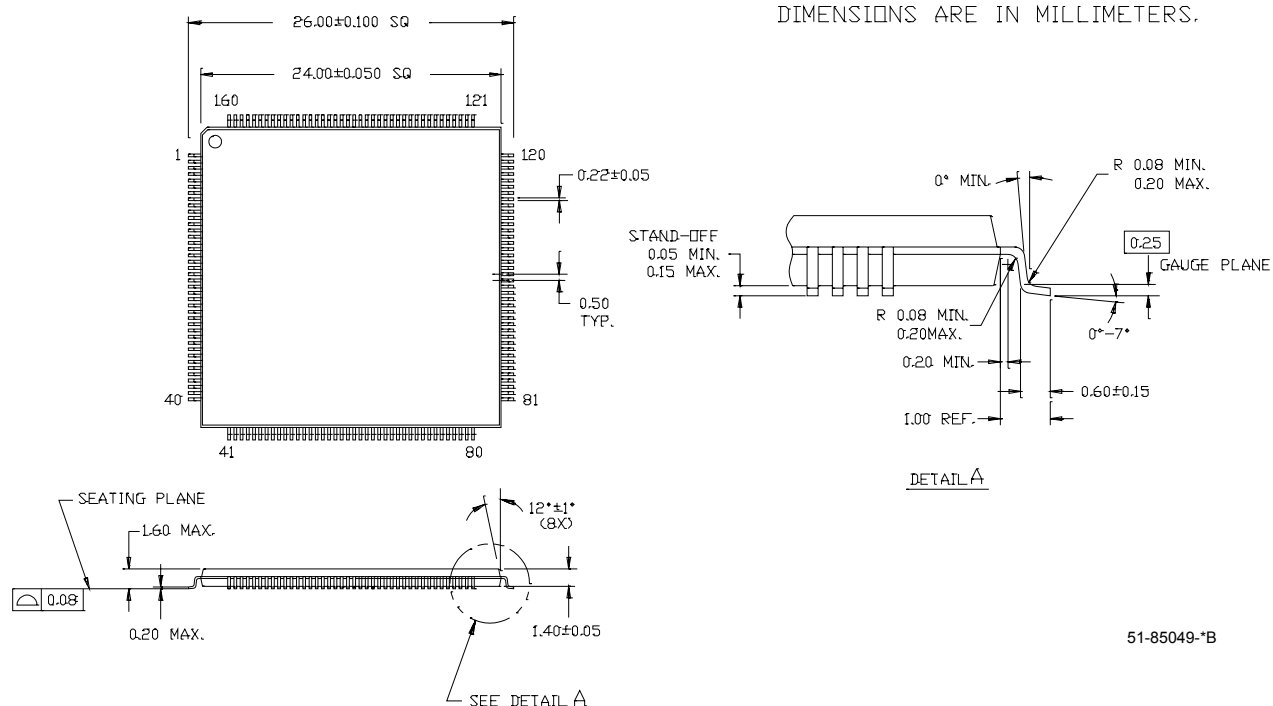
51-85107-B



Ultra37000 CPLD Family

Package Diagrams (continued)

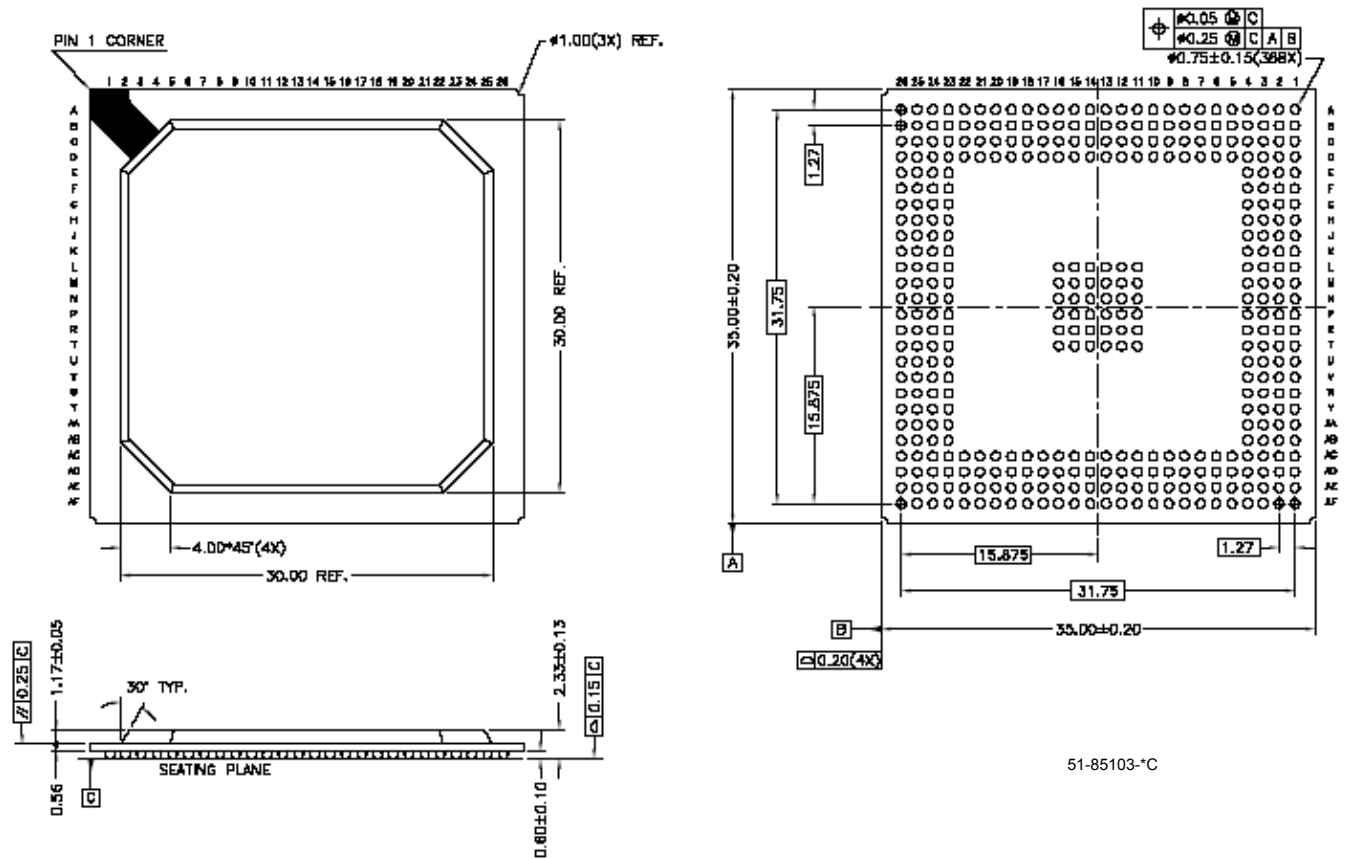
160-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (24 x 24 x 1.4 mm) (TQFP) A160



51-85049-*B

Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388



51-85103-°C