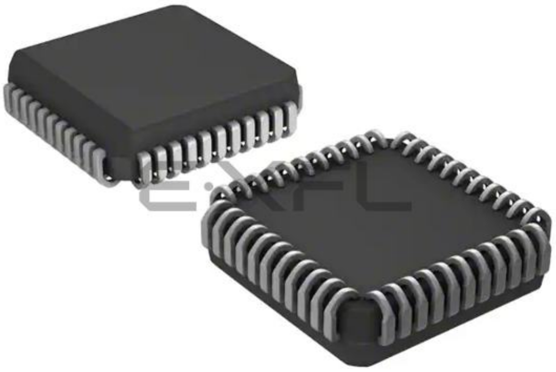


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	37
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.61x16.61)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37064p44-154jxi

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V					X		X	
CY37192V						X		X
CY37256V						X		X
CY37384V							X	X
CY37512V							X	X

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead CLCC	48-Lead FBGA	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	256-Lead FBGA	388-Lead PBGA	400-Lead FBGA
CY37032V	37		37											
CY37064V	37	37	37		69	69								
CY37128V				69	69	85	133							
CY37192V							125							
CY37256V							133	133	165		197	197		
CY37384V									165		197			
CY37512V									165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The PIM consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*® and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note *Understanding Bus-Hold—A Feature of Cypress CPLDs*.

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

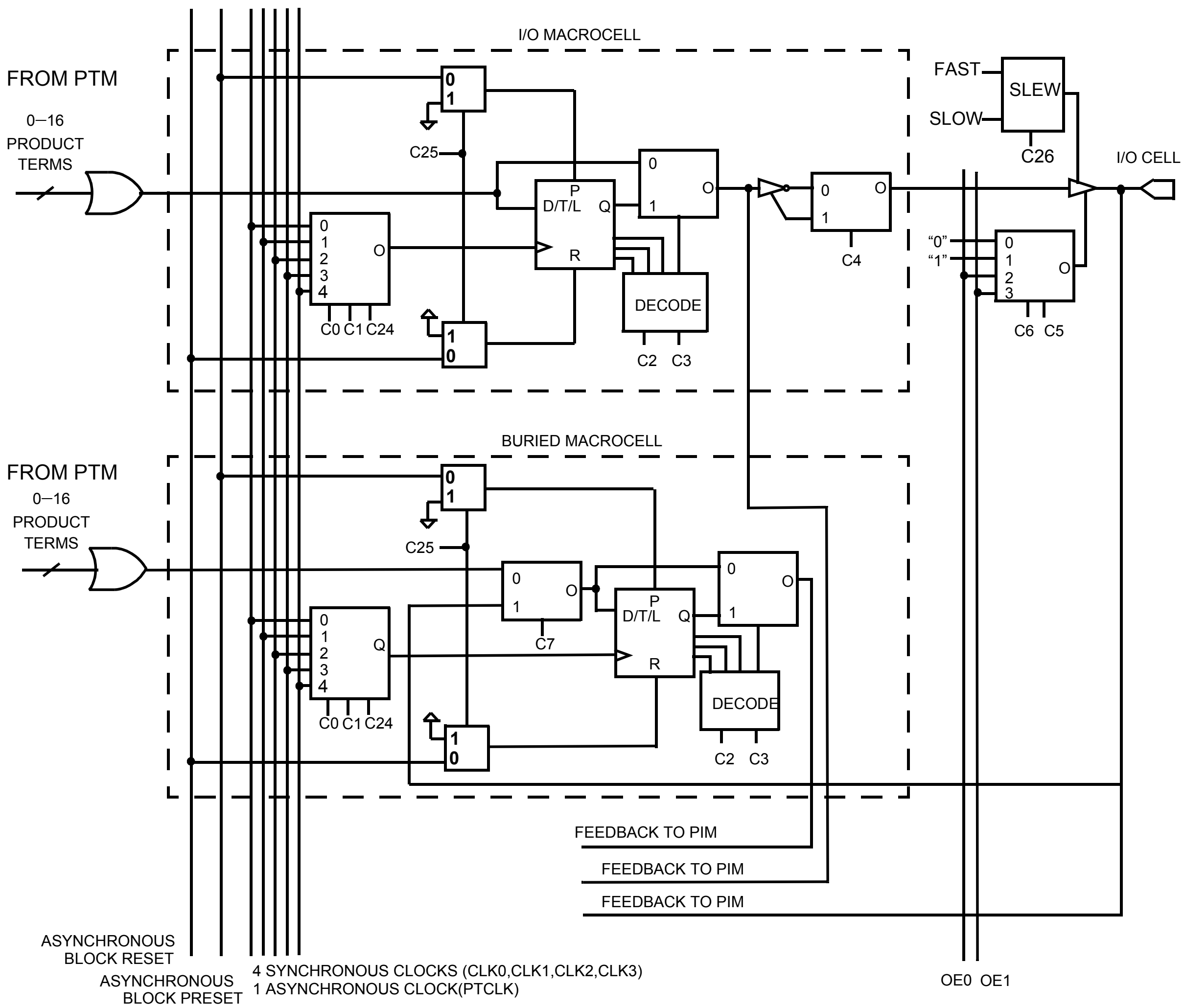


Figure 2. I/O and Buried Macrocells

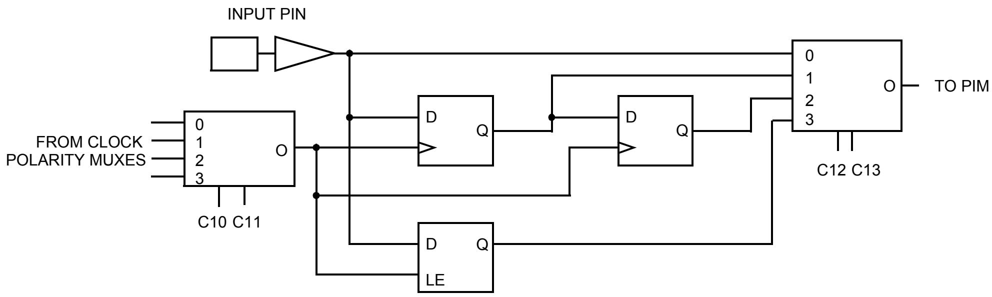


Figure 3. Input Macrocell

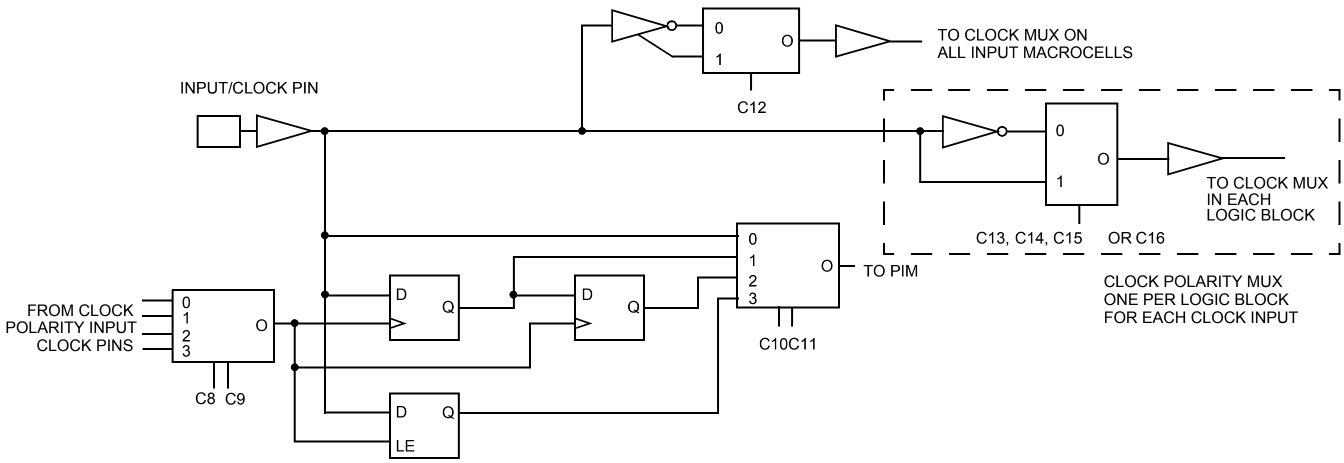


Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

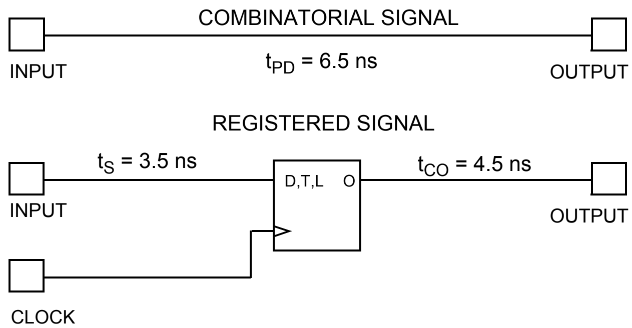


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

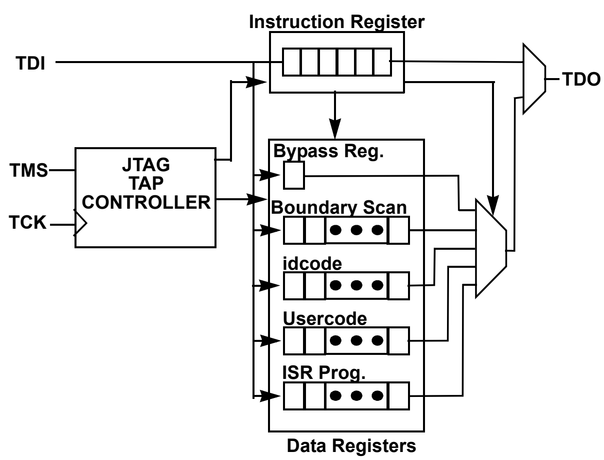


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC, *Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

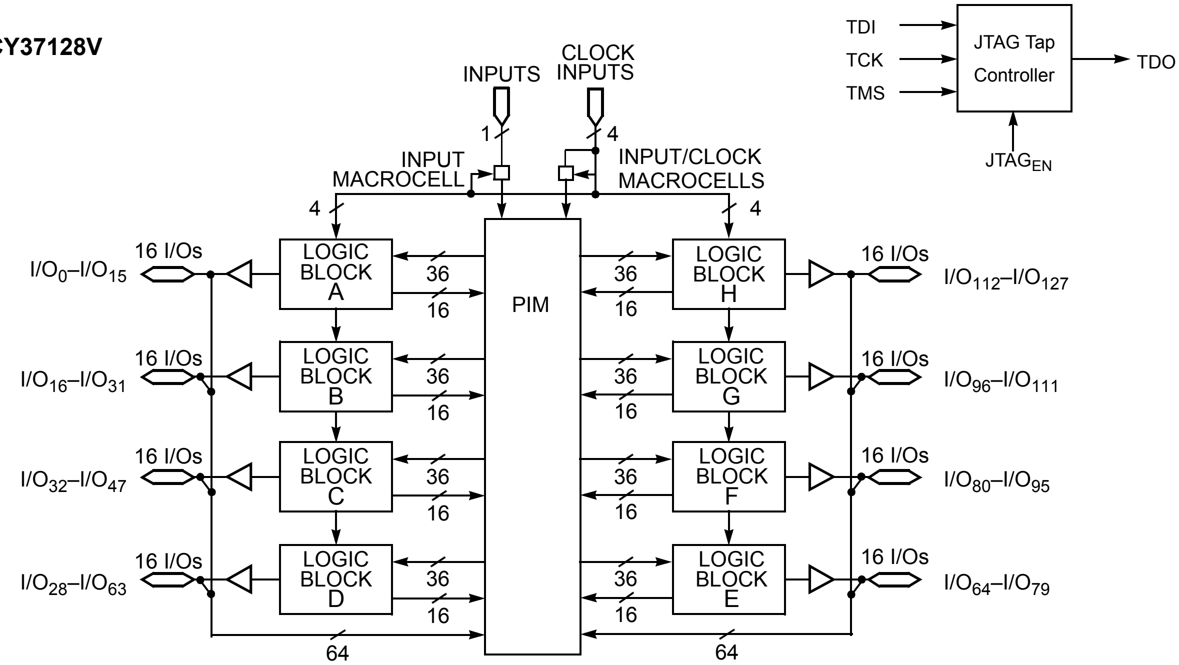
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

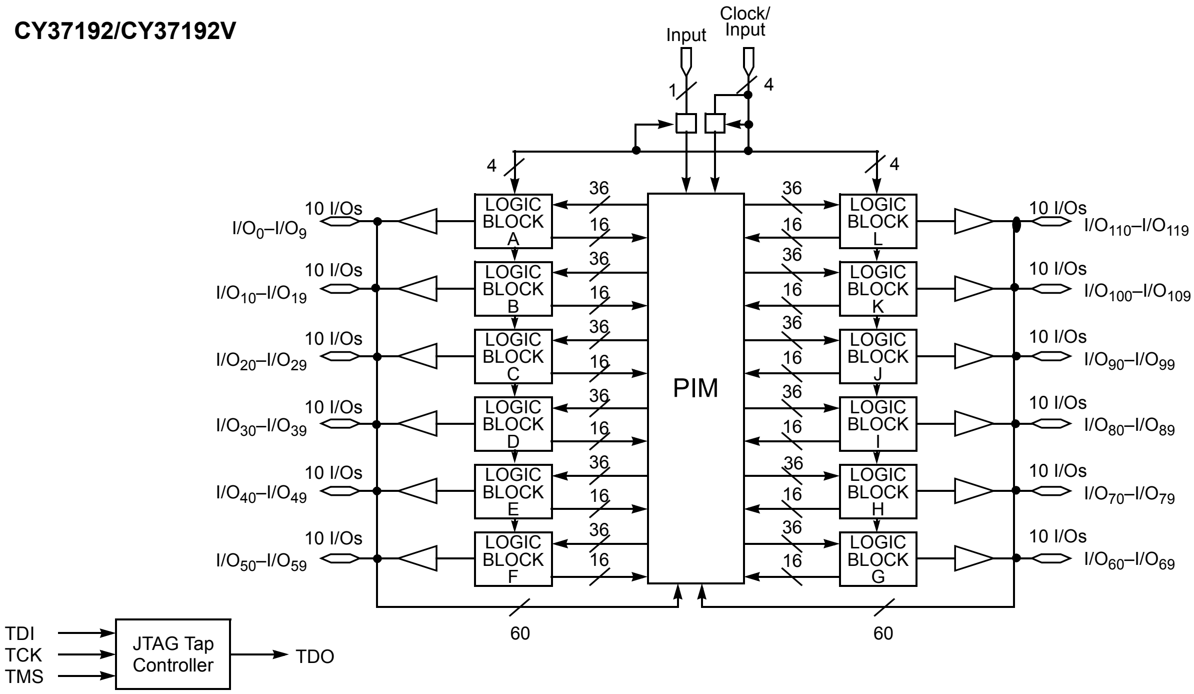
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams (continued)

CY37128/CY37128V

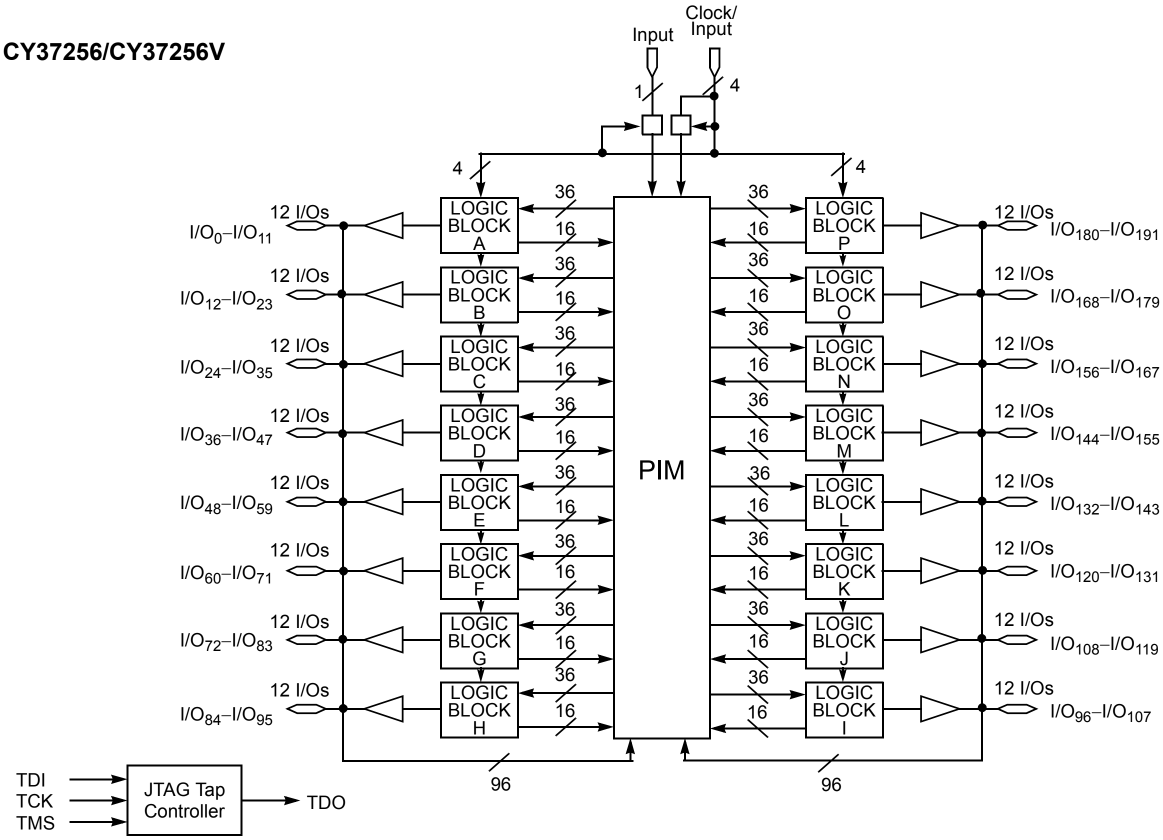


CY37192/CY37192V



Logic Block Diagrams (continued)

CY37256/CY37256V



5.0V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied..–55°C to +125°C

Supply Voltage to Ground Potential ....–0.5V to +7.0V

DC Voltage Applied to Outputs
in High-Z State..–0.5V to +7.0V

DC Input Voltage ....–0.5V to +7.0V

DC Program Voltage... 4.5 to 5.5V

Current into Outputs .... 16 mA

Static Discharge Voltage.. > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current... > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

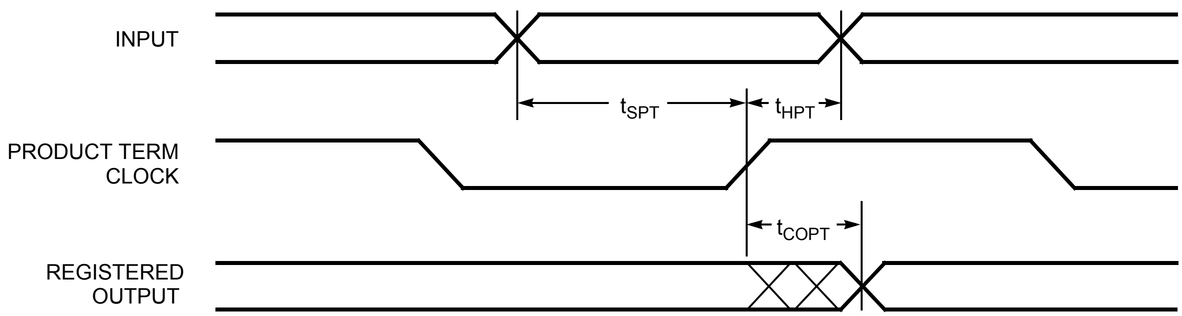
5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[5]	V_{CC} = Max.	I_{OH} = 0 μA (Com'l)[6]			4.2	V
			I_{OH} = 0 μA (Ind/Mil)[6]			4.5	V
			I_{OH} = –100 μA (Com'l)[6]			3.6	V
			I_{OH} = –150 μA (Ind/Mil)[6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	μA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	μA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			μA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			μA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.				+500	μA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.				–500	μA

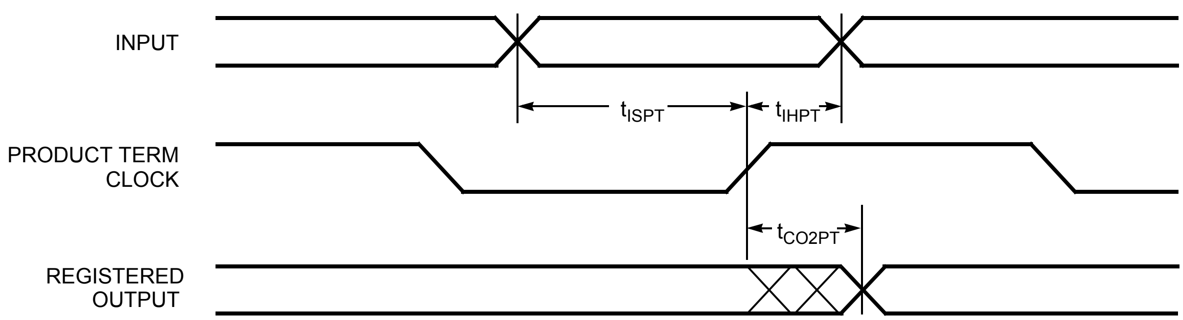
Notes:
2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled “An Introduction to In System Reprogramming with the Ultra37000.”
3. T_A is the “Instant On” case temperature.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note “Understanding Bus-Hold” for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Switching Waveforms (continued)

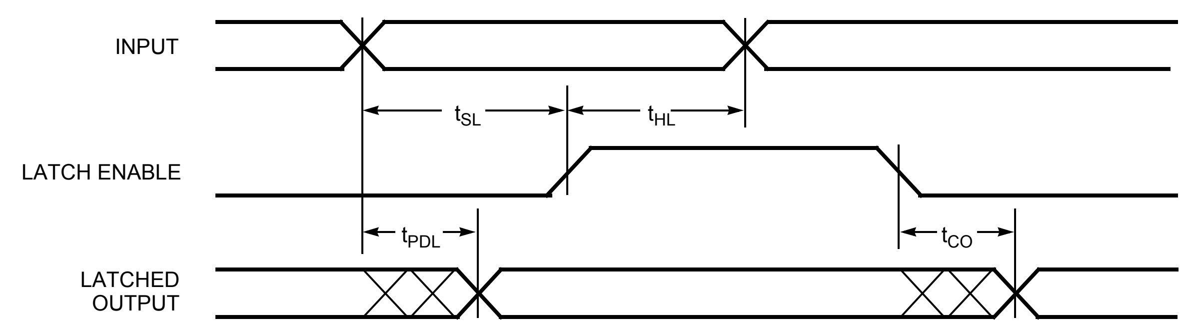
Registered Output with Product Term Clocking Input Going Through the Array



Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register

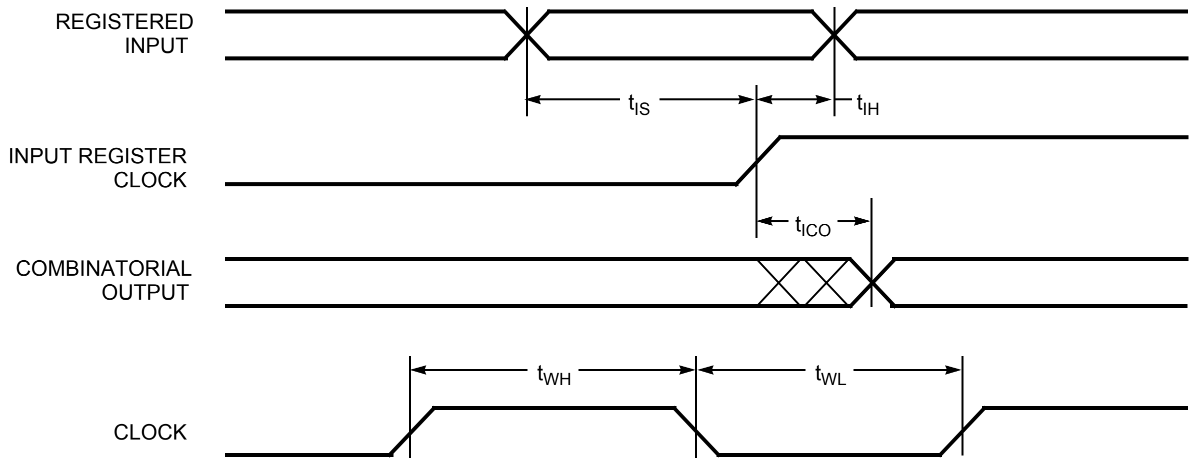


Latched Output

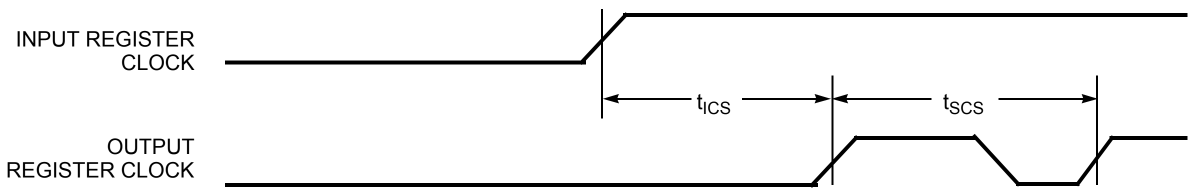


Switching Waveforms (continued)

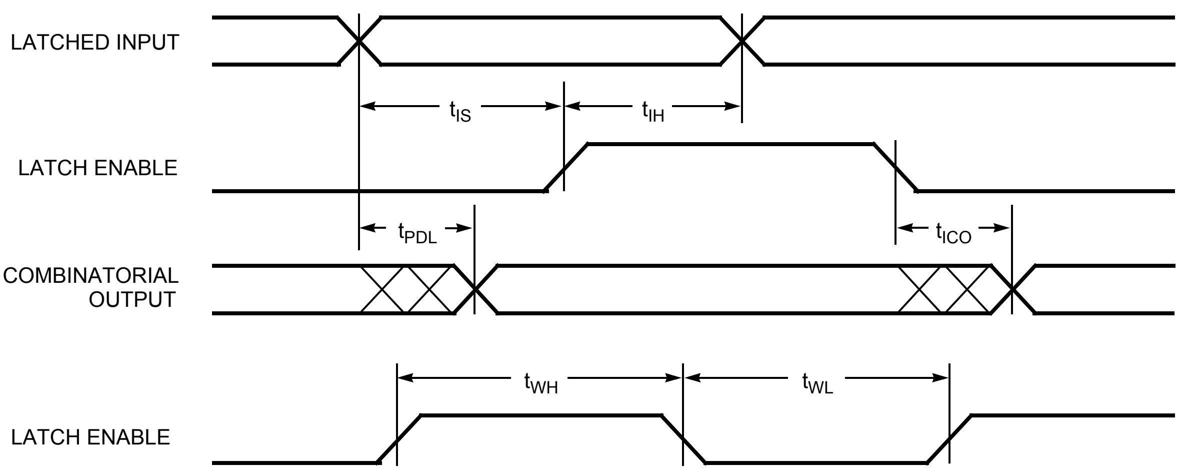
Registered Input



Clock to Clock

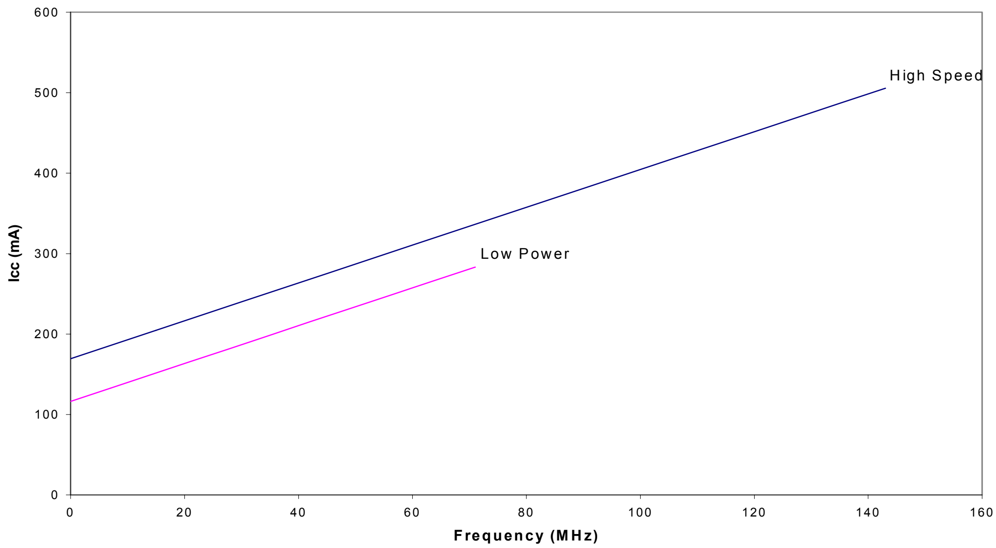


Latched Input



Typical 5.0V Power Consumption (continued)

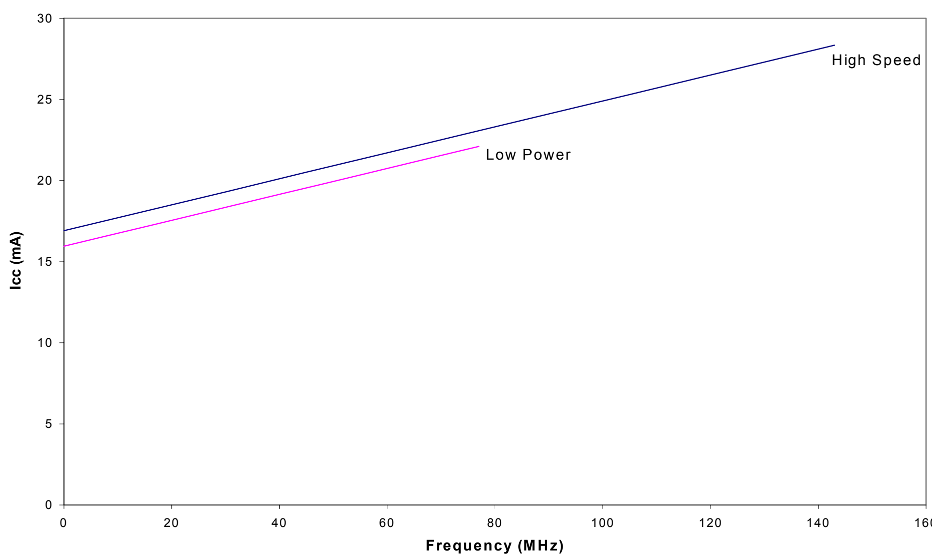
CY37512



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 3.3V Power Consumption

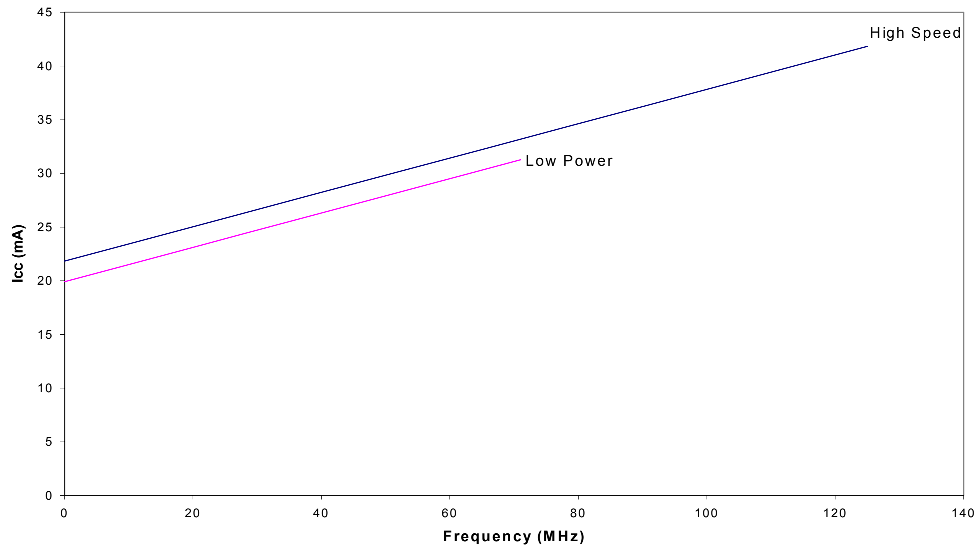
CY37032V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

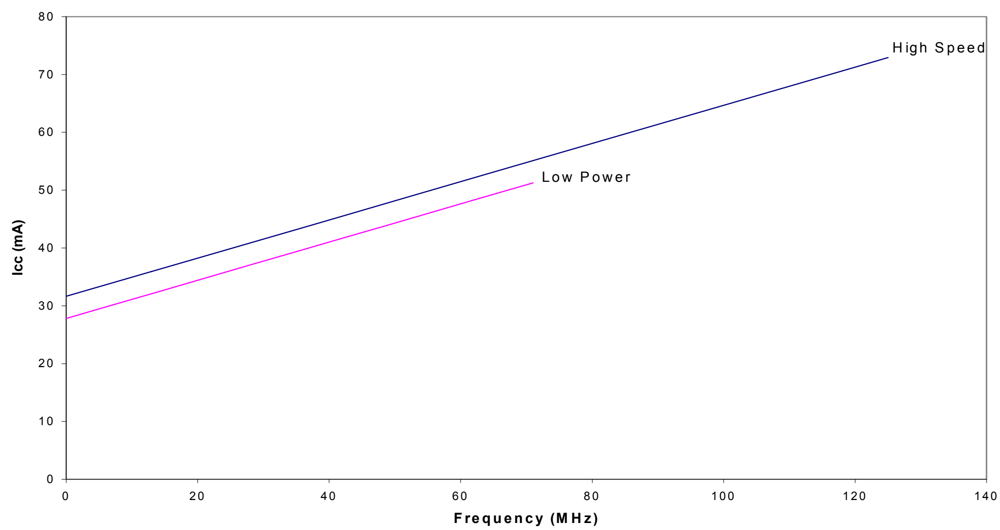
Typical 3.3V Power Consumption (continued)

CY37064V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

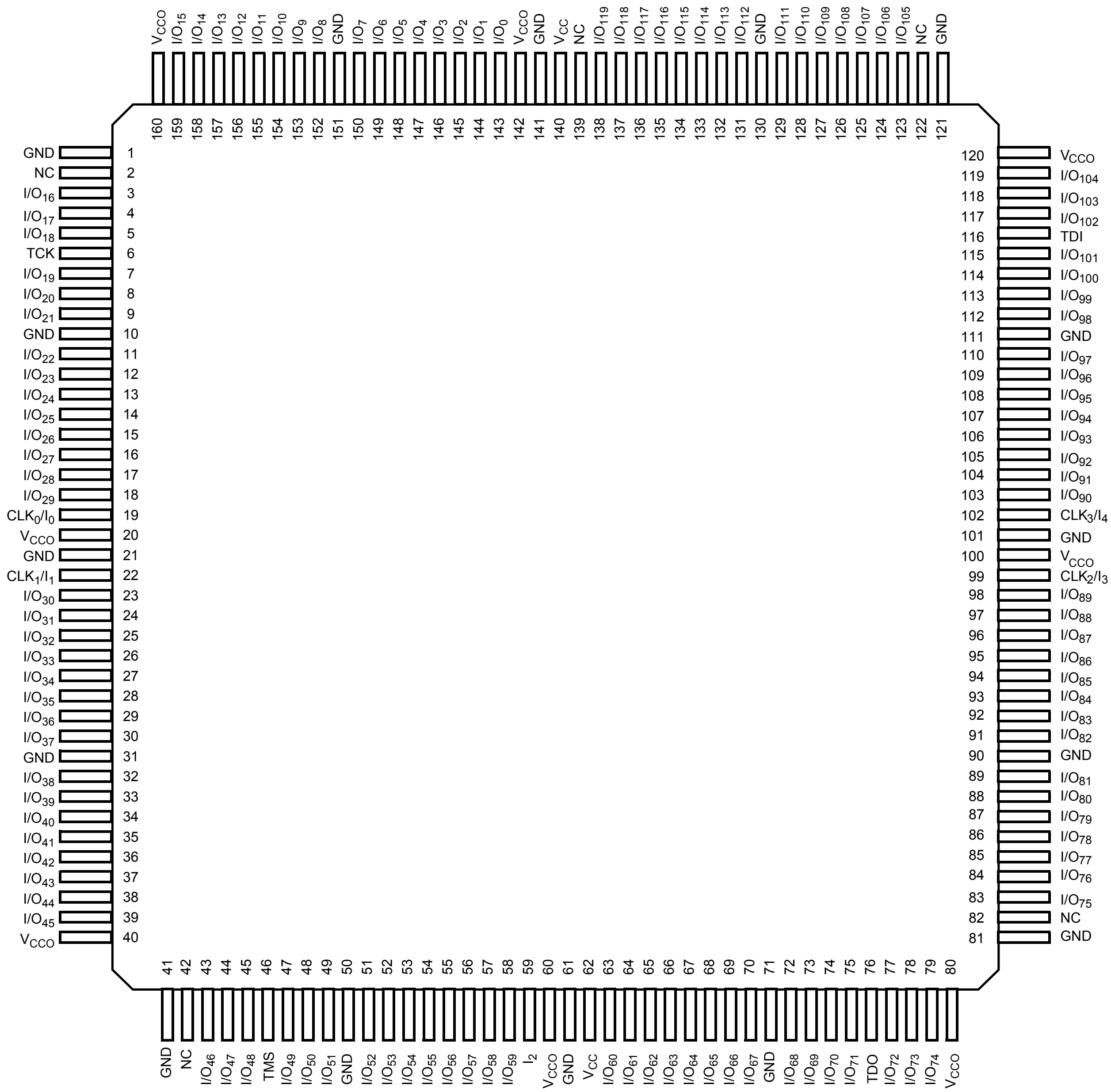
CY37128V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

Pin Configurations[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[20] (continued)

256-Ball Fine-Pitch BGA (BB256)
Top View

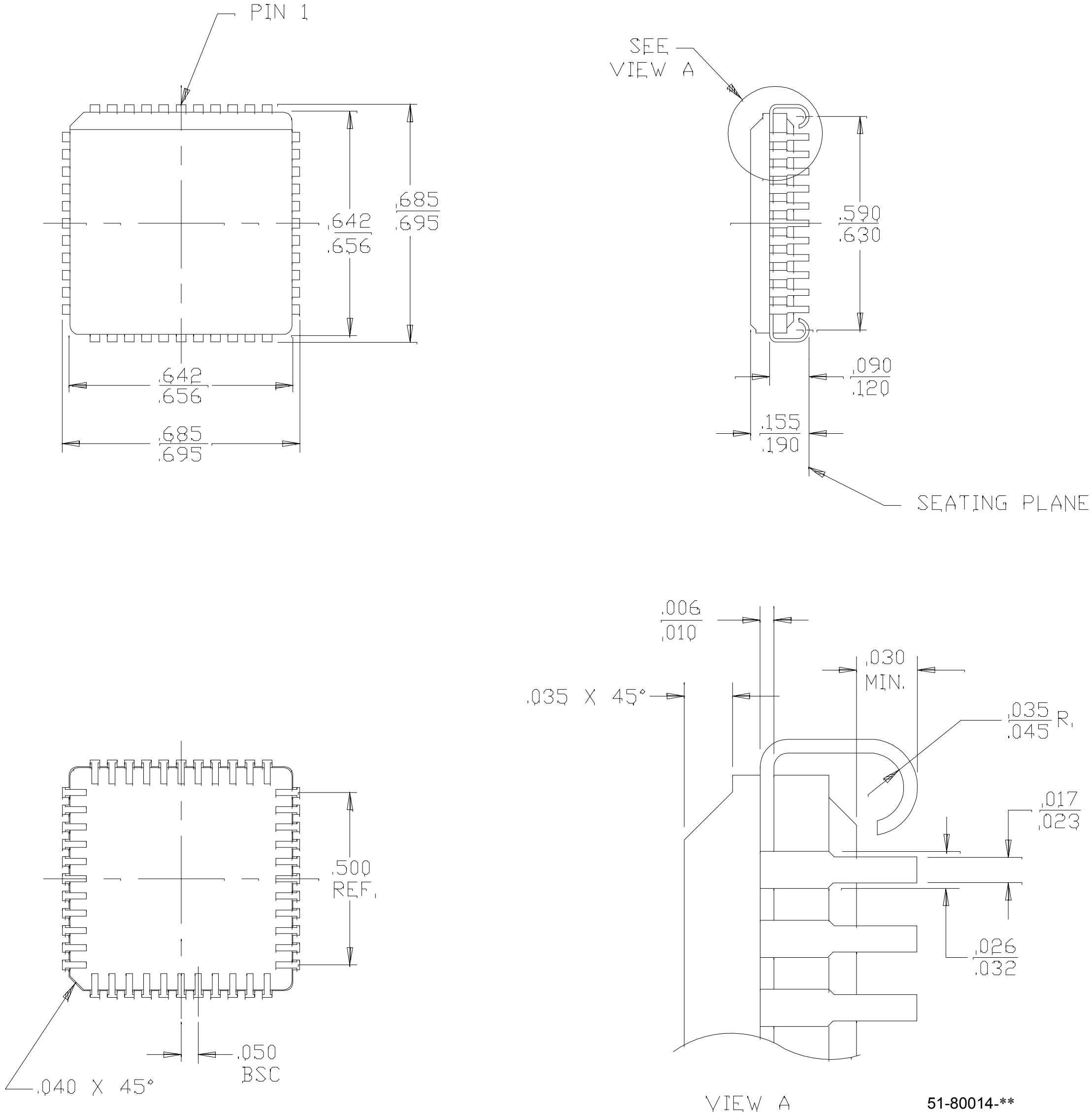
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	I/O$_{26}$	I/O$_{24}$	I/O$_{20}$	V_{CC}	I/O$_{11}$	GND	GND	I/O$_{186}$	V_{CC}	I/O$_{177}$	I/O$_{172}$	I/O$_{167}$	GND	GND
B	GND	I/O$_{27}$	I/O$_{25}$	I/O$_{23}$	I/O$_{19}$	I/O$_{15}$	I/O$_{10}$	GND	GND	I/O$_{185}$	I/O$_{181}$	I/O$_{176}$	I/O$_{171}$	I/O$_{166}$	I/O$_{165}$	GND
C	I/O$_{29}$	I/O$_{28}$	NC	I/O$_{22}$	I/O$_{18}$	I/O$_{14}$	I/O$_{9}$	I/O$_{4}$	I/O$_{191}$	I/O$_{184}$	I/O$_{180}$	I/O$_{175}$	I/O$_{170}$	NC	I/O$_{163}$	I/O$_{164}$
D	I/O$_{32}$	I/O$_{31}$	I/O$_{30}$	NC	I/O$_{17}$	I/O$_{13}$	I/O$_{8}$	I/O$_{3}$	I/O$_{190}$	I/O$_{183}$	I/O$_{179}$	I/O$_{174}$	I/O$_{169}$	I/O$_{160}$	I/O$_{161}$	I/O$_{162}$
E	I/O$_{35}$	I/O$_{34}$	I/O$_{33}$	I/O$_{21}$	I/O$_{16}$	I/O$_{12}$	I/O$_{7}$	I/O$_{2}$	I/O$_{189}$	V_{CC}	I/O$_{178}$	I/O$_{173}$	I/O$_{168}$	I/O$_{157}$	I/O$_{158}$	I/O$_{159}$
F	V_{CC}	I/O$_{38}$	I/O$_{37}$	I/O$_{36}$	TCK	V_{CC}	I/O$_{6}$	I/O$_{1}$	I/O$_{188}$	I/O$_{182}$	V_{CC}	TDI	I/O$_{154}$	I/O$_{155}$	I/O$_{156}$	V_{CC}
G	I/O$_{43}$	I/O$_{42}$	I/O$_{41}$	I/O$_{40}$	V_{CC}	I/O$_{39}$	I/O$_{5}$	I/O$_{0}$	I/O$_{187}$	I/O$_{148}$	I/O$_{149}$	CLK$_{3}$ /I$_{4}$	I/O$_{150}$	I/O$_{151}$	I/O$_{152}$	I/O$_{153}$
H	GND	GND	I/O$_{47}$	I/O$_{46}$	CLK$_{0}$ /I$_{0}$	I/O$_{45}$	I/O$_{44}$	GND	GND	I/O$_{144}$	I/O$_{145}$	CLK$_{2}$ /I$_{3}$	I/O$_{146}$	I/O$_{147}$	GND	GND
J	GND	GND	I/O$_{51}$	I/O$_{50}$	NC	I/O$_{49}$	I/O$_{48}$	GND	GND	I/O$_{140}$	I/O$_{141}$	I$_{2}$	I/O$_{142}$	I/O$_{143}$	GND	GND
K	I/O$_{57}$	I/O$_{56}$	I/O$_{55}$	I/O$_{54}$	CLK$_{1}$ /I$_{1}$	I/O$_{53}$	I/O$_{52}$	I/O$_{91}$	I/O$_{96}$	I/O$_{101}$	I/O$_{135}$	V_{CC}	I/O$_{136}$	I/O$_{137}$	I/O$_{138}$	I/O$_{139}$
L	V_{CC}	I/O$_{60}$	I/O$_{59}$	I/O$_{58}$	TMS	V_{CC}	I/O$_{86}$	I/O$_{92}$	I/O$_{97}$	I/O$_{102}$	V_{CC}	TDO	I/O$_{132}$	I/O$_{133}$	I/O$_{134}$	V_{CC}
M	I/O$_{63}$	I/O$_{62}$	I/O$_{61}$	I/O$_{72}$	I/O$_{77}$	I/O$_{82}$	V_{CC}	I/O$_{93}$	I/O$_{98}$	I/O$_{103}$	I/O$_{108}$	I/O$_{112}$	I/O$_{117}$	I/O$_{129}$	I/O$_{130}$	I/O$_{131}$
N	I/O$_{66}$	I/O$_{65}$	I/O$_{64}$	I/O$_{73}$	I/O$_{78}$	I/O$_{83}$	I/O$_{87}$	I/O$_{94}$	I/O$_{99}$	I/O$_{104}$	I/O$_{109}$	I/O$_{113}$	NC	I/O$_{126}$	I/O$_{127}$	I/O$_{128}$
P	I/O$_{68}$	I/O$_{67}$	NC	I/O$_{74}$	I/O79	I/O$_{84}$	I/O$_{88}$	I/O$_{95}$	I/O$_{100}$	I/O$_{105}$	I/O$_{110}$	I/O$_{114}$	I/O$_{118}$	NC	I/O$_{124}$	I/O$_{125}$
R	GND	I/O$_{69}$	I/O$_{70}$	I/O$_{75}$	I/O$_{80}$	I/O$_{85}$	I/O$_{89}$	GND	GND	I/O$_{106}$	I/O$_{111}$	I/O$_{115}$	I/O$_{119}$	I/O$_{121}$	I/O$_{123}$	GND
T	GND	GND	I/O$_{71}$	I/O$_{76}$	I/O$_{81}$	V_{CC}	I/O$_{90}$	GND	GND	I/O$_{107}$	V_{CC}	I/O$_{116}$	I/O$_{120}$	I/O$_{122}$	GND	GND

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military

Package Diagrams (continued)

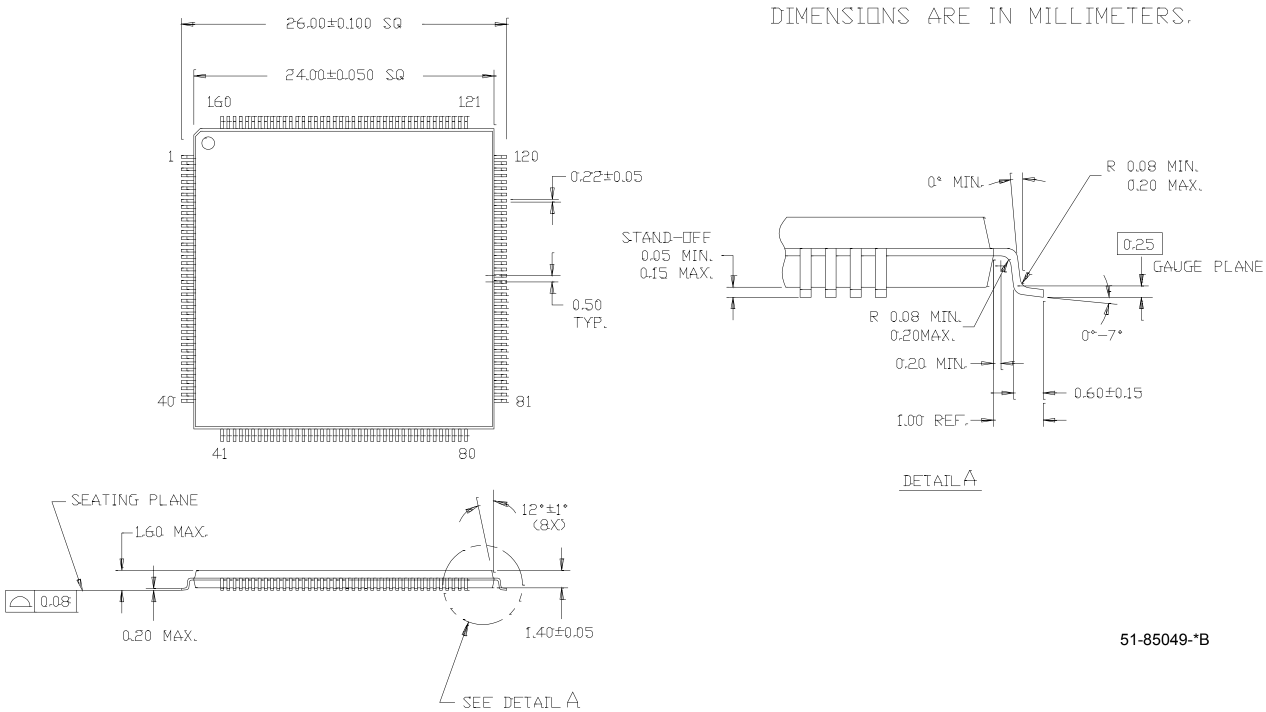
44-Lead Ceramic Leaded Chip Carrier Y67



51-80014-**

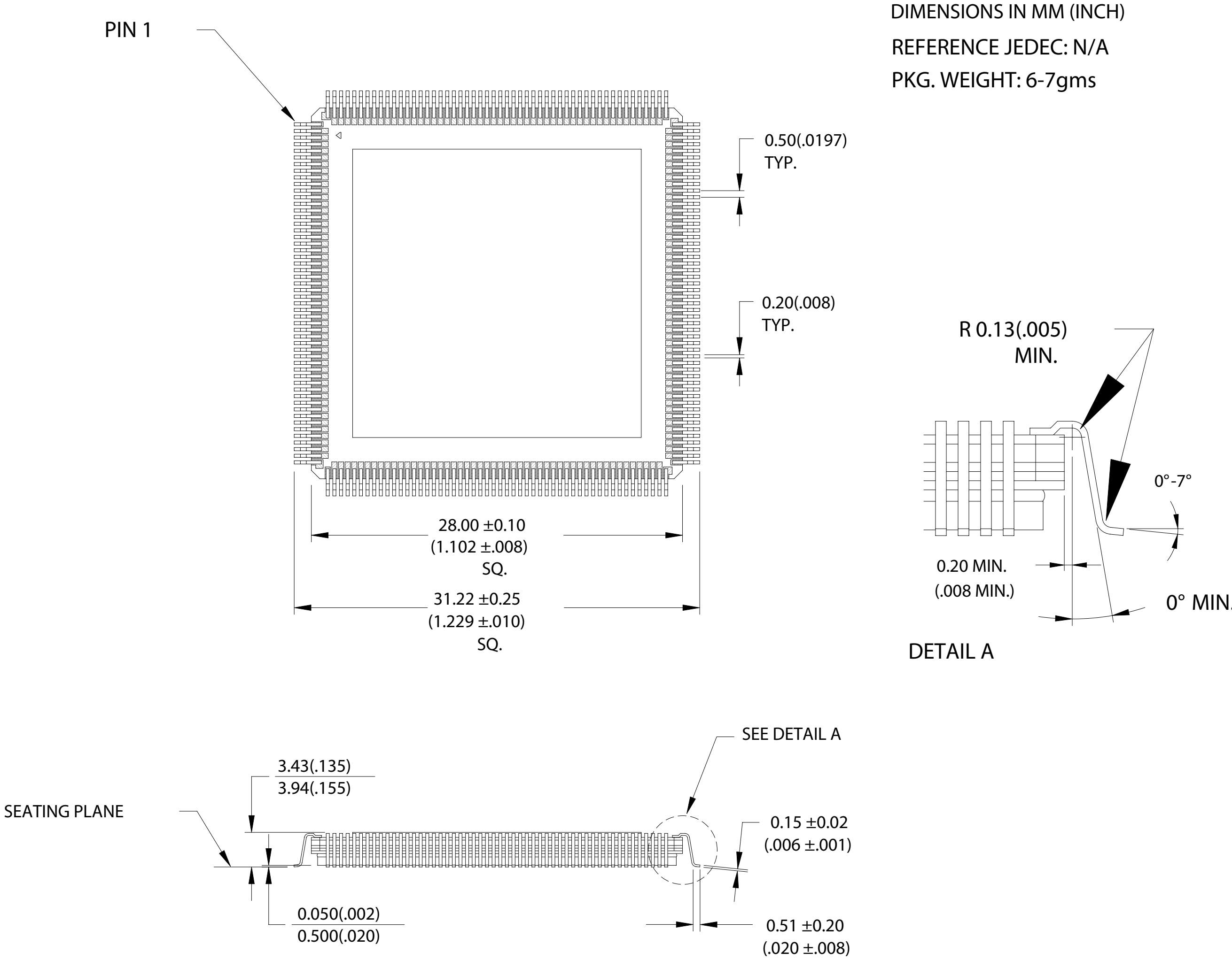
Package Diagrams (continued)

160-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (24 x 24 x 1.4 mm) (TQFP) A160



Package Diagrams (continued)

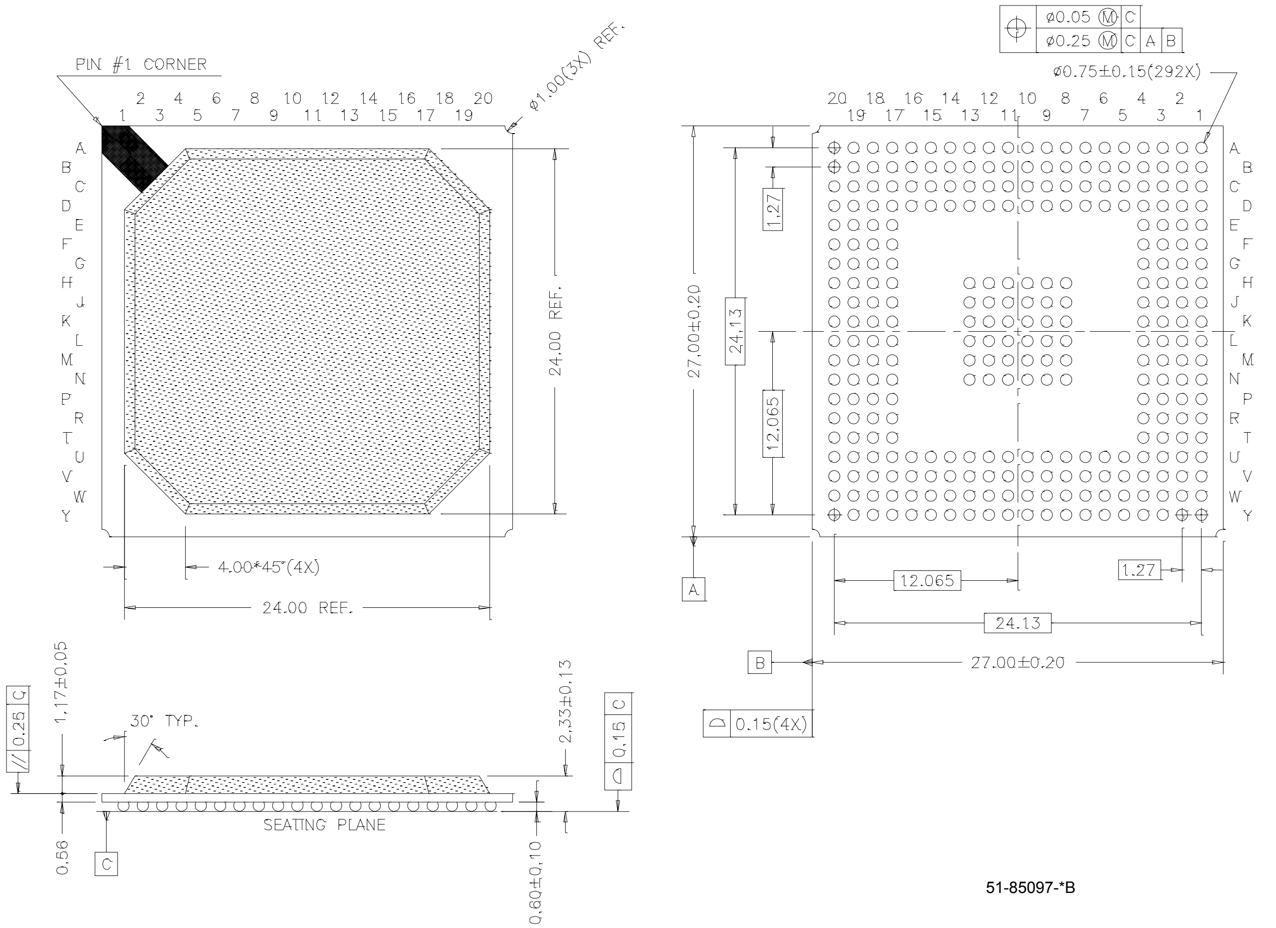
208-Lead Ceramic Quad Flatpack (Cavity Up) U208



51-80105-*B

Package Diagrams (continued)

292-Ball Plastic Ball Grid Array PBGA (27 x 27 x 2.33 mm) BG292



51-85097-*B

Addendum

3.3V Operating Range

(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.16V