



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) Flash
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	37
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37064vp44-100axc

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

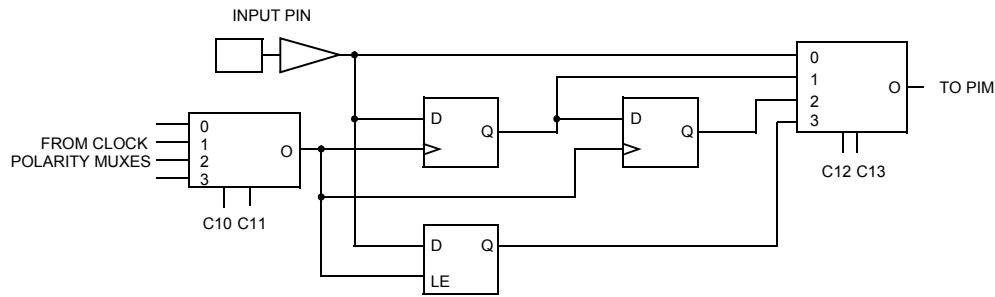
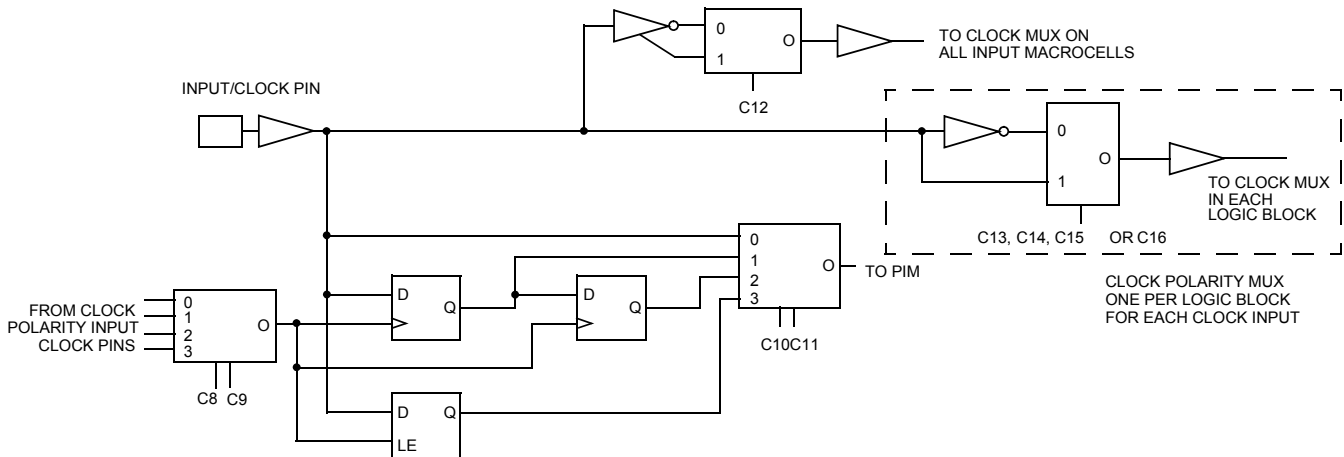
Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	388-Lead PBGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83


Figure 3. Input Macrocell

Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

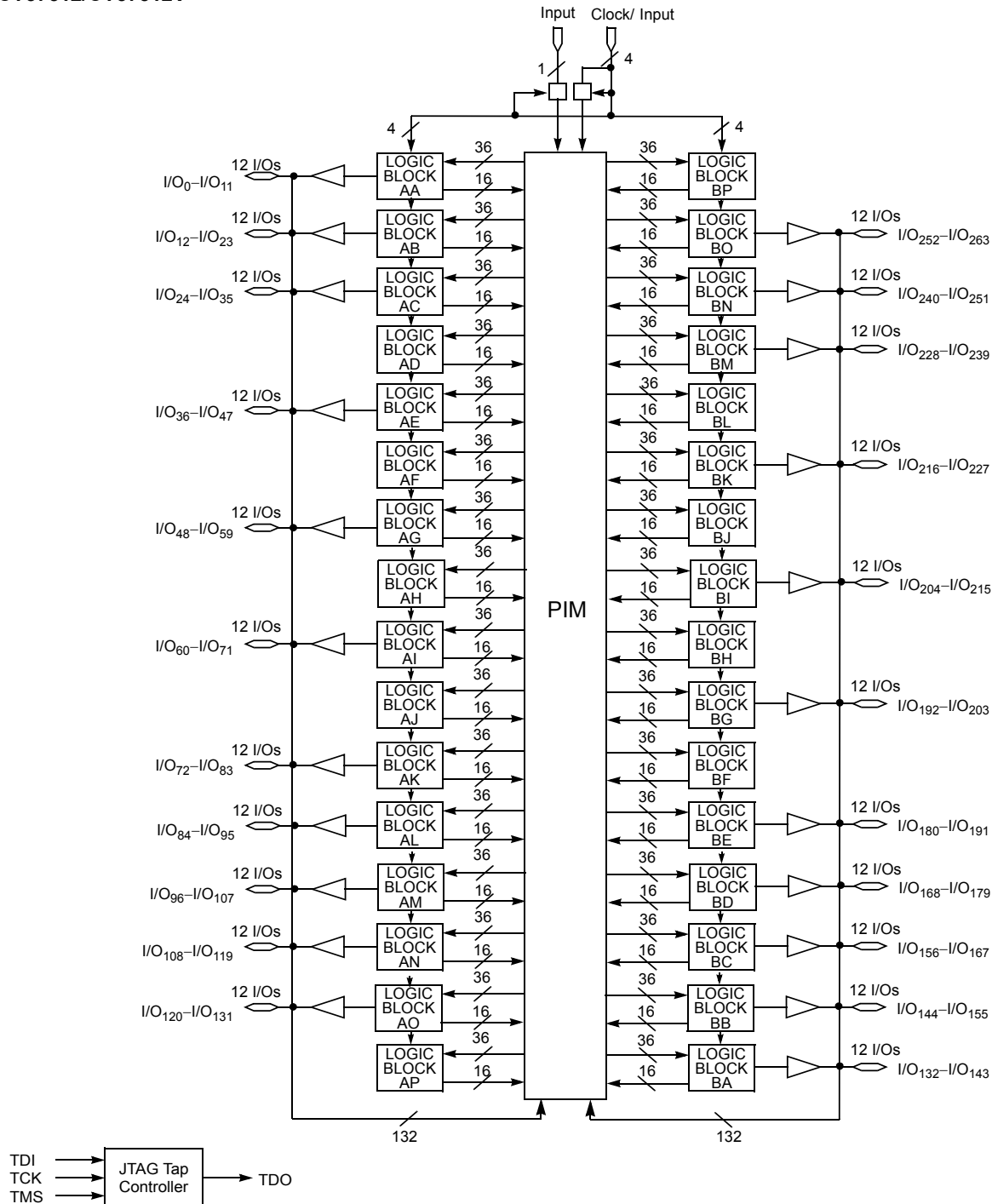
The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

Logic Block Diagrams (continued)

CY37512/CY37512V



5.0V Device Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Voltage Applied to Outputs

in High-Z State -0.5V to +7.0V

DC Input Voltage -0.5V to +7.0V

DC Program Voltage 4.5 to 5.5V

Current into Outputs 16 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range^[2]

Range	Ambient Temperature ^[2]	Junction Temperature	Output Condition	V _{CC}	V _{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	-40°C to +85°C	-40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military ^[3]	-55°C to +125°C	-55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min. I _{OH} = -3.2 mA (Com'I/Ind) ^[4] I _{OH} = -2.0 mA (Mil) ^[4]	2.4 2.4			V
V _{OHZ}	Output HIGH Voltage with Output Disabled ^[5]	V _{CC} = Max. I _{OH} = 0 μA (Com'I) ^[6] I _{OH} = 0 μA (Ind/Mil) ^[6] I _{OH} = -100 μA (Com'I) ^[6] I _{OH} = -150 μA (Ind/Mil) ^[6]			4.2 4.5 3.6 3.6	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. I _{OL} = 16 mA (Com'I/Ind) ^[4] I _{OL} = 12 mA (Mil) ^[4]			0.5 0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs ^[7]	2.0		V _{CCmax}	V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs ^[7]	-0.5		0.8	V
I _{IX}	Input Load Current	V _I = GND OR V _{CC} , Bus-Hold Disabled	-10		10	μA
I _{OZ}	Output Leakage Current	V _O = GND or V _{CC} , Output Disabled, Bus-Hold Disabled	-50		50	μA
I _{OS}	Output Short Circuit Current ^[5, 8]	V _{CC} = Max., V _{OUT} = 0.5V	-30		-160	mA
I _{BHL}	Input Bus-Hold LOW Sustaining Current	V _{CC} = Min., V _{IL} = 0.8V	+75			μA
I _{BHH}	Input Bus-Hold HIGH Sustaining Current	V _{CC} = Min., V _{IH} = 2.0V	-75			μA
I _{BHLO}	Input Bus-Hold LOW Overdrive Current	V _{CC} = Max.			+500	μA
I _{BHHO}	Input Bus-Hold HIGH Overdrive Current	V _{CC} = Max.			-500	μA

Notes:

- Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled "An Introduction to In System Reprogramming with the Ultra37000."
- T_A is the "Instant On" case temperature.
- I_{OH} = -2 mA, I_{OL} = 2 mA for TDO.
- Tested initially and after any design or process changes that may affect these parameters.
- When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Inductance^[5]

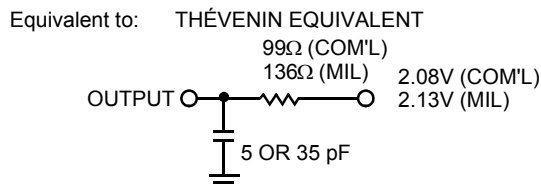
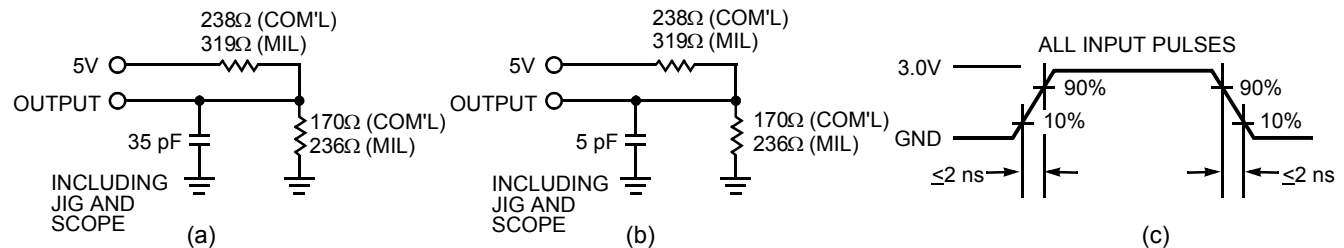
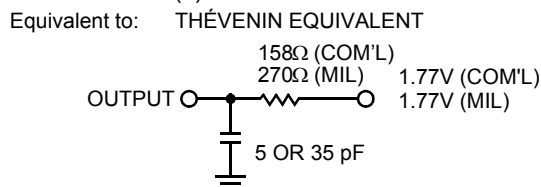
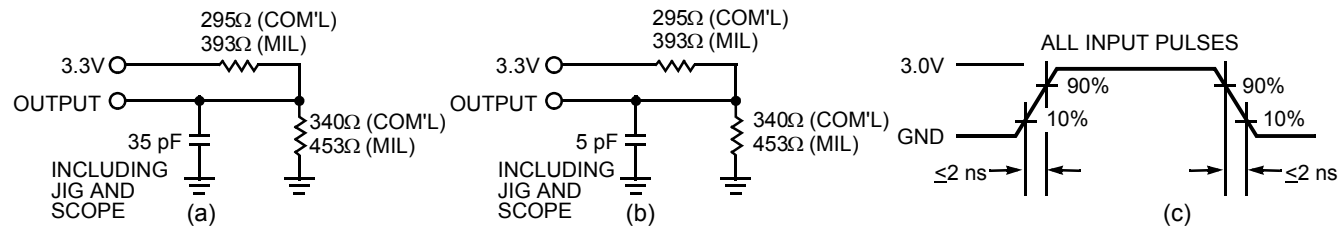
Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	$V_{IN} = 3.3V$ at $f = 1\text{ MHz}$	2	5	2	8	5	8	9	11	nH

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{IN} = 3.3V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	8	pF
C_{CLK}	Clock Signal Capacitance	$V_{IN} = 3.3V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	12	pF
C_{DP}	Dual Functional Pins ^[9]	$V_{IN} = 3.3V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	16	pF

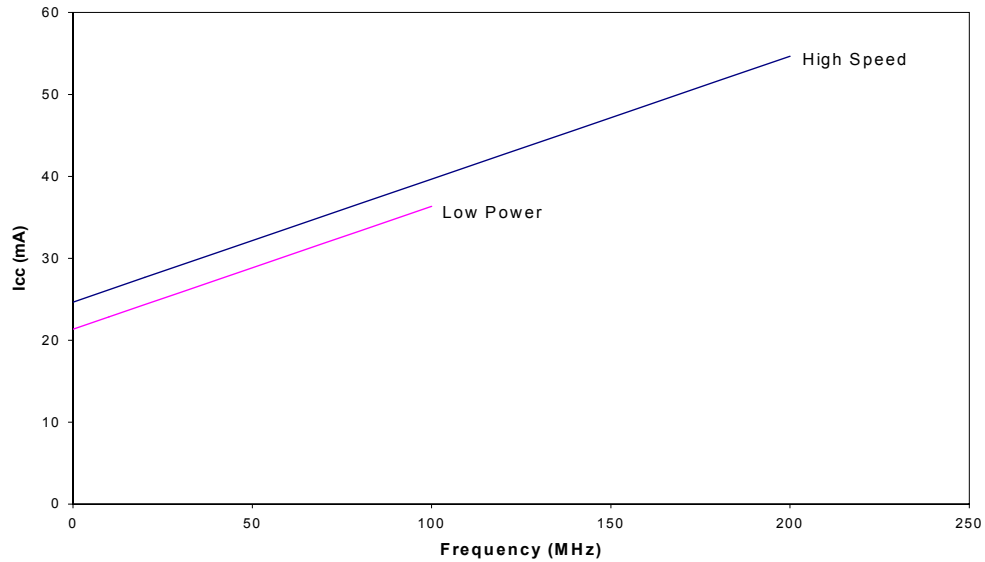
Endurance Characteristics^[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions ^[2]	1,000	10,000	Cycles

AC Characteristics
5.0V AC Test Loads and Waveforms

3.3V AC Test Loads and Waveforms


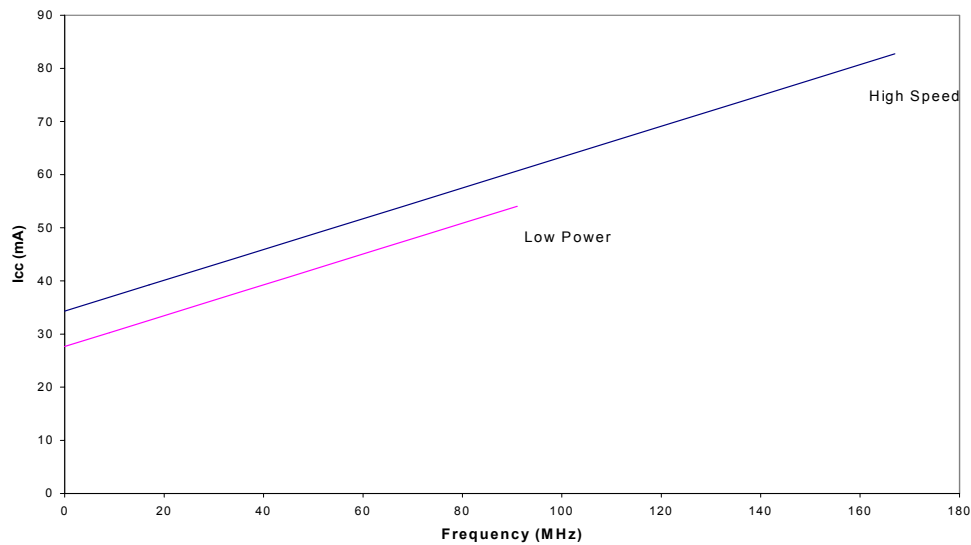
Power Consumption

Typical 5.0V Power Consumption CY37032

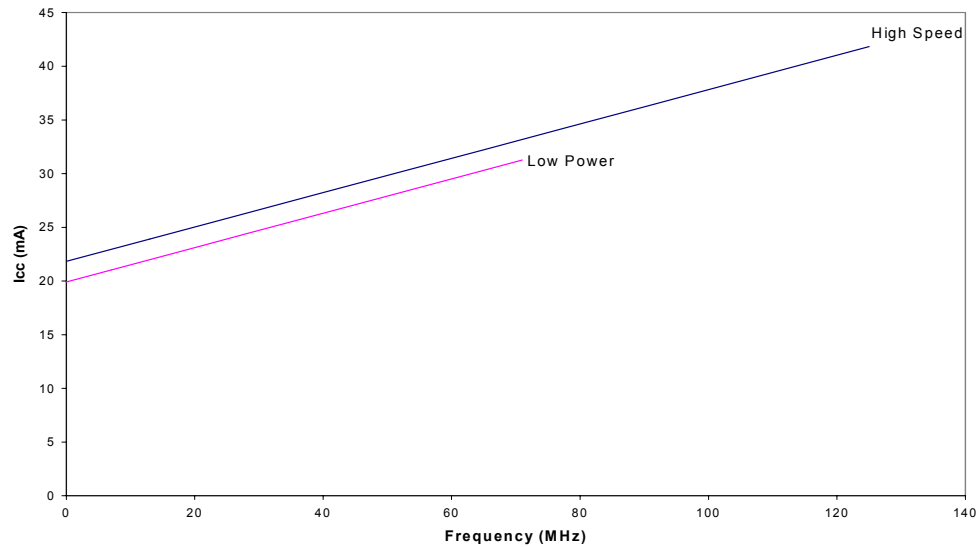


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

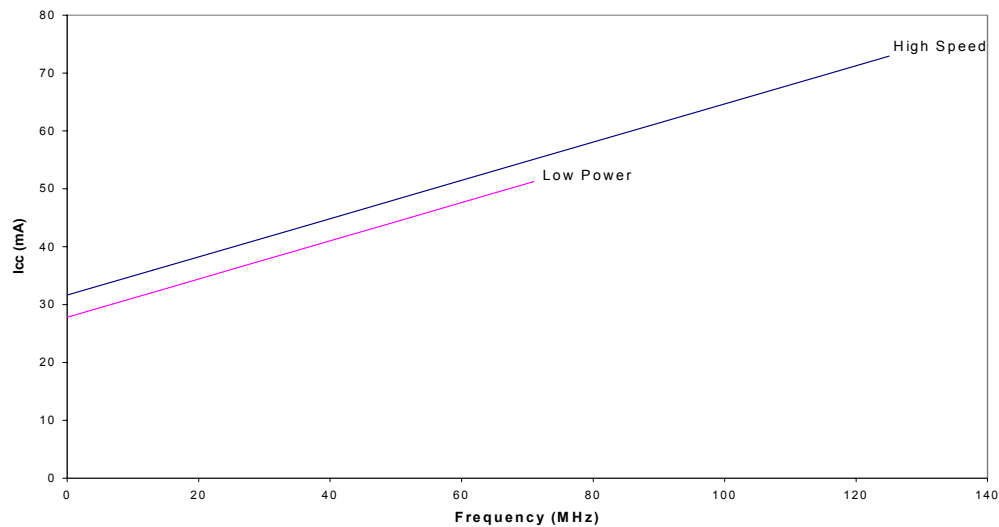
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 3.3V Power Consumption (continued)
CY37064V


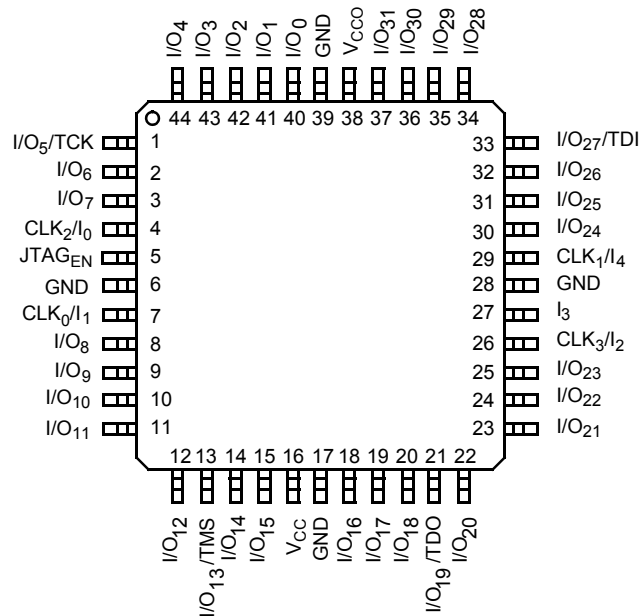
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

CY37128V


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

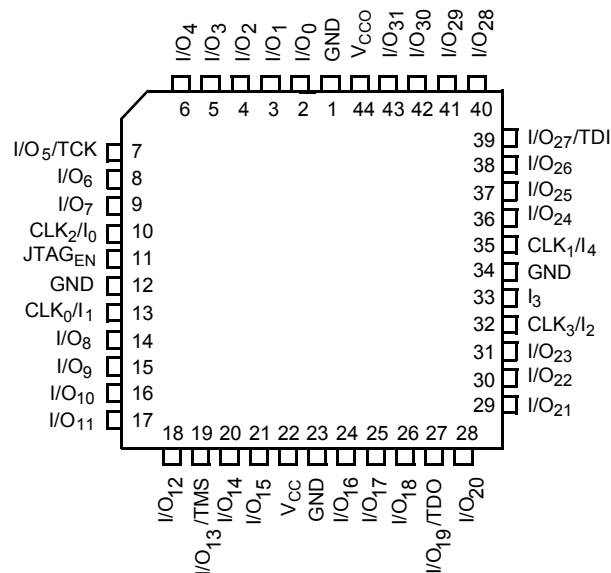
44-pin TQFP (A44)

Top View



44-pin PLCC (J67) / CLCC (Y67)

Top View

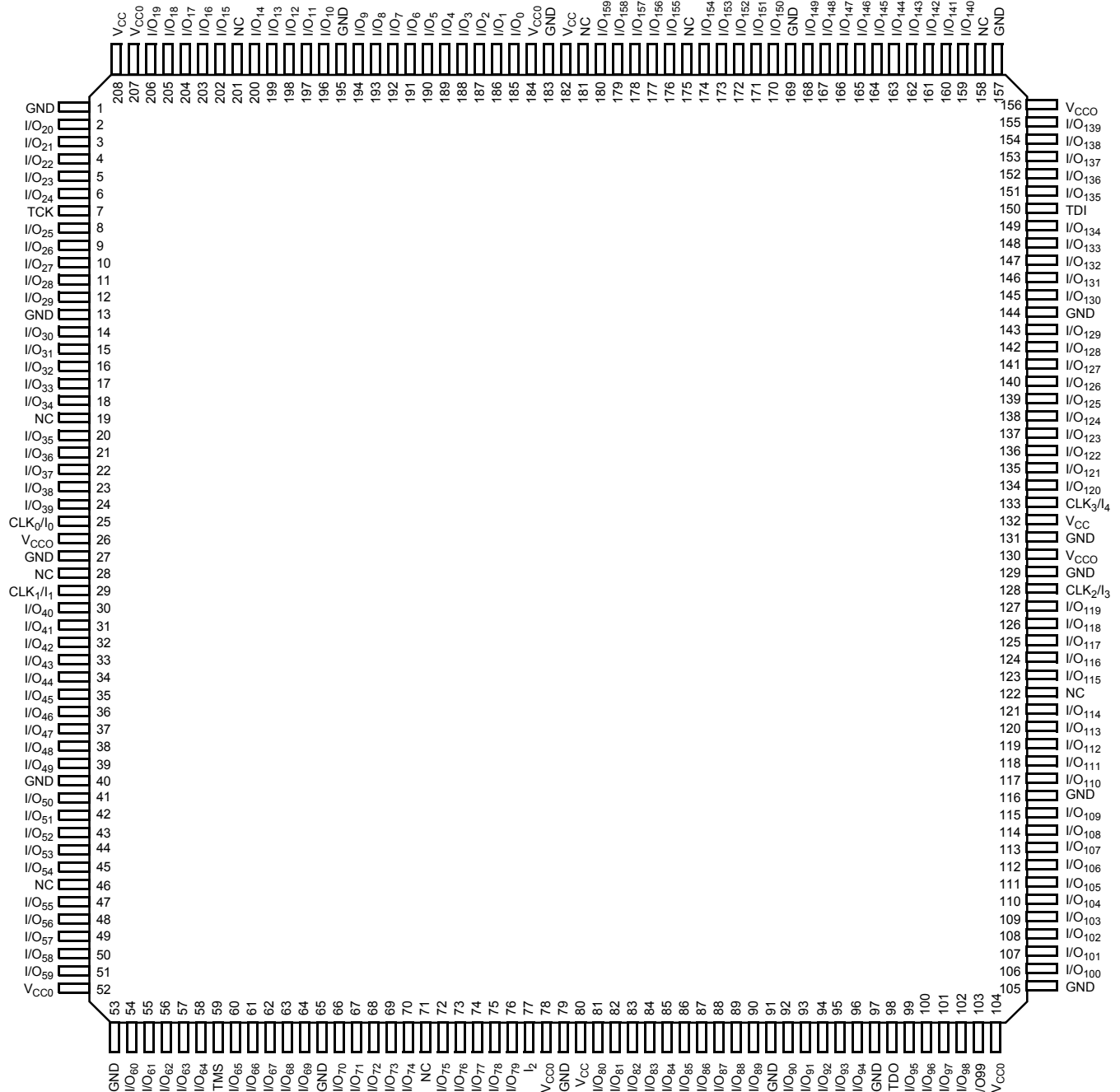


Pin Configurations^[20] (continued)
100-ball Fine-Pitch BGA (BB100) for CY37064V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	NC	I/O ₇	I/O ₅	I/O ₂	I/O ₆₂	I/O ₆₀	I/O ₅₈	I/O ₅₇	I/O ₅₆
B	I/O ₉	I/O ₈	I/O ₆	I/O ₄	I/O ₁	I/O ₆₃	V _{CC}	I/O ₅₉	I/O ₅₅	NC
C	I/O ₁₀	TCK	V _{CC}	I/O ₃	NC	NC	I/O ₆₁	V _{CC}	TDI	I/O ₅₄
D	I/O ₁₁	NC	I/O ₁₂	I/O ₁₃	I/O ₀	NC	I/O ₅₁	I/O ₅₂	CLK ₃ / I ₄	I/O ₅₃
E	I/O ₁₄	CLK ₀ / I ₀	I/O ₁₅	NC	GND	GND	I/O ₄₈	I/O ₄₉	CLK ₂ / I ₃	I/O ₅₀
F	I/O ₁₇	NC	NC	I/O ₁₆	GND	GND	NC	NC	I ₂	I/O ₄₇
G	I/O ₂₂	CLK ₁ / I ₁	I/O ₂₁	I/O ₁₉	I/O ₁₈	I/O ₄₆	I/O ₄₅	I/O ₄₄	NC	I/O ₄₃
H	I/O ₂₃	TMS	V _{CC}	I/O ₂₀	NC	I/O ₃₂	I/O ₄₂	V _{CC}	TDO	I/O ₄₁
J	NC	I/O ₂₆	I/O ₂₈	NC	I/O ₃₁	I/O ₃₃	I/O ₃₅	I/O ₃₇	I/O ₃₉	I/O ₄₀
K	I/O ₂₄	I/O ₂₅	I/O ₂₇	I/O ₂₉	I/O ₃₀	I/O ₃₄	I/O ₃₆	I/O ₃₈	NC	NC

100-ball Fine-Pitch BGA (BB100) for CY37128V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	I/O ₉	I/O ₈	I/O ₆	I/O ₃	I/O ₇₆	I/O ₇₄	I/O ₇₂	I/O ₇₁	I/O ₇₀
B	I/O ₁₁	I/O ₁₀	I/O ₇	I/O ₅	I/O ₂	I/O ₇₇	V _{CC}	I/O ₇₃	I/O ₆₈	I/O ₆₉
C	I/O ₁₂	I/O ₁₃ TCK	V _{CC}	I/O ₄	I/O ₁	I/O ₇₈	I/O ₇₅	V _{CC}	I/O ₆₇ TDI	I/O ₆₆
D	I/O ₁₄	NC	I/O ₁₅	I/O ₁₆	I/O ₀	I/O ₇₉	I/O ₆₃	I/O ₆₄	CLK ₃ / I ₄	I/O ₆₅
E	I/O ₁₇	CLK ₀ / I ₀	I/O ₁₈	I/O ₁₉	GND	GND	I/O ₆₀	I/O ₆₁	CLK ₂ / I ₃	I/O ₆₂
F	I/O ₂₂	JTAG EN	I/O ₂₁	I/O ₂₀	GND	GND	I/O ₅₉	I/O ₅₈	I ₂	I/O ₅₇
G	I/O ₂₇	CLK ₁ / I ₁	I/O ₂₆	I/O ₂₄	I/O ₂₃	I/O ₅₆	I/O ₅₅	I/O ₅₄	NC	I/O ₅₃
H	I/O ₂₈	I/O ₃₃ TMS	V _{CC}	I/O ₂₅	I/O ₃₉	I/O ₄₀	I/O ₅₂	V _{CC}	I/O ₄₇ TDO	I/O ₅₁
J	I/O ₂₉	I/O ₃₂	I/O ₃₅	V _{CC}	I/O ₃₈	I/O ₄₁	I/O ₄₃	I/O ₄₅	I/O ₄₈	I/O ₅₀
K	I/O ₃₀	I/O ₃₁	I/O ₃₄	I/O ₃₆	I/O ₃₇	I/O ₄₂	I/O ₄₄	I/O ₄₆	I/O ₄₉	NC

Pin Configurations^[20] (continued)
**208-Lead PQFP (N208) / CQFP (U208)
Top View**


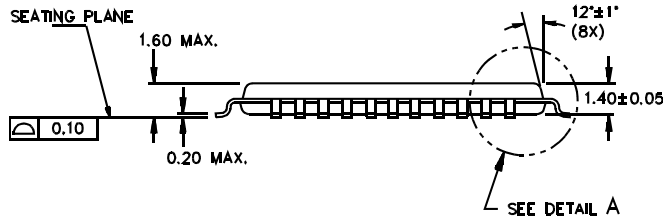
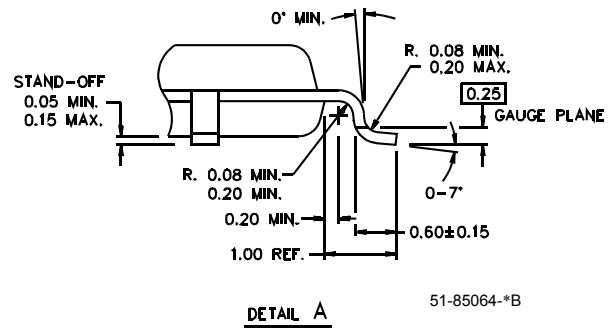
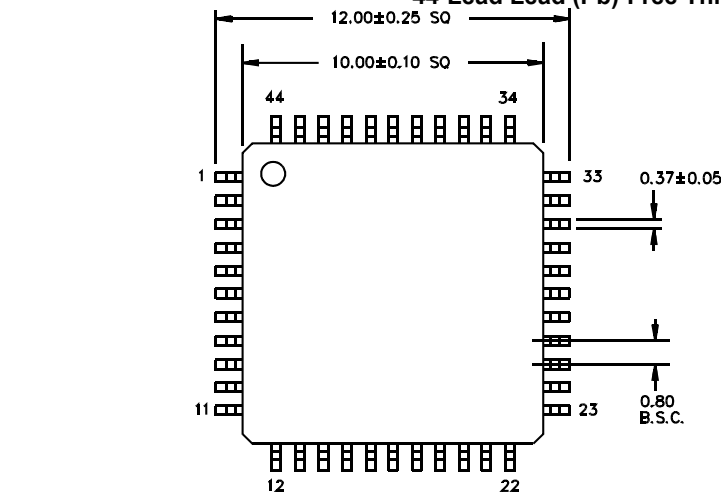
5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
128	167	CY37128P84-167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-167JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-167AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-167AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-167AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-167AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	125	CY37128P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-125JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P84-125JXI	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-125AI	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		5962-9952102QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
	100	CY37128P84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-100JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-100AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-100AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-100AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128P84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-100AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-100AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-100AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952101QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	154	CY37192P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-154AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	125	CY37192P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37192P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	83	CY37192P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37192P160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	

Package Diagrams

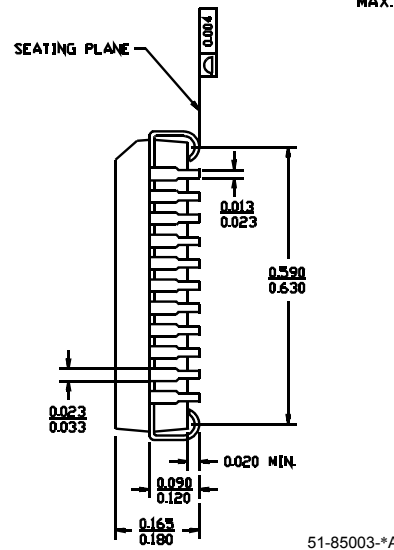
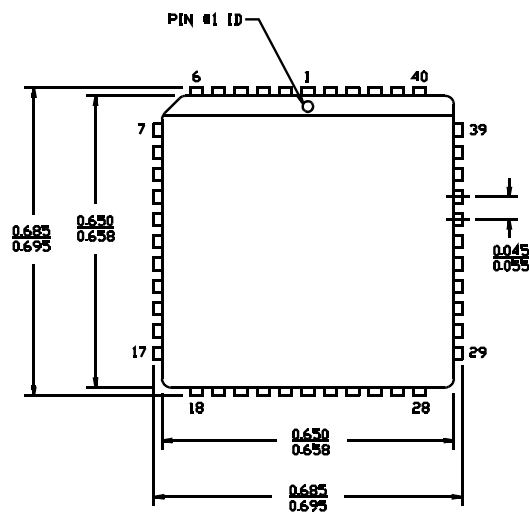
44-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack A44

DIMENSIONS ARE IN MILLIMETERS



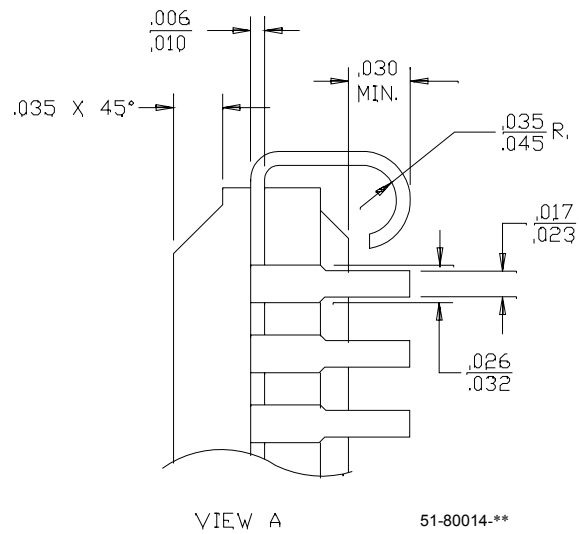
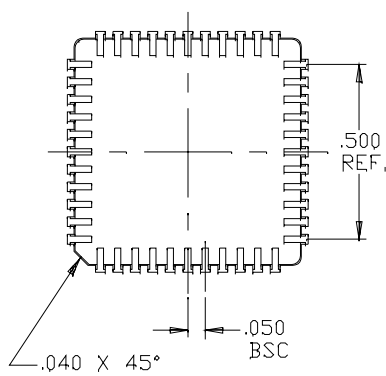
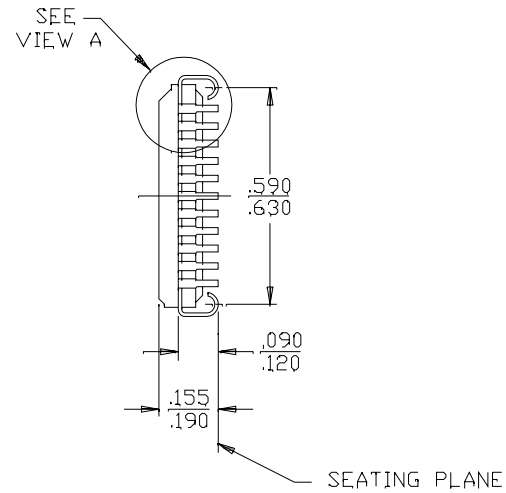
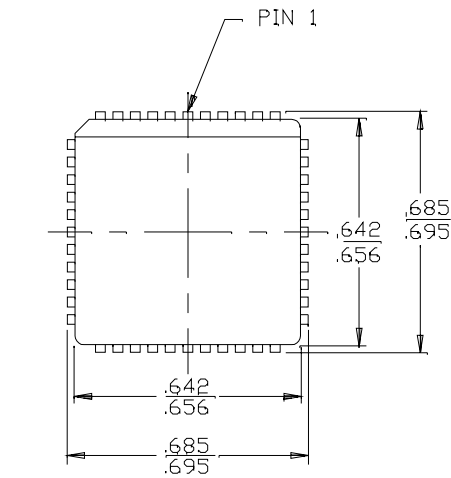
44-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J67

DIMENSIONS IN INCHES MIN. MAX.



Package Diagrams (continued)

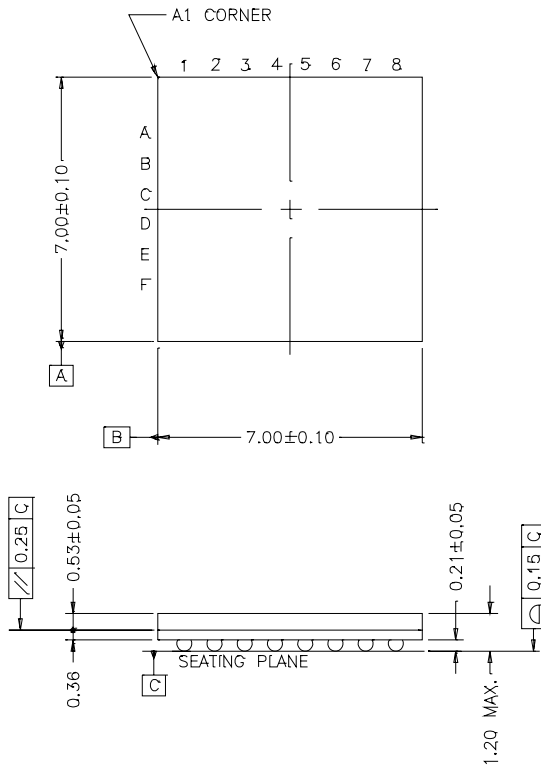
44-Lead Ceramic Leaded Chip Carrier Y67



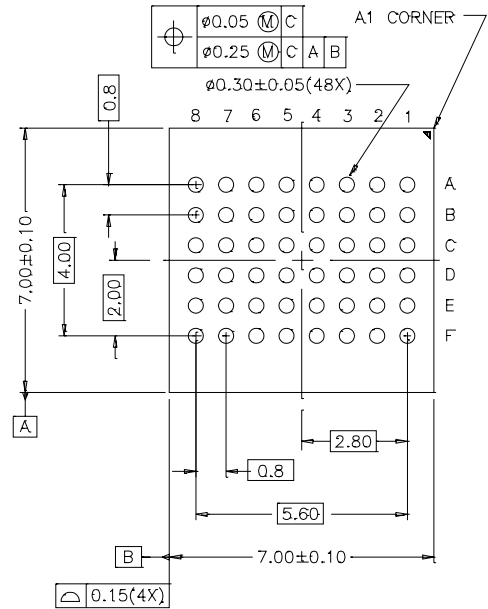
Package Diagrams (continued)

48-Ball (7.0 mm x 7.0 mm x 1.2 mm, 0.80 pitch) Thin BGA BA48D

TOP VIEW



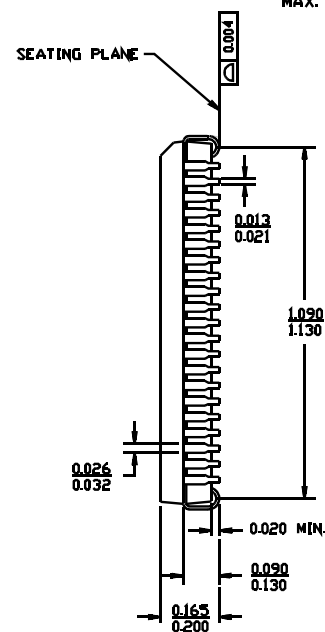
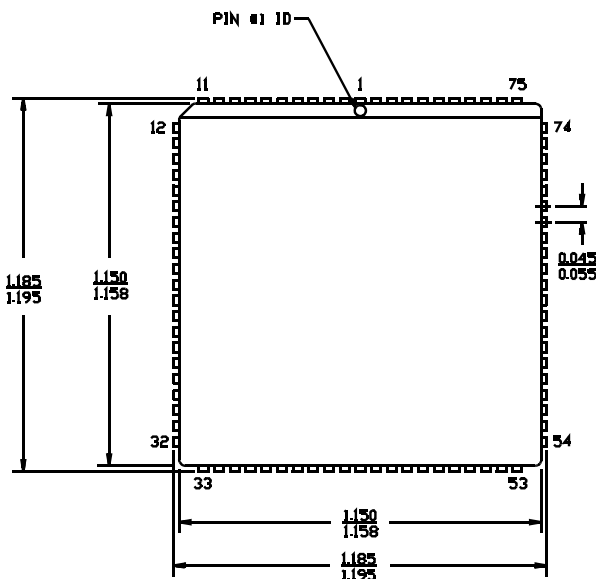
BOTTOM VIEW



51-85109-*C

84-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J83

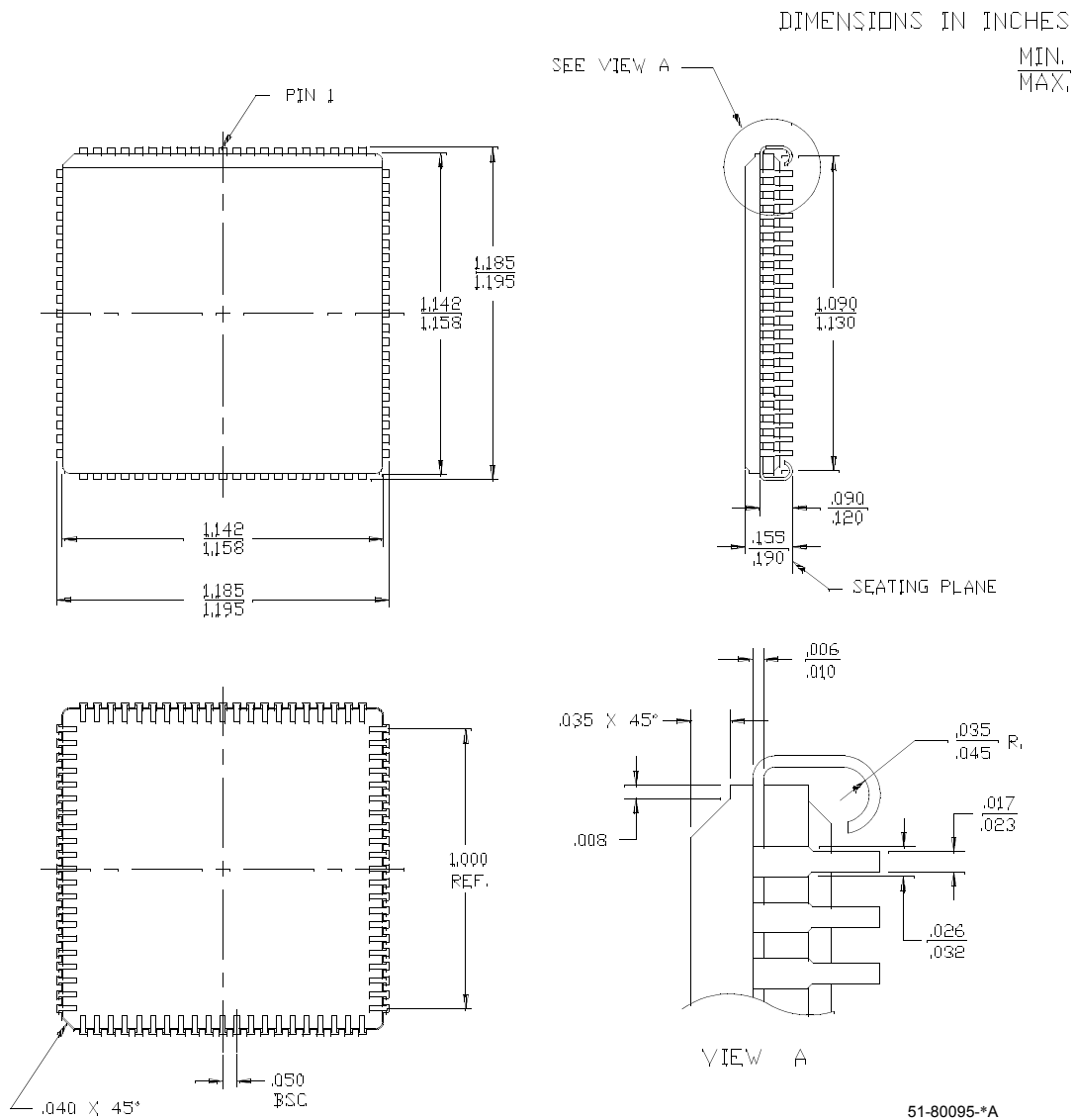
DIMENSIONS IN INCHES MIN. MAX.



51-85006-*A

Package Diagrams (continued)

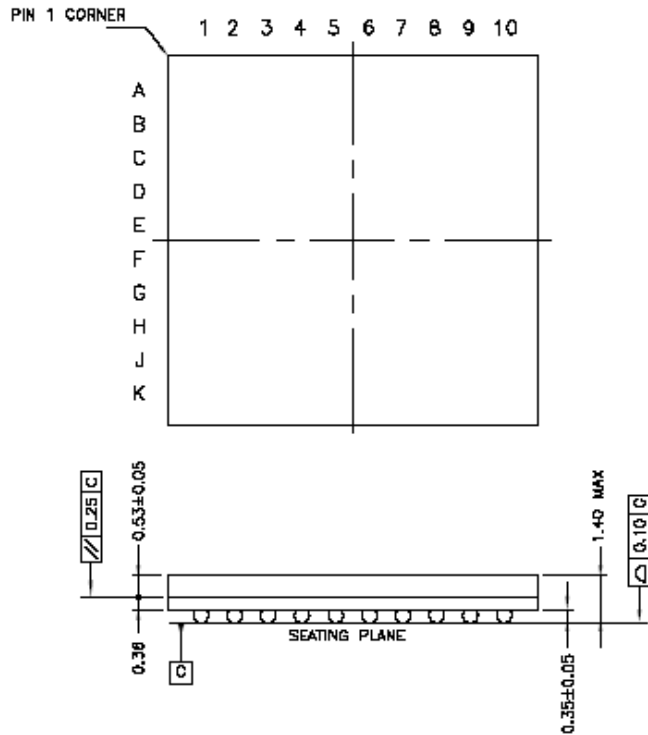
84-Lead Ceramic Leaded Chip Carrier Y84



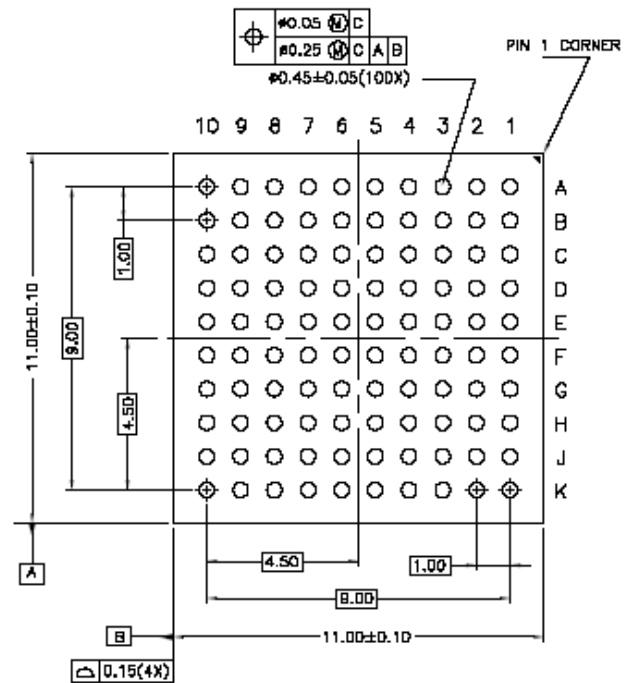
Package Diagrams (continued)

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100

TOP VIEW



BOTTOM VIEW



51-85107-B

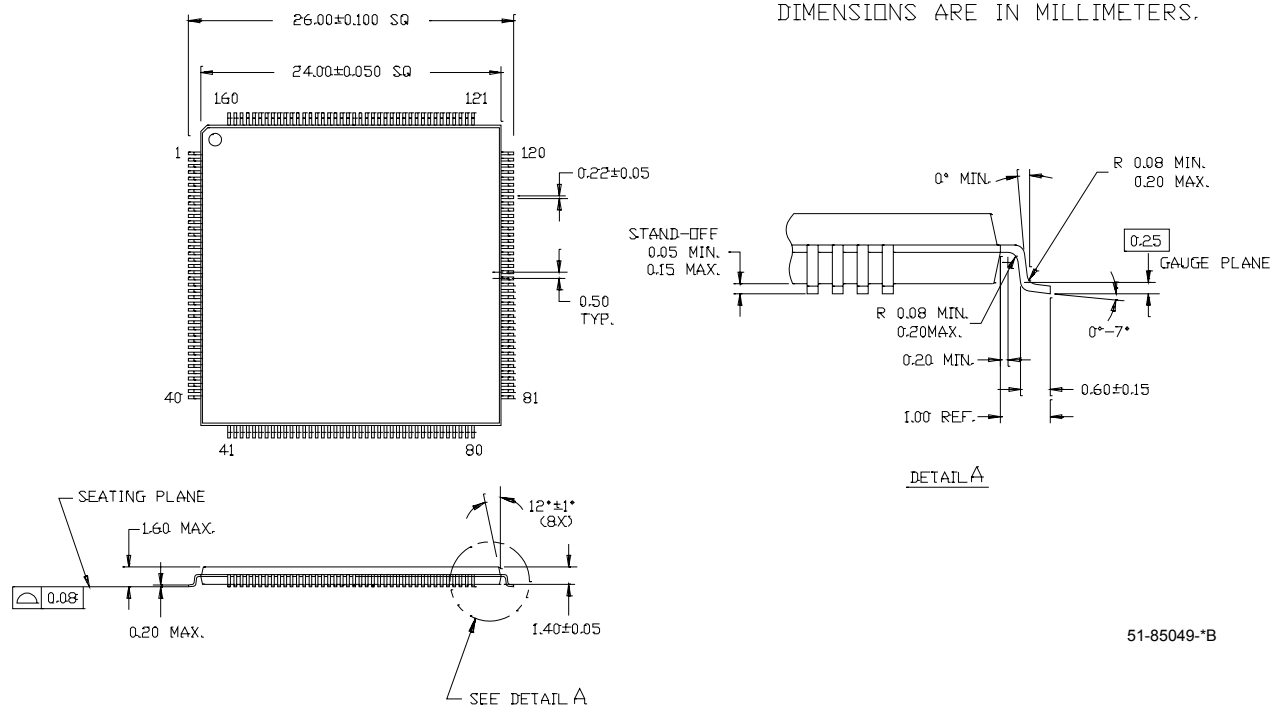


Ultra37000 CPLD Family

Package Diagrams (continued)

160-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (24 x 24 x 1.4 mm) (TQFP) A160

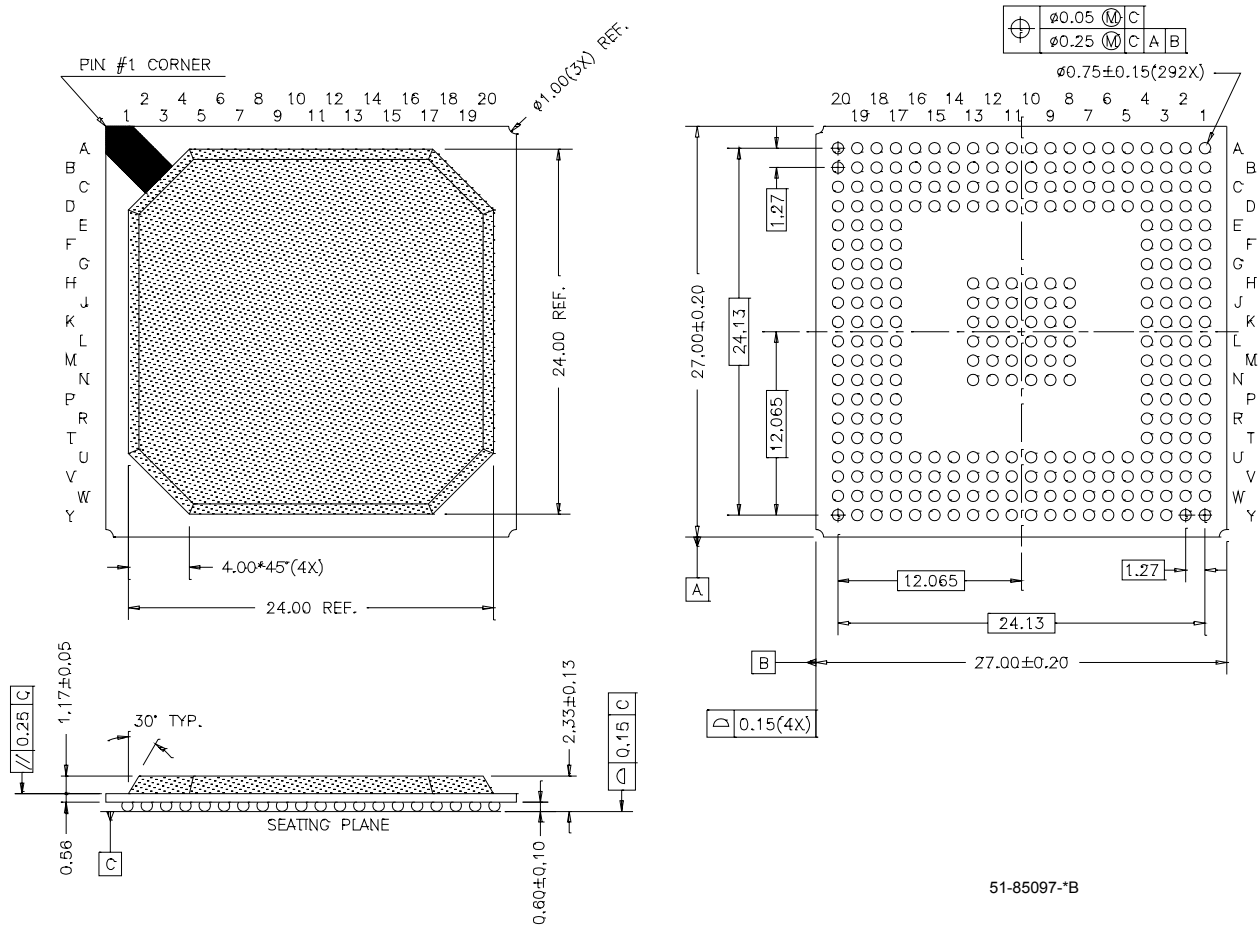
DIMENSIONS ARE IN MILLIMETERS.



51-85049-*B

Package Diagrams (continued)

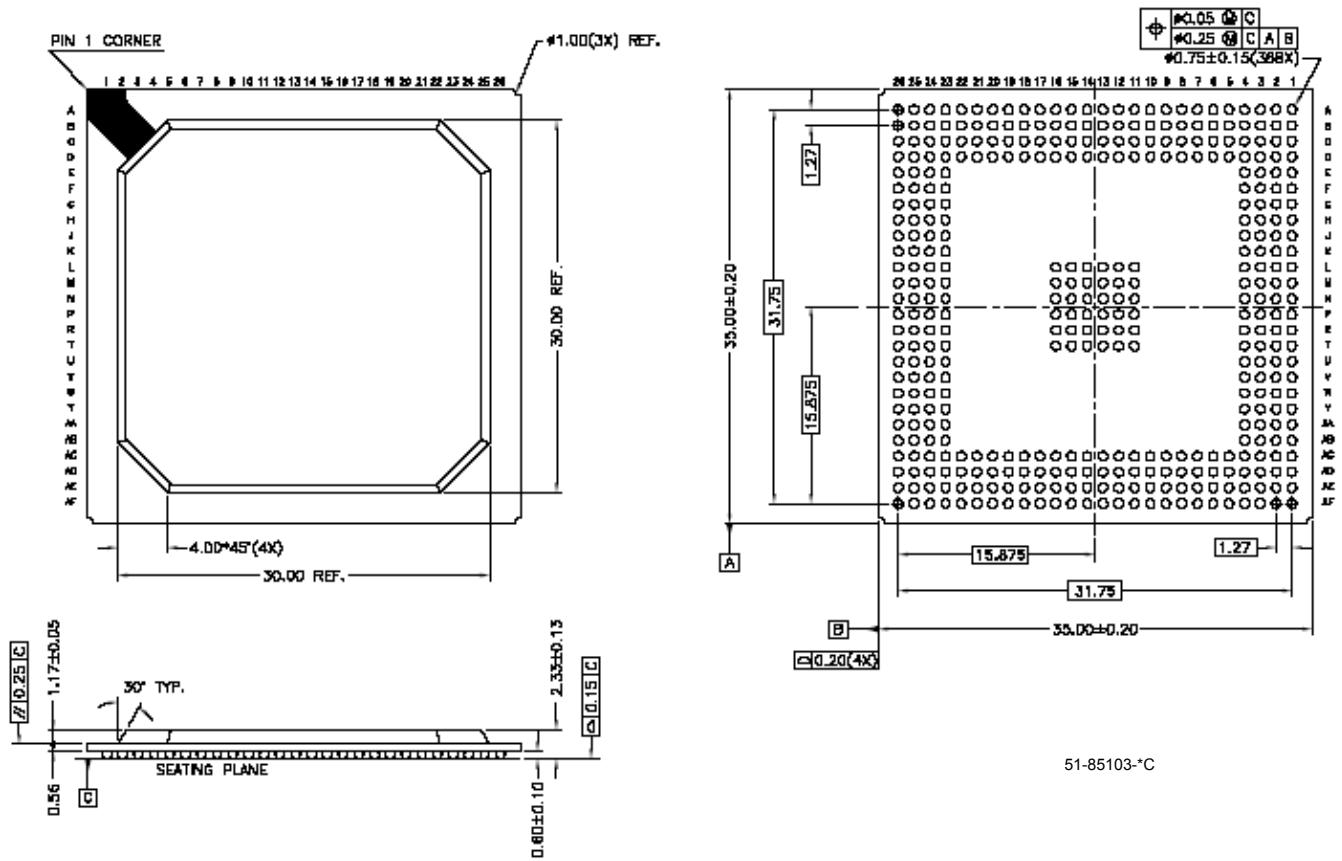
292-Ball Plastic Ball Grid Array PBGA (27 x 27 x 2.33 mm) BG292



51-85097-*B

Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388



51-85103-°C

Addendum**3.3V Operating Range****(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)**

Range	Ambient Temperature ^[2]	Junction Temperature	V _{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.16V