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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	69
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37128p100-125axc

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V					X		X	
CY37192V						X		X
CY37256V						X		X
CY37384V							X	X
CY37512V							X	X

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead CLCC	48-Lead FBGA	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	256-Lead FBGA	388-Lead PBGA	400-Lead FBGA
CY37032V	37		37											
CY37064V	37	37	37		69	69								
CY37128V				69	69	85	133							
CY37192V							125							
CY37256V							133	133	165		197	197		
CY37384V									165		197			
CY37512V									165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The PIM consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*[®] and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

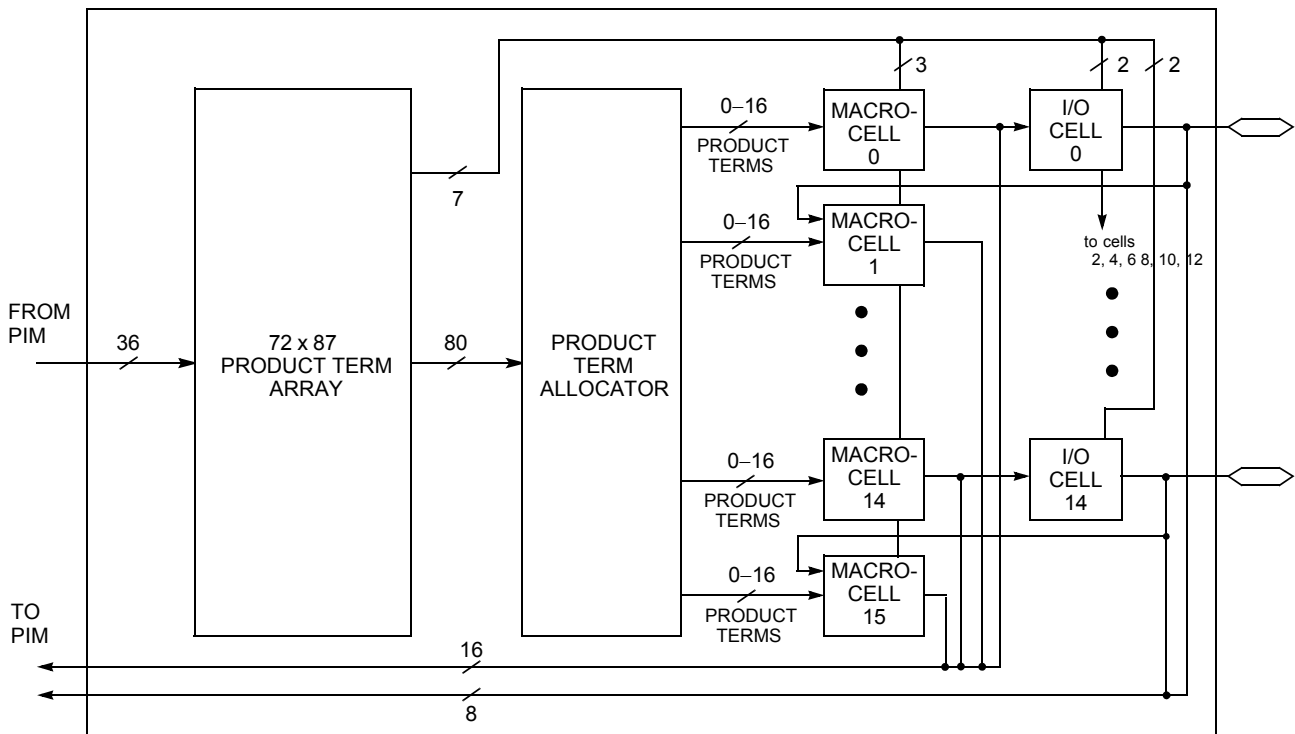


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a

variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

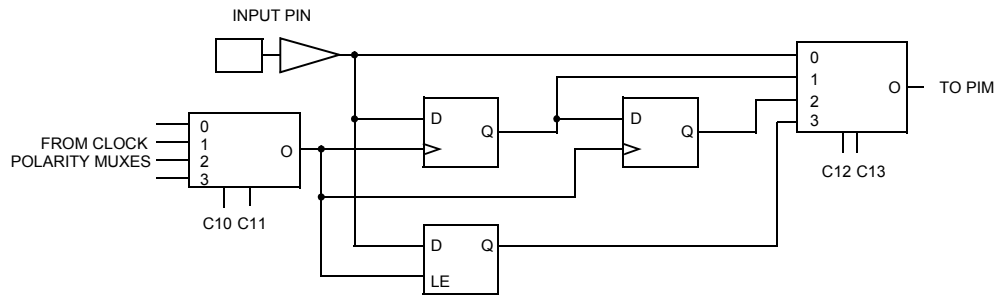
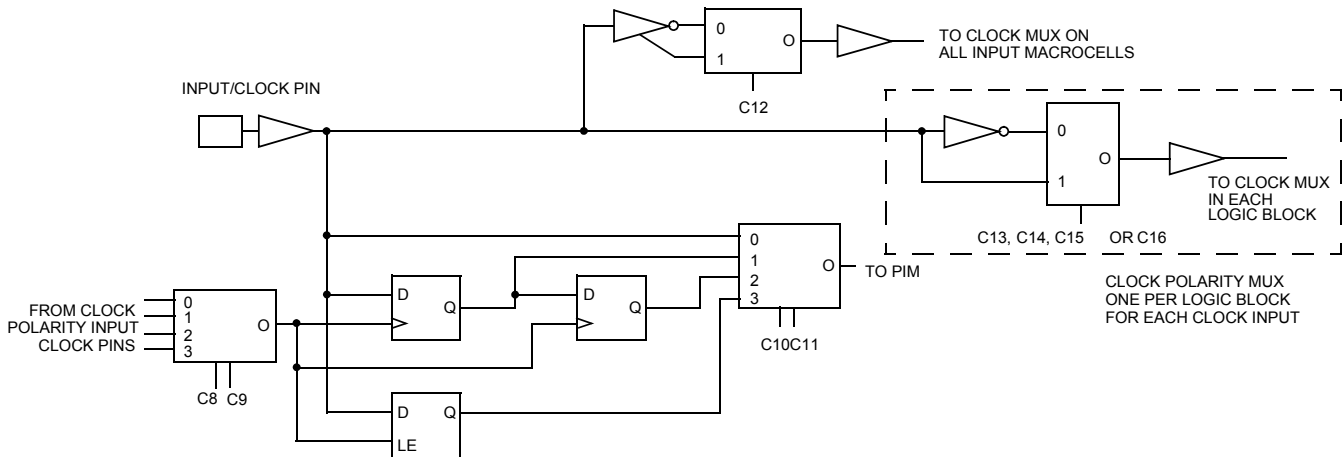
Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.


Figure 3. Input Macrocell

Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

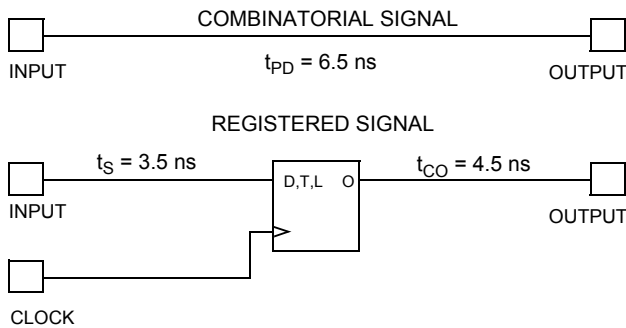


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in Figure 6.

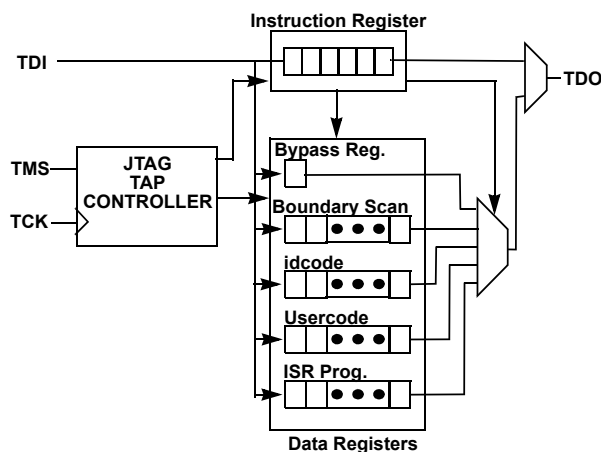


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing

resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the Warp for PC, Warp for UNIX, Warp Professional and Warp Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although Warp is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.



Ultra37000 CPLD Family

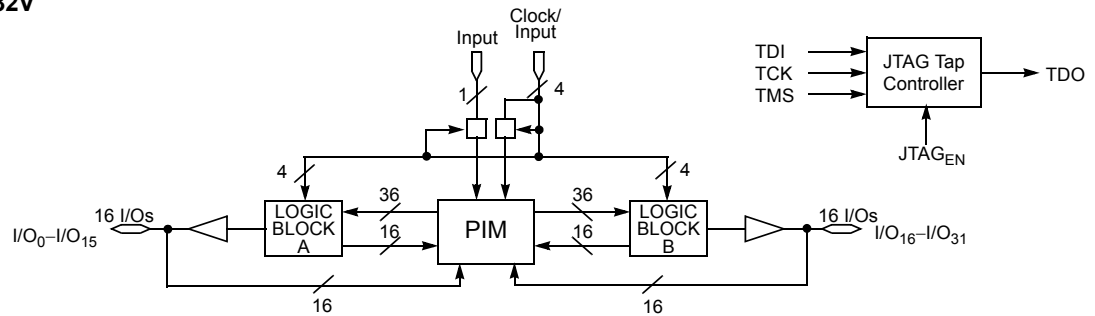
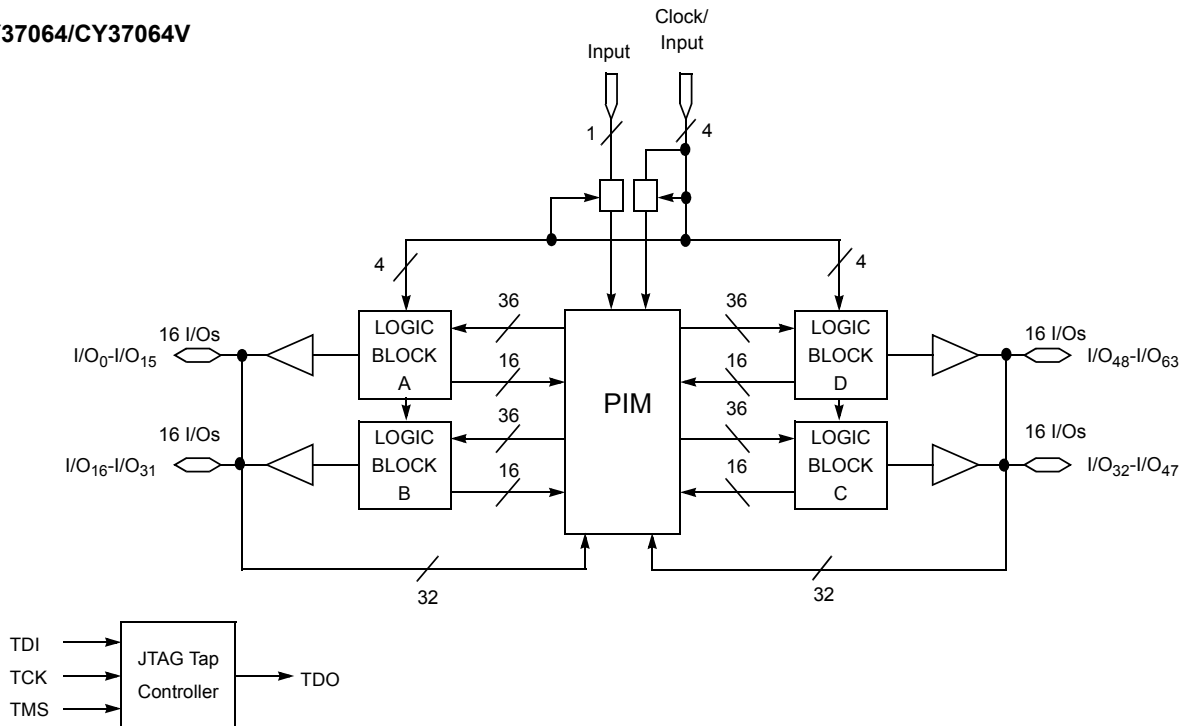
The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

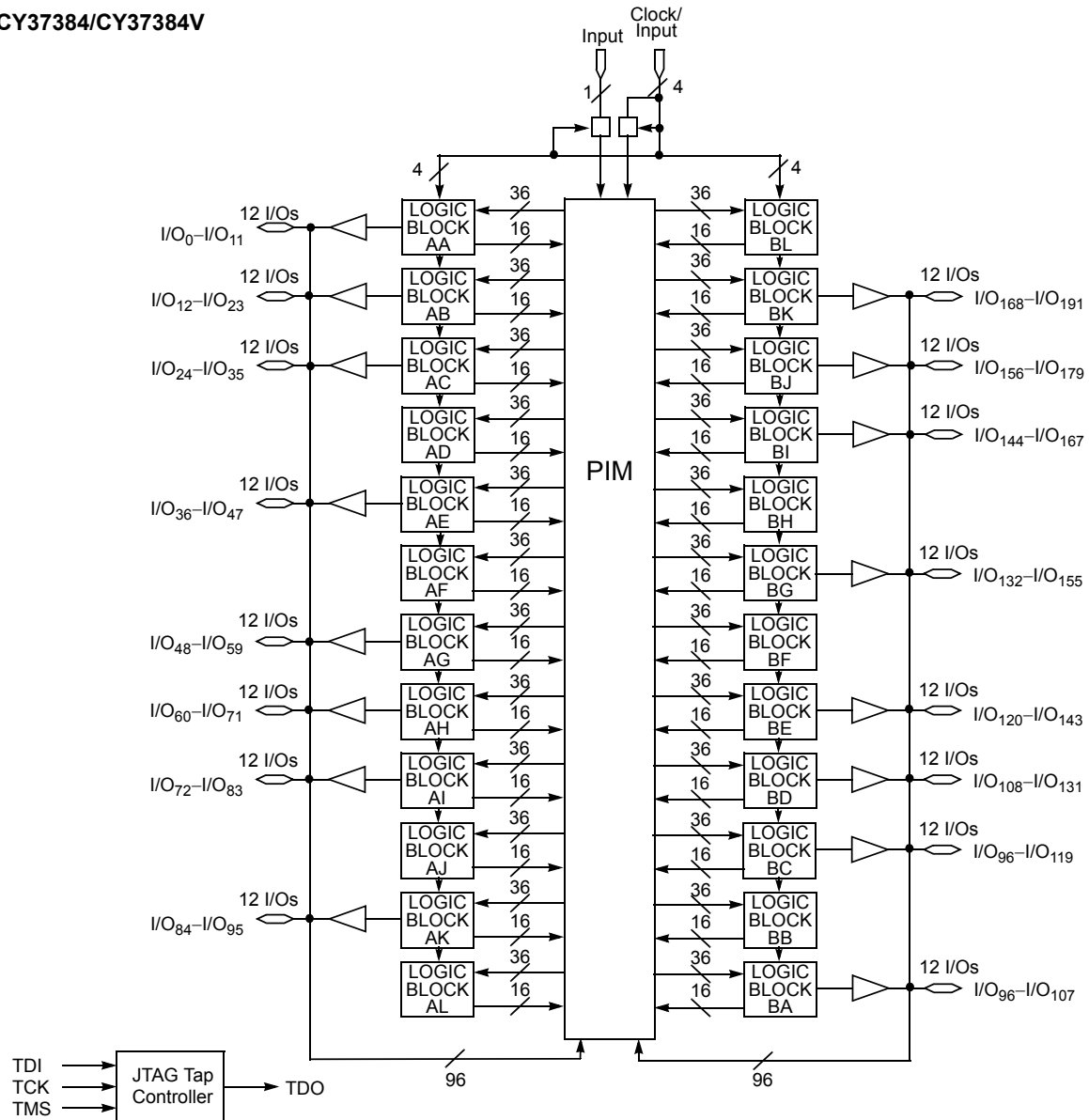
Third-Party Programmers

As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams
CY37032/CY37032V

CY37064/CY37064V


Logic Block Diagrams (continued)

CY37384/CY37384V



Switching Characteristics Over the Operating Range ^[12]

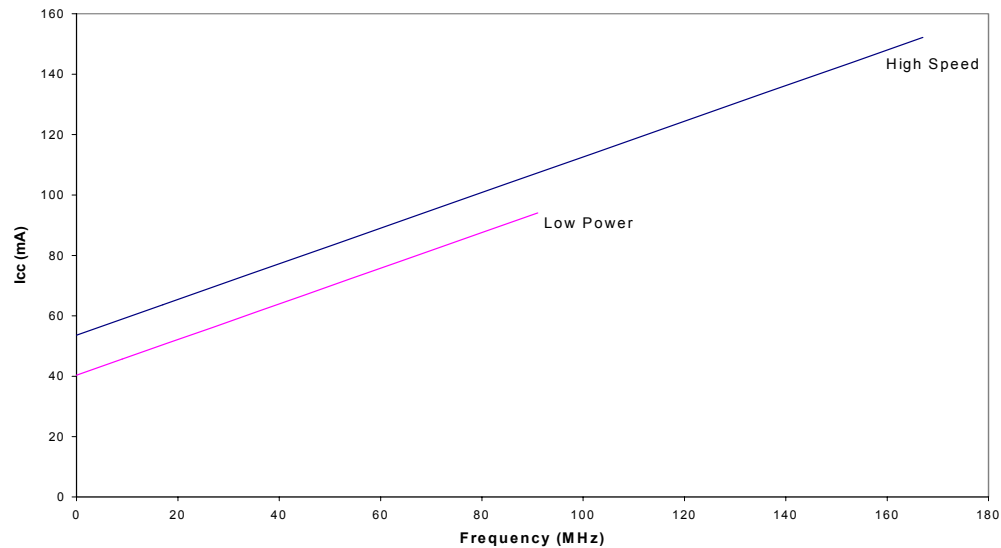
Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t _{PD} ^[13, 14, 15]		6		6.5		7.5		8.5		10		12		15		20	ns
t _{PDL} ^[13, 14, 15]		11		12.5		14.5		16		16.5		17		19		22	ns
t _{PDLL} ^[13, 14, 15]		12		13.5		15.5		17		17.5		18		20		24	ns
t _{EA} ^[13, 14, 15]		8		8.5		11		13		14		16		19		24	ns
t _{ER} ^[11, 13]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t _{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t _{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t _{IS}	2		2		2		2		2		2.5		3		4		ns
t _{IH}	2		2		2		2		2		2.5		3		4		ns
t _{ICO} ^[13, 14, 15]		11		11		11		12.5		12.5		16		19		24	ns
t _{ICOL} ^[13, 14, 15]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t _{CO} ^[14, 15]		4		4		4.5		6		6.5 ^[16]		6.5 ^[17]		8 ^[18]		10	ns
t _S ^[13]	4		4		5		5		5.5 ^[16]		6 ^[17]		8 ^[18]		10		ns
t _H	0		0		0		0		0		0		0		0		ns
t _{CO2} ^[13, 14, 15]		9.5		10		11		12		14		16		19		24	ns
t _{SCS} ^[13]	5		6		6.5		7		8 ^[16]		10		12		15		ns
t _{SL} ^[13]	7.5		7.5		8.5		9		10		12		15		15		ns
t _{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t _{COPT} ^[13, 14, 15]		7		10		10		13		13		13		15		20	ns
t _{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t _{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t _{ISPT} ^[13]	0		0		0		0		0		0		0		0		ns
t _{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t _{CO2PT} ^[13, 14, 15]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t _{ICS} ^[13]	5		6		6		7		8 ^[16]		10		12		15		ns
Operating Frequency Parameters																	
f _{MAX1}	200		167		154		143		125 ^[16]		100		83		66		MHz
f _{MAX2}	200		200		200		167		154		153 ^[17]		125 ^[18]		100		MHz
f _{MAX3}	125		125		105		91		83		80 ^[17]		62.5		50		MHz
f _{MAX4}	167		167		154		125		118		100		83		66		MHz
Reset/Preset Parameters																	
t _{RW}	8		8		8		8		10		12		15		20		ns
t _{RR} ^[13]	10		10		10		10		12		14		17		22		ns

Notes:

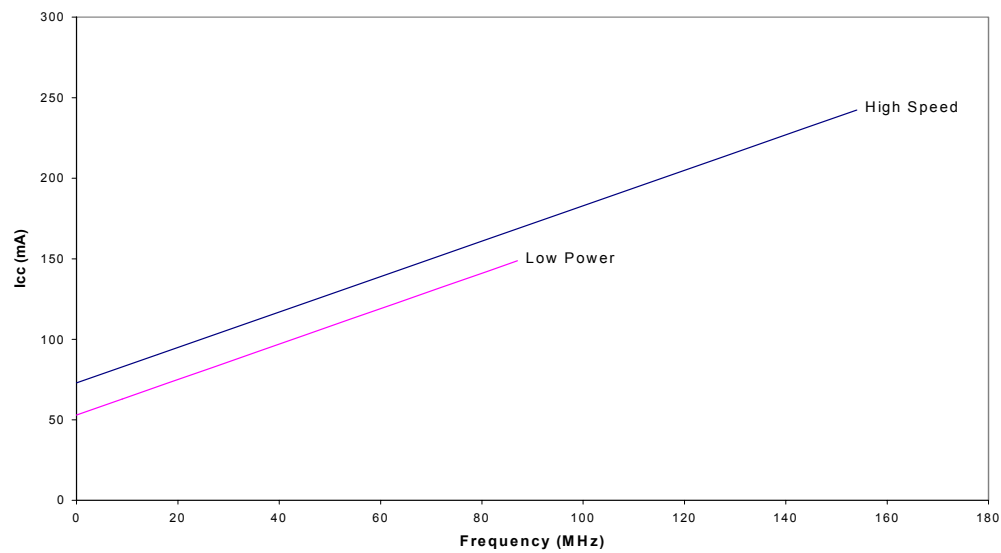
16. The following values correspond to the CY37512 and CY37384 devices: $t_{CO} = 5$ ns, $t_S = 6.5$ ns, $t_{SCS} = 8.5$ ns, $t_{ICS} = 8.5$ ns, $f_{MAX1} = 118$ MHz.

17. The following values correspond to the CY37192V and CY37256V devices: $t_{CO} = 6$ ns, $t_S = 7$ ns, $f_{MAX2} = 143$ MHz, $f_{MAX3} = 77$ MHz, and $f_{MAX4} = 100$ MHz; and for the CY37512 devices: $t_S = 7$ ns.

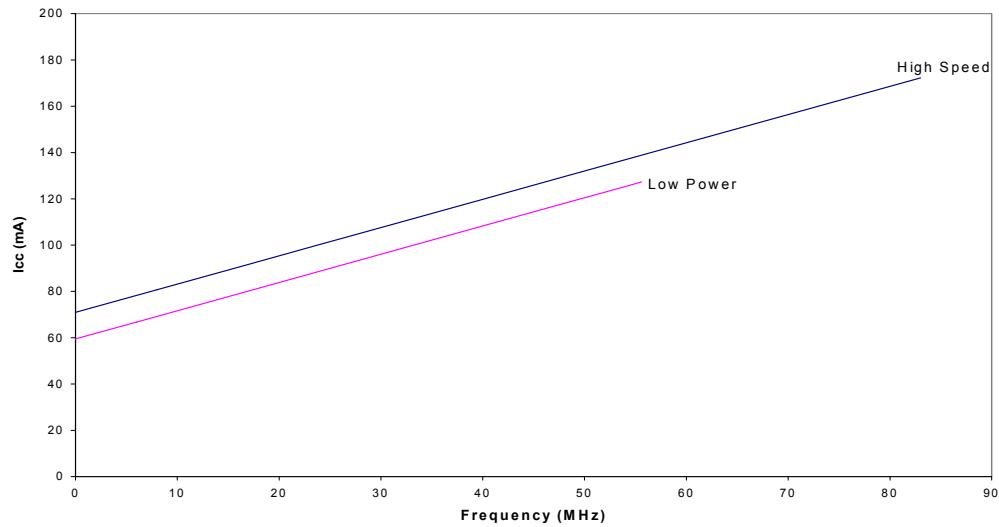
18. The following values correspond to the CY37512V and CY37384V devices: $t_{CO} = 6.5$ ns, $t_S = 9.5$ ns, and $f_{MAX2} = 105$ MHz.

Typical 5.0V Power Consumption (continued)
CY37128


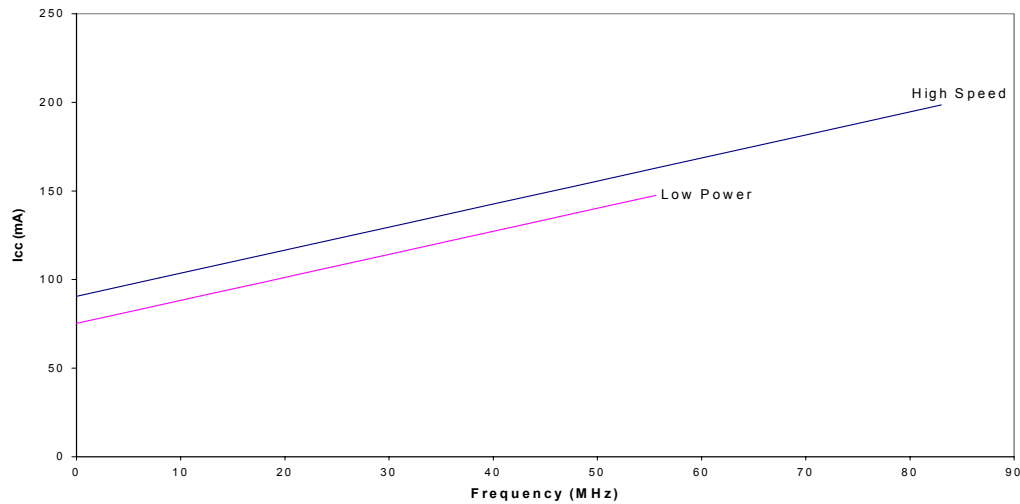
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

CY37192


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Typical 3.3V Power Consumption (continued)
CY37384V


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

CY37512V


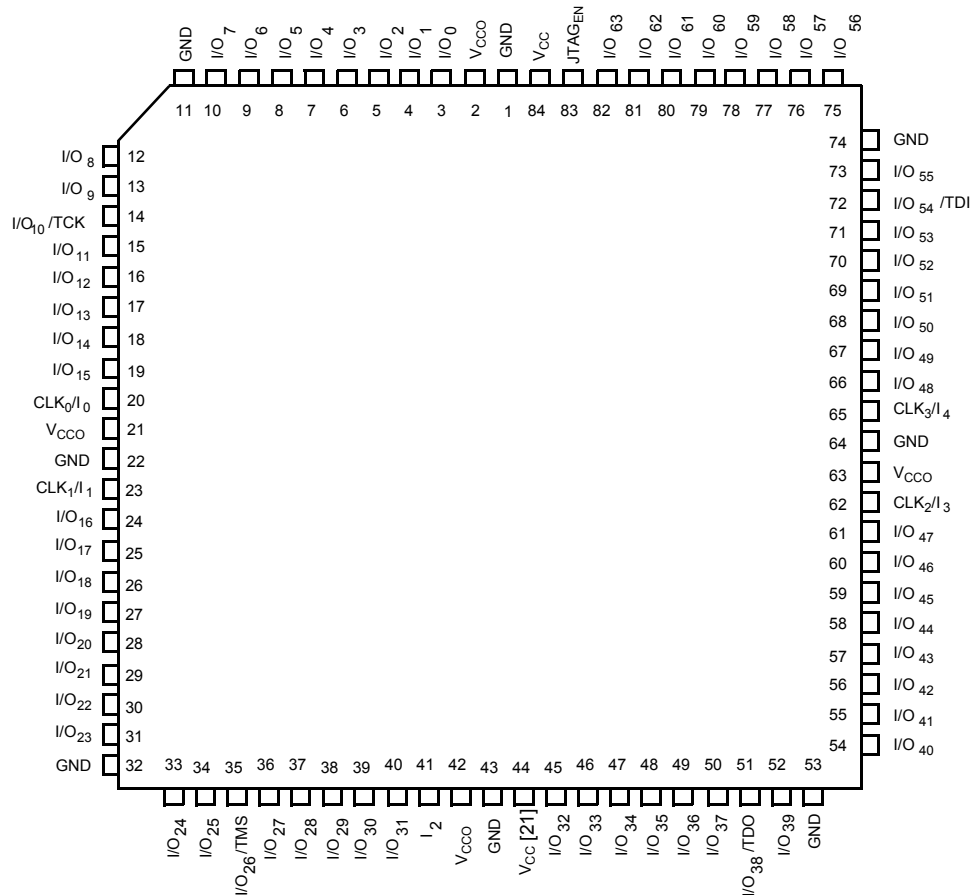
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

Pin Configurations^[20] (continued)
48-ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O ₅ TCK	V _{CC}	I/O ₃	I/O ₁	I/O ₃₁	I/O ₃₀	V _{CC}	I/O ₂₇ TDI
B	V _{CC}	I/O ₄	I/O ₂	I/O ₀	I/O ₂₉	I/O ₂₈	I/O ₂₆	CLK ₁ /I ₄
C	CLK ₂ /I ₀	I/O ₇	I/O ₆	GND	GND	I/O ₂₅	I/O ₂₄	I ₃
D	JTAG _{EN}	I/O ₈	I/O ₉	GND	GND	I/O ₂₂	I/O ₂₃	CLK ₃ /I ₂
E	CLK ₀ /I ₁	I/O ₁₂	I/O ₁₁	I/O ₁₀	I/O ₁₆	I/O ₂₀	I/O ₂₁	V _{CC}
F	I/O ₁₃ TMS	V _{CC}	I/O ₁₄	I/O ₁₅	I/O ₁₇	I/O ₁₈	V _{CC}	I/O ₁₉ TDO

Note:

20. For 3.3V versions (Ultra37000V), V_{CCO} = V_{CC}.

84-lead PLCC (J83) / CLCC (Y84)
Top View

Note:

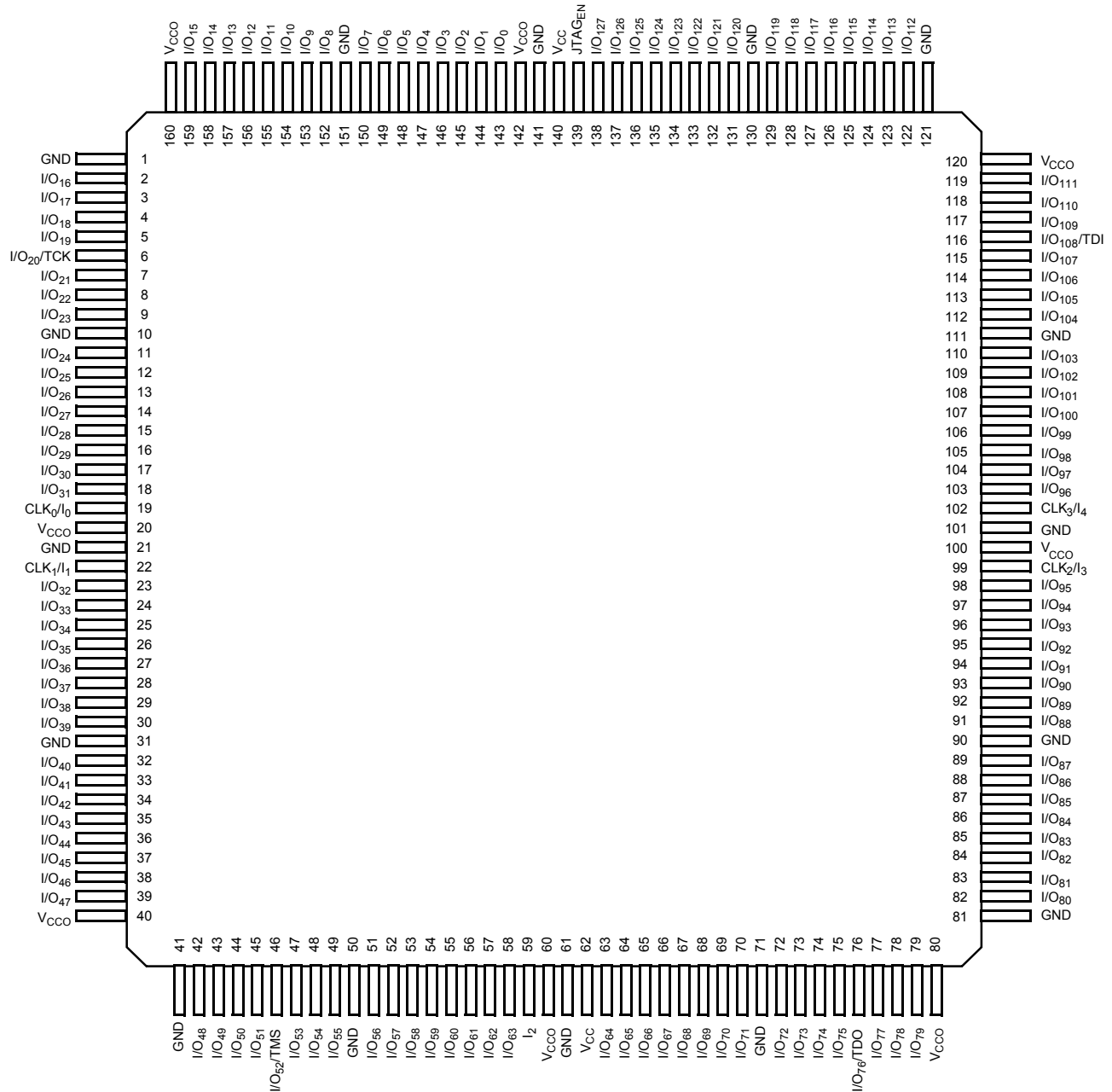
21. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations^[20] (continued)
100-ball Fine-Pitch BGA (BB100) for CY37064V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	NC	I/O ₇	I/O ₅	I/O ₂	I/O ₆₂	I/O ₆₀	I/O ₅₈	I/O ₅₇	I/O ₅₆
B	I/O ₉	I/O ₈	I/O ₆	I/O ₄	I/O ₁	I/O ₆₃	V _{CC}	I/O ₅₉	I/O ₅₅	NC
C	I/O ₁₀	TCK	V _{CC}	I/O ₃	NC	NC	I/O ₆₁	V _{CC}	TDI	I/O ₅₄
D	I/O ₁₁	NC	I/O ₁₂	I/O ₁₃	I/O ₀	NC	I/O ₅₁	I/O ₅₂	CLK ₃ / I ₄	I/O ₅₃
E	I/O ₁₄	CLK ₀ / I ₀	I/O ₁₅	NC	GND	GND	I/O ₄₈	I/O ₄₉	CLK ₂ / I ₃	I/O ₅₀
F	I/O ₁₇	NC	NC	I/O ₁₆	GND	GND	NC	NC	I ₂	I/O ₄₇
G	I/O ₂₂	CLK ₁ / I ₁	I/O ₂₁	I/O ₁₉	I/O ₁₈	I/O ₄₆	I/O ₄₅	I/O ₄₄	NC	I/O ₄₃
H	I/O ₂₃	TMS	V _{CC}	I/O ₂₀	NC	I/O ₃₂	I/O ₄₂	V _{CC}	TDO	I/O ₄₁
J	NC	I/O ₂₆	I/O ₂₈	NC	I/O ₃₁	I/O ₃₃	I/O ₃₅	I/O ₃₇	I/O ₃₉	I/O ₄₀
K	I/O ₂₄	I/O ₂₅	I/O ₂₇	I/O ₂₉	I/O ₃₀	I/O ₃₄	I/O ₃₆	I/O ₃₈	NC	NC

100-ball Fine-Pitch BGA (BB100) for CY37128V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	I/O ₉	I/O ₈	I/O ₆	I/O ₃	I/O ₇₆	I/O ₇₄	I/O ₇₂	I/O ₇₁	I/O ₇₀
B	I/O ₁₁	I/O ₁₀	I/O ₇	I/O ₅	I/O ₂	I/O ₇₇	V _{CC}	I/O ₇₃	I/O ₆₈	I/O ₆₉
C	I/O ₁₂	I/O ₁₃ TCK	V _{CC}	I/O ₄	I/O ₁	I/O ₇₈	I/O ₇₅	V _{CC}	I/O ₆₇ TDI	I/O ₆₆
D	I/O ₁₄	NC	I/O ₁₅	I/O ₁₆	I/O ₀	I/O ₇₉	I/O ₆₃	I/O ₆₄	CLK ₃ / I ₄	I/O ₆₅
E	I/O ₁₇	CLK ₀ / I ₀	I/O ₁₈	I/O ₁₉	GND	GND	I/O ₆₀	I/O ₆₁	CLK ₂ / I ₃	I/O ₆₂
F	I/O ₂₂	JTAG EN	I/O ₂₁	I/O ₂₀	GND	GND	I/O ₅₉	I/O ₅₈	I ₂	I/O ₅₇
G	I/O ₂₇	CLK ₁ / I ₁	I/O ₂₆	I/O ₂₄	I/O ₂₃	I/O ₅₆	I/O ₅₅	I/O ₅₄	NC	I/O ₅₃
H	I/O ₂₈	I/O ₃₃ TMS	V _{CC}	I/O ₂₅	I/O ₃₉	I/O ₄₀	I/O ₅₂	V _{CC}	I/O ₄₇ TDO	I/O ₅₁
J	I/O ₂₉	I/O ₃₂	I/O ₃₅	V _{CC}	I/O ₃₈	I/O ₄₁	I/O ₄₃	I/O ₄₅	I/O ₄₈	I/O ₅₀
K	I/O ₃₀	I/O ₃₁	I/O ₃₄	I/O ₃₆	I/O ₃₇	I/O ₄₂	I/O ₄₄	I/O ₄₆	I/O ₄₉	NC

Pin Configurations^[20] (continued)
**160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View**


Pin Configurations^[20] (continued)
400-Ball Fine-Pitch BGA (BB400)
Top View

A	GND	GND	NC	I/O ₁₇	I/O ₁₆	I/O ₁₄	I/O ₂₉	V _{CC}	I/O ₁₁	GND	GND	I/O ₂₅₇	V _{CC}	I/O ₂₃₉	I/O ₂₃₃	I/O ₂₃₂	I/O ₂₃₀	NC	GND	GND
B	GND	GND	GND	NC	I/O ₁₅	I/O ₁₃	I/O ₂₈	V _{CC}	I/O ₁₀	GND	GND	I/O ₂₅₆	V _{CC}	I/O ₂₃₈	I/O ₂₃₁	I/O ₂₂₉	NC	GND	GND	GND
C	NC	GND	GND	GND	I/O ₂₀	I/O ₁₂	I/O ₂₇	V _{CC}	I/O ₉	GND	GND	I/O ₂₅₅	V _{CC}	I/O ₂₃₇	I/O ₂₂₈	I/O ₂₄₅	GND	GND	GND	NC
D	I/O ₄₄	NC	GND	I/O ₂₁	I/O ₁₉	I/O ₁₈	I/O ₂₆	I/O ₂₅	I/O ₈	GND	GND	I/O ₂₅₄	I/O ₂₃₅	I/O ₂₃₆	I/O ₂₅₁	I/O ₂₄₄	I/O ₂₄₃	GND	NC	I/O ₂₂₇
E	I/O ₄₆	I/O ₄₃	I/O ₂₃	I/O ₂₂	NC	I/O ₃₅	I/O ₃₄	I/O ₂₄	I/O ₇	I/O ₄	I/O ₂₆₃	I/O ₂₅₃	I/O ₂₃₄	I/O ₂₅₀	I/O ₂₄₈	NC	I/O ₂₄₁	I/O ₂₄₂	I/O ₂₂₅	I/O ₂₂₆
F	I/O ₄₇	I/O ₄₅	I/O ₄₂	I/O ₄₁	I/O ₄₀	NC	I/O ₃₃	I/O ₃₂	I/O ₆	I/O ₃	I/O ₂₆₂	I/O ₂₅₂	I/O ₂₄₉	I/O ₂₄₇	I/O ₂₂₀	I/O ₂₂₁	I/O ₂₄₀	I/O ₂₂₂	I/O ₂₂₃	I/O ₂₂₄
G	I/O ₅₃	I/O ₅₂	I/O ₅₁	I/O ₅₀	I/O ₃₉	I/O ₃₈	I/O ₃₇	I/O ₃₁	I/O ₅	I/O ₂	I/O ₂₆₁	V _{CC}	I/O ₂₄₆	I/O ₂₁₇	I/O ₂₁₈	I/O ₂₁₉	I/O ₂₁₂	I/O ₂₁₃	I/O ₂₁₄	I/O ₂₁₅
H	V _{CC}	V _{CC}	V _{CC}	I/O ₄₉	I/O ₄₈	I/O ₃₆	TCK	V _{CC}	I/O ₃₀	I/O ₁	I/O ₂₅₉	I/O ₂₆₀	V _{CC}	TDI	I/O ₂₁₆	I/O ₂₁₀	I/O ₂₁₁	V _{CC}	V _{CC}	V _{CC}
J	I/O ₅₉	I/O ₅₈	I/O ₅₇	I/O ₅₆	I/O ₅₅	I/O ₅₄	V _{CC}	I/O ₆₂	I/O ₆₀	I/O ₀	I/O ₂₅₈	I/O ₂₀₂	I/O ₂₀₃	CLK ₃ /I ₄	I/O ₂₀₄	I/O ₂₀₅	I/O ₂₀₆	I/O ₂₀₇	I/O ₂₀₈	I/O ₂₀₉
K	GND	GND	GND	GND	I/O ₆₅	I/O ₆₄	CLK ₀ /I ₀	I/O ₆₃	I/O ₆₁	GND	GND	I/O ₁₉₈	I/O ₁₉₉	CLK ₂ /I ₃	I/O ₂₀₀	I/O ₂₀₁	GND	GND	GND	GND
L	GND	GND	GND	GND	I/O ₆₉	I/O ₆₈	NC	I/O ₆₇	I/O ₆₆	GND	GND	I/O ₁₉₃	I/O ₁₉₅	I ₂	I/O ₁₉₆	I/O ₁₉₇	GND	GND	GND	GND
M	I/O ₈₉	I/O ₈₈	I/O ₈₇	I/O ₈₆	I/O ₈₅	I/O ₈₄	CLK ₁ /I ₁	I/O ₇₁	I/O ₇₀	I/O ₁₂₆	I/O ₁₃₂	I/O ₁₉₂	I/O ₁₉₄	V _{CC}	I/O ₁₇₄	I/O ₁₇₅	I/O ₁₇₆	I/O ₁₇₇	I/O ₁₇₈	I/O ₁₇₉
N	V _{CC}	V _{CC}	V _{CC}	I/O ₉₁	I/O ₉₀	I/O ₇₂	TMS	V _{CC}	I/O ₁₂₈	I/O ₁₂₇	I/O ₁₃₃	I/O ₁₆₂	V _{CC}	TDO	I/O ₁₈₀	I/O ₁₆₈	I/O ₁₆₉	V _{CC}	V _{CC}	V _{CC}
P	I/O ₉₅	I/O ₉₄	I/O ₉₃	I/O ₉₂	I/O ₇₅	I/O ₇₄	I/O ₇₃	I/O ₁₁₄	V _{CC}	I/O ₁₂₉	I/O ₁₃₄	I/O ₁₃₇	I/O ₁₆₃	I/O ₁₈₁	I/O ₁₈₂	I/O ₁₈₃	I/O ₁₇₀	I/O ₁₇₁	I/O ₁₇₂	I/O ₁₇₃
R	I/O ₉₀	I/O ₇₉	I/O ₇₈	I/O ₁₀₈	I/O ₇₇	I/O ₇₆	I/O ₁₁₅	I/O ₁₁₇	I/O ₁₂₀	I/O ₁₃₀	I/O ₁₃₅	I/O ₁₃₈	I/O ₁₆₄	I/O ₁₆₅	NC	I/O ₁₈₄	I/O ₁₈₅	I/O ₁₈₆	I/O ₁₈₉	I/O ₁₉₁
T	I/O ₈₂	I/O ₈₁	I/O ₁₁₀	I/O ₁₀₉	NC	I/O ₁₁₆	I/O ₁₁₈	I/O ₁₀₂	I/O ₁₂₁	I/O ₁₃₁	I/O ₁₃₆	I/O ₁₃₉	I/O ₁₅₆	I/O ₁₆₆	I/O ₁₆₇	NC	I/O ₁₅₄	I/O ₁₅₅	I/O ₁₈₇	I/O ₁₉₀
U	I/O ₈₃	NC	GND	I/O ₁₁₁	I/O ₁₁₂	I/O ₁₁₉	I/O ₁₀₄	I/O ₁₀₃	I/O ₁₂₂	GND	GND	I/O ₁₄₀	I/O ₁₅₇	I/O ₁₅₈	I/O ₁₅₀	I/O ₁₅₁	I/O ₁₅₃	GND	NC	I/O ₁₈₈
V	NC	GND	GND	GND	I/O ₁₁₃	I/O ₉₆	I/O ₁₀₅	V _{CC}	I/O ₁₂₃	GND	GND	I/O ₁₄₁	V _{CC}	I/O ₁₅₉	I/O ₁₄ 4	I/O ₁₅₂	GND	GND	GND	NC
W	GND	GND	GND	NC	I/O ₉₇	I/O ₉₉	I/O ₁₀₆	V _{CC}	I/O ₁₂₄	GND	GND	I/O ₁₄₂	V _{CC}	I/O ₁₆₀	I/O ₁₄₅	I/O ₁₄₇	NC	GND	GND	GND
Y	GND	GND	NC	I/O ₉₈	I/O ₁₀₀	I/O ₁₀₁	I/O ₁₀₇	V _{CC}	I/O ₁₂₅	GND	GND	I/O ₁₄₃	V _{CC}	I/O ₁₆₁	I/O ₁₄₆	I/O ₁₄₈	I/O ₁₄₉	NC	GND	GND

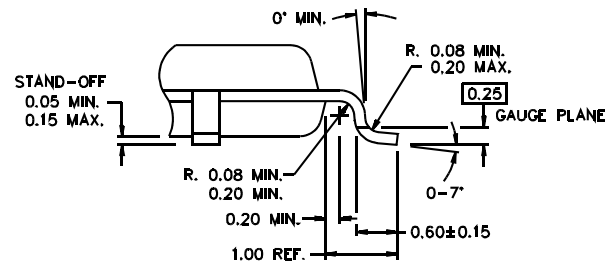
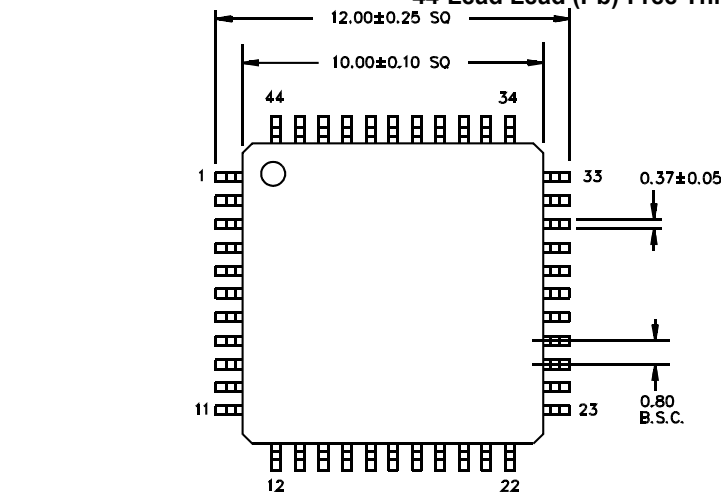
5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military

Package Diagrams

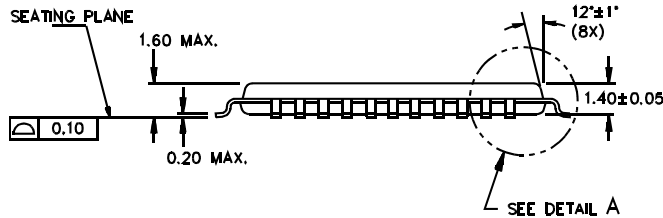
44-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack A44

DIMENSIONS ARE IN MILLIMETERS



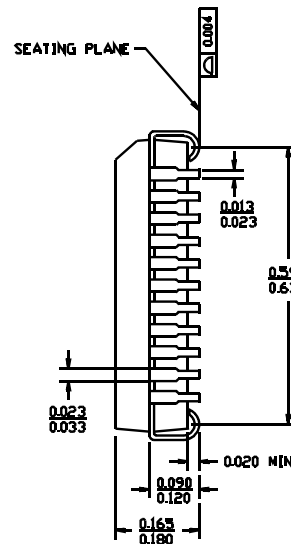
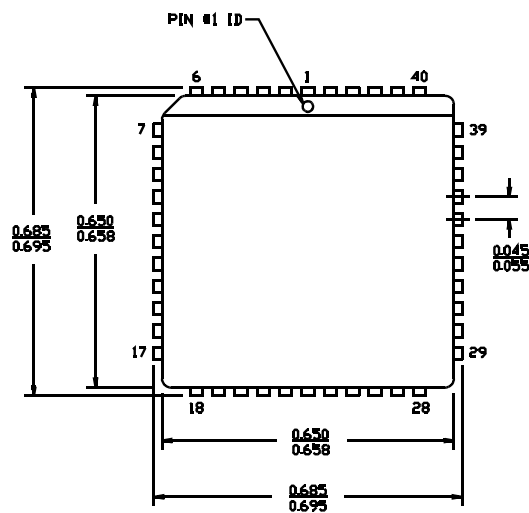
DETAIL A

51-85064-*B



44-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J67

DIMENSIONS IN INCHES MIN. MAX.



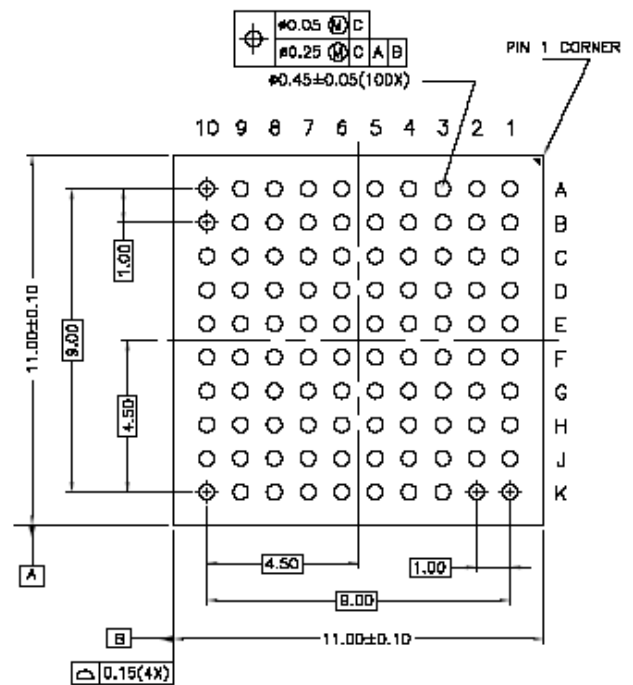
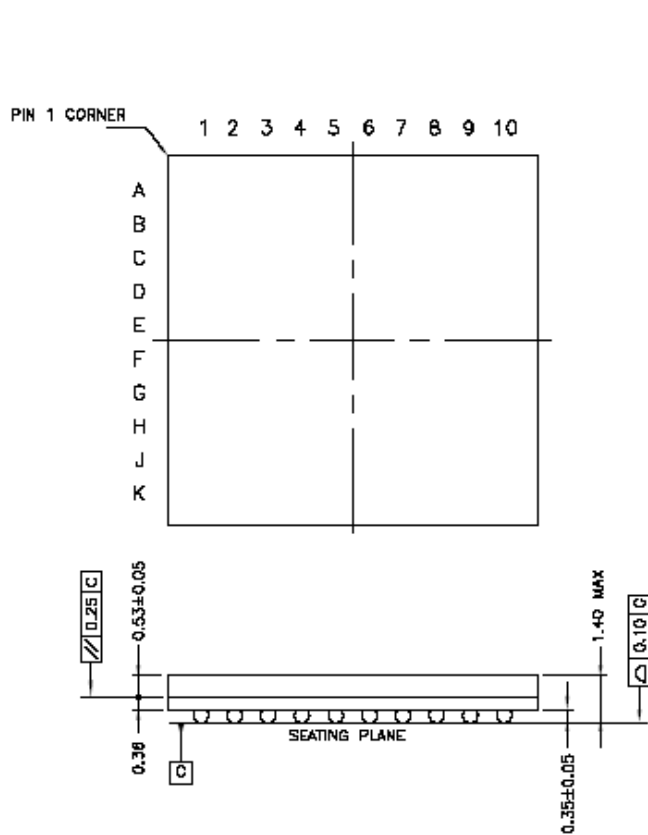
51-85003-*A

Package Diagrams (continued)

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100

TOP VIEW

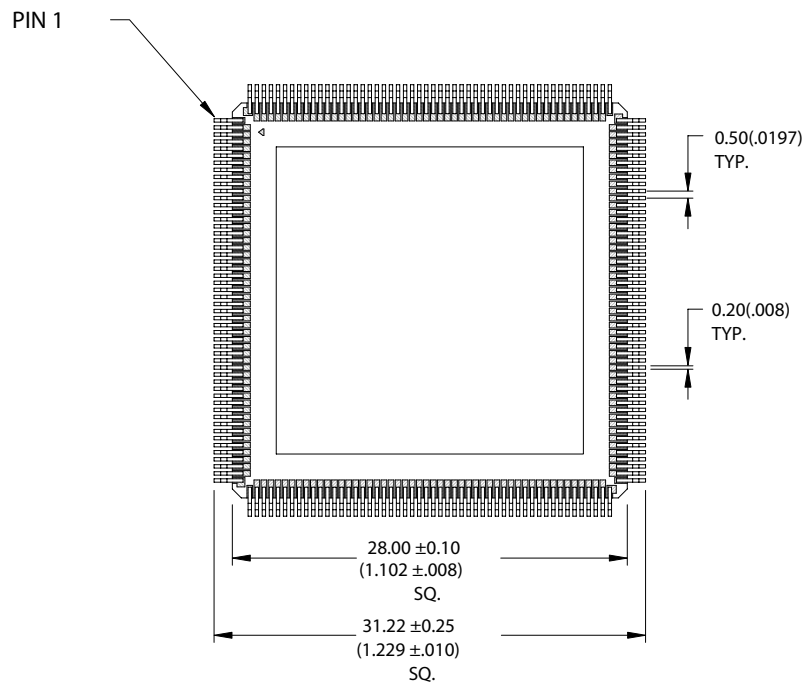
BOTTOM VIEW



51-85107-B

Package Diagrams (continued)

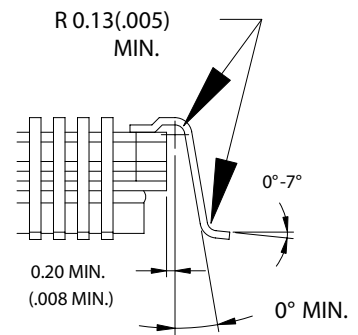
208-Lead Ceramic Quad Flatpack (Cavity Up) U208



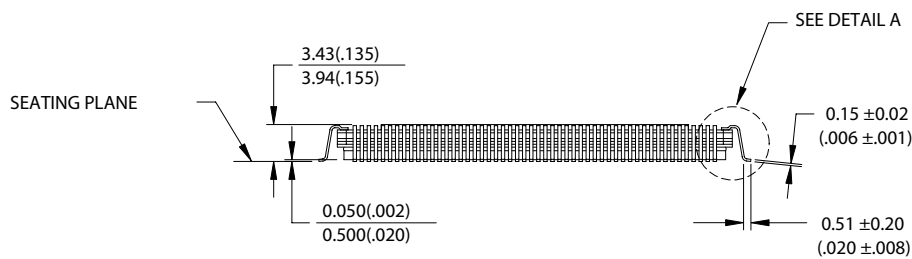
DIMENSIONS IN MM (INCH)

REFERENCE JEDEC: N/A

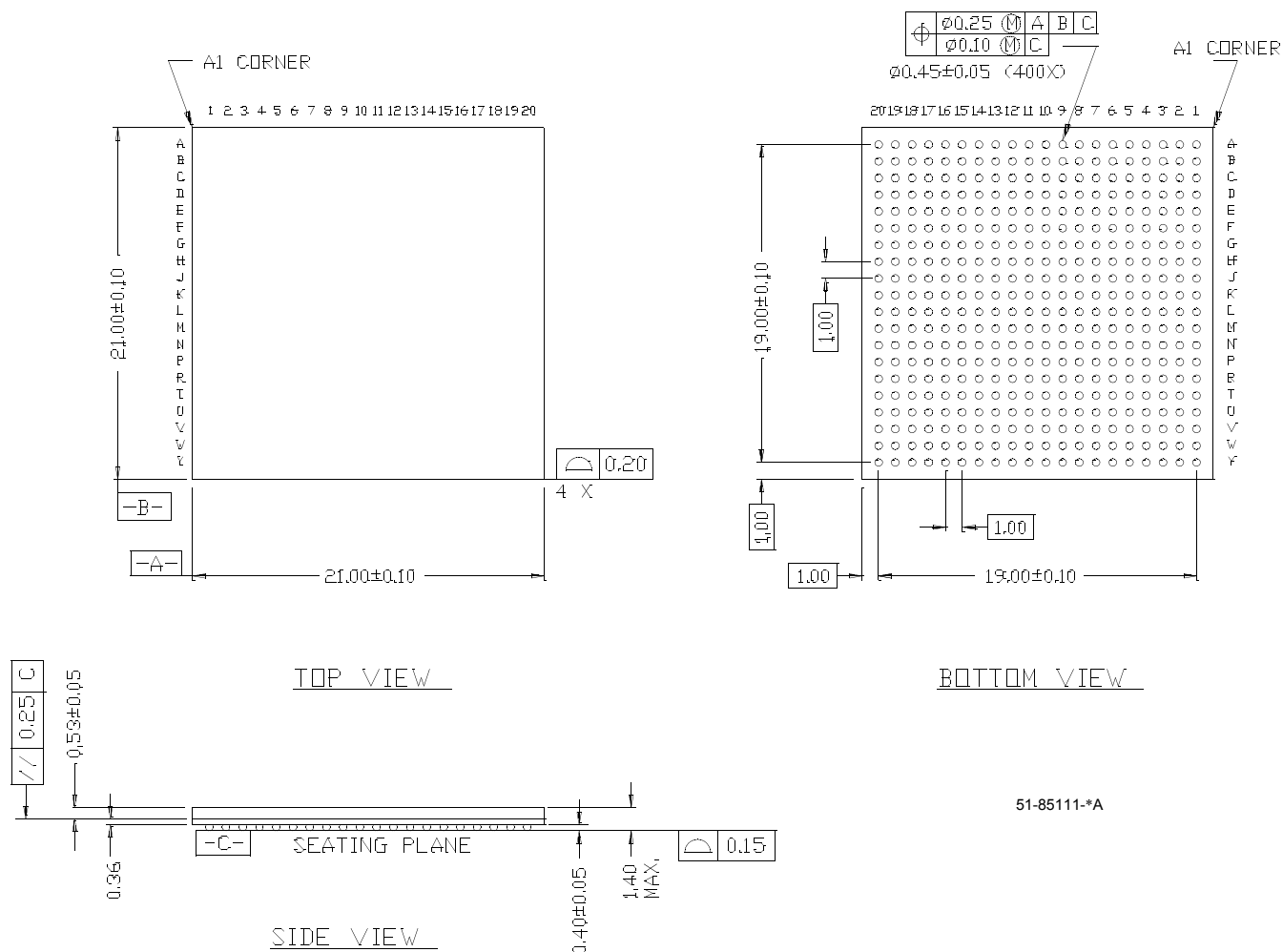
PKG. WEIGHT: 6-7gms



DETAIL A



51-80105-B

Package Diagrams (continued)
400-Ball FBGA (21 x 21 x 1.4 mm) BB400


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