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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	69
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37128p100-125axi

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	388-Lead PBGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83



Ultra37000 CPLD Family

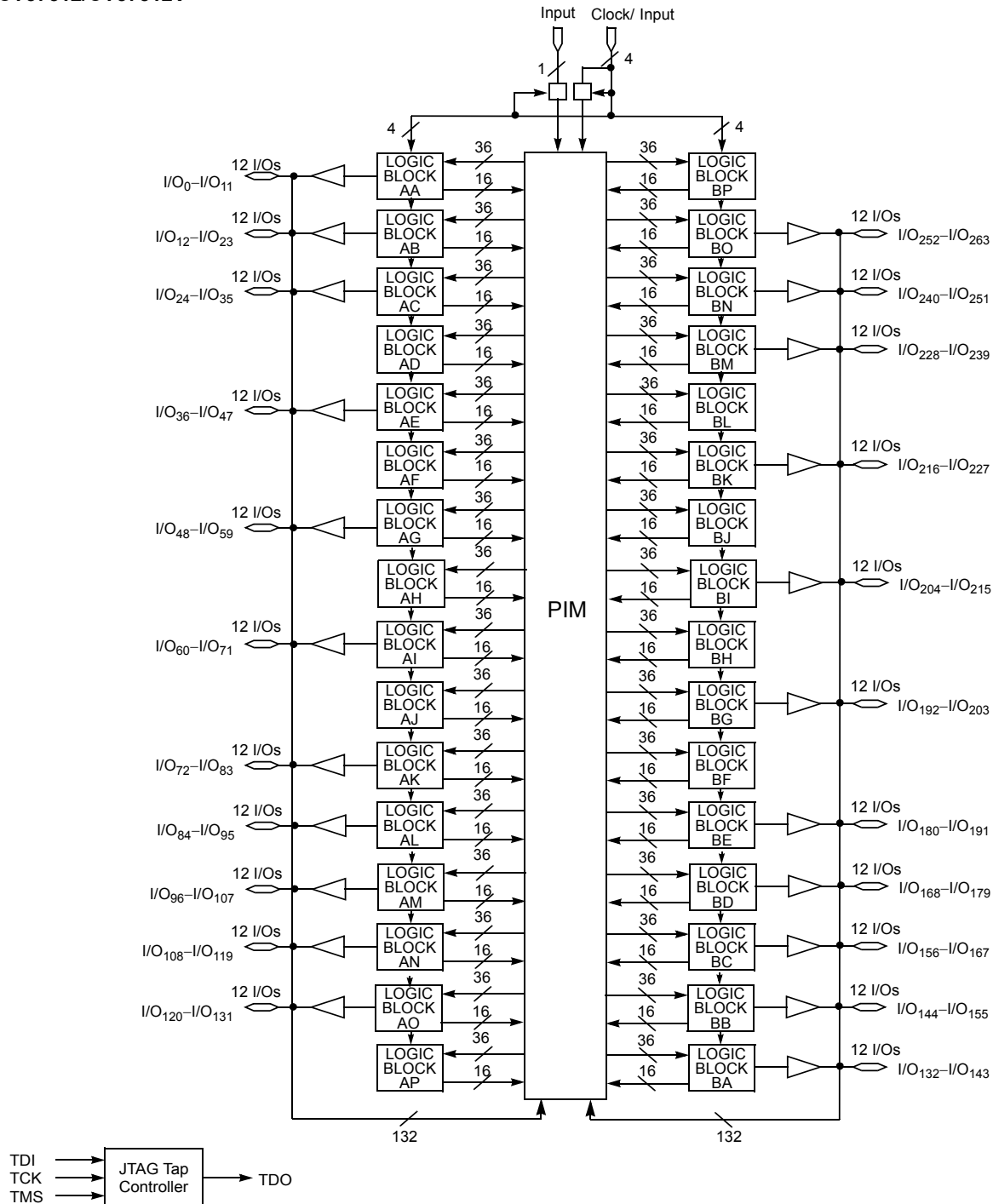
The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams (continued)
CY37512/CY37512V


Inductance^[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$	2	5	2	8	5	8	9	11	nH

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	10	pF
C_{CLK}	Clock Signal Capacitance	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	12	pF
C_{DP}	Dual-Function Pins ^[9]	$V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$	16	pF

Endurance Characteristics^[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions ^[2]	1,000	10,000	Cycles

3.3V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature $-65^\circ C$ to $+150^\circ C$

Ambient Temperature with

Power Applied $-55^\circ C$ to $+125^\circ C$

Supply Voltage to Ground Potential $-0.5V$ to $+4.6V$

DC Voltage Applied to Outputs

in High-Z State $-0.5V$ to $+7.0V$

DC Input Voltage $-0.5V$ to $+7.0V$

DC Program Voltage 3.0 to $3.6V$

Current into Outputs 8 mA

Static Discharge Voltage $> 2001V$
(per MIL-STD-883, Method 3015)

Latch-up Current $> 200\text{ mA}$

Operating Range^[2]

Range	Ambient Temperature ^[2]	Junction Temperature	V_{CC} ^[10]
Commercial	$0^\circ C$ to $+70^\circ C$	$0^\circ C$ to $+90^\circ C$	$3.3V \pm 0.3V$
Industrial	$-40^\circ C$ to $+85^\circ C$	$-40^\circ C$ to $+105^\circ C$	$3.3V \pm 0.3V$
Military ^[3]	$-55^\circ C$ to $+125^\circ C$	$-55^\circ C$ to $+130^\circ C$	$3.3V \pm 0.3V$

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -4\text{ mA (Com'I)}^{[4]}$ $I_{OH} = -3\text{ mA (Mil)}^{[4]}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $I_{OL} = 8\text{ mA (Com'I)}^{[4]}$ $I_{OL} = 6\text{ mA (Mil)}^{[4]}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs ^[7]	2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs ^[7]	-0.5	0.8	V
I_{IX}	Input Load Current	$V_I = \text{GND OR } V_{CC}$, Bus-Hold Disabled	-10	10	μA
I_{OZ}	Output Leakage Current	$V_O = \text{GND or } V_{CC}$, Output Disabled, Bus-Hold Disabled	-50	50	μA
I_{OS}	Output Short Circuit Current ^[5, 8]	$V_{CC} = \text{Max.}$, $V_{OUT} = 0.5V$	-30	-160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	$V_{CC} = \text{Min.}$, $V_{IL} = 0.8V$	+75		μA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	$V_{CC} = \text{Min.}$, $V_{IH} = 2.0V$	-75		μA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	$V_{CC} = \text{Max.}$		+500	μA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	$V_{CC} = \text{Max.}$		-500	μA

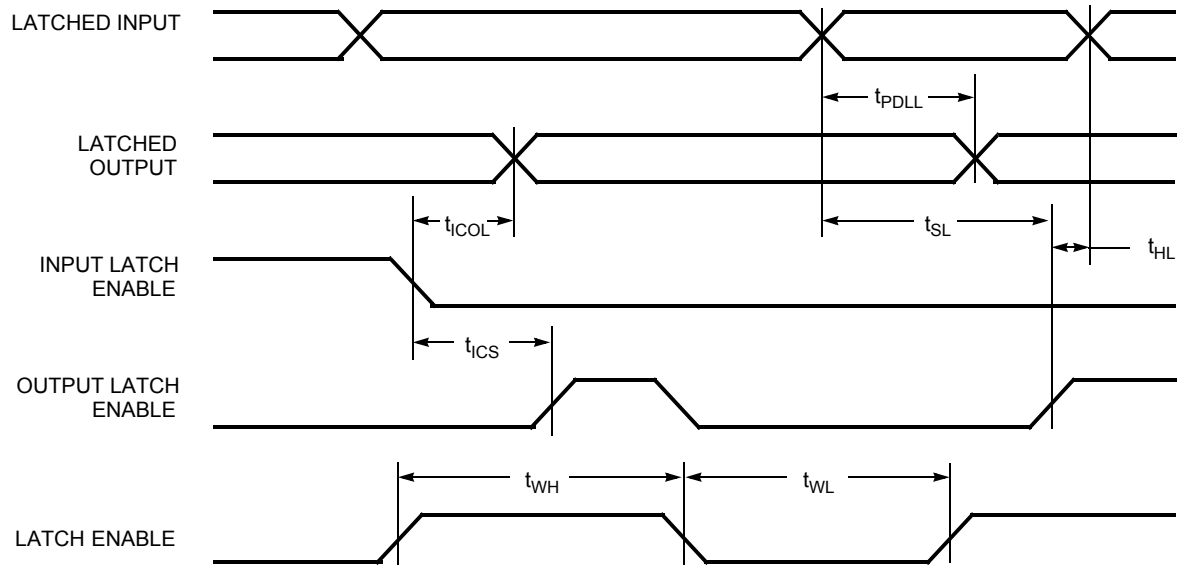
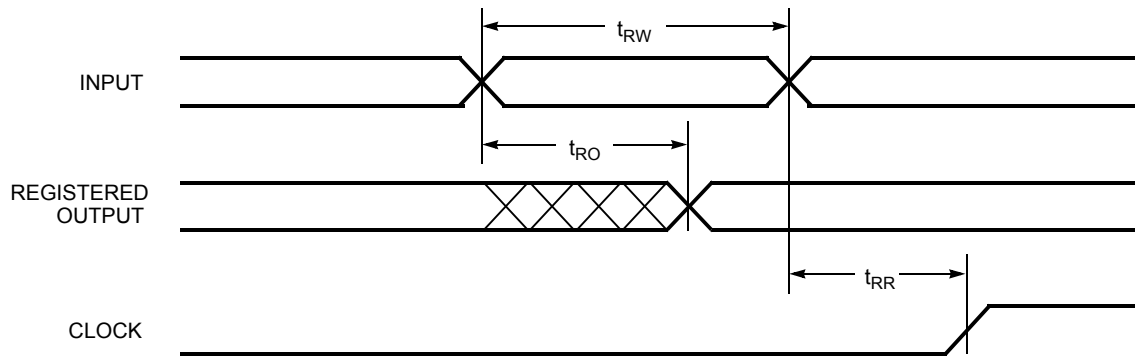
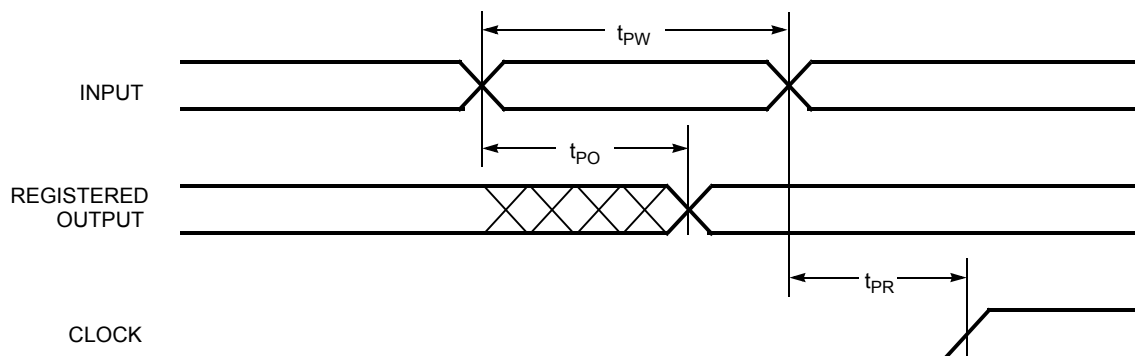
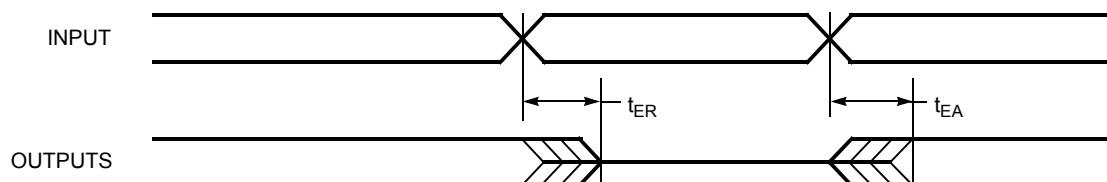
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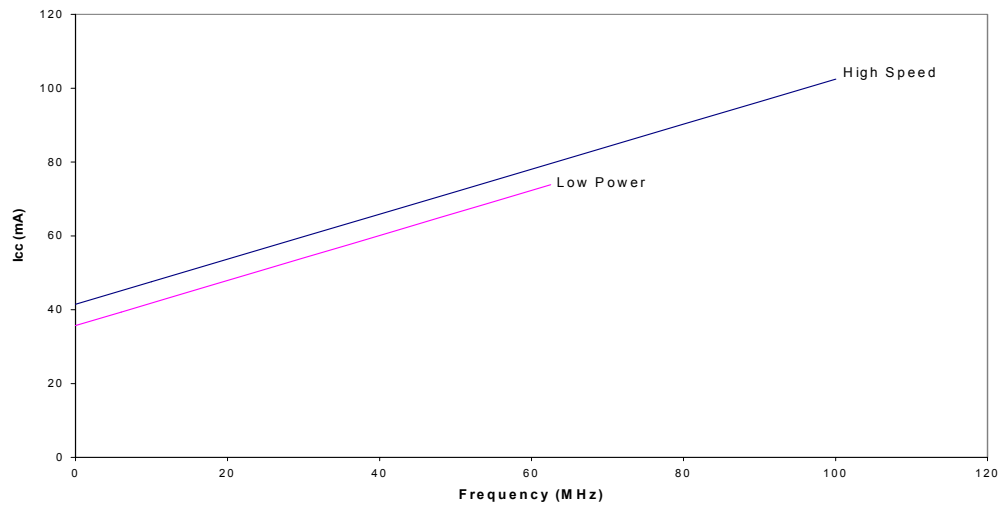
9. Dual pins are I/O with JTAG pins.

10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is $3.3V \pm 0.16V$.

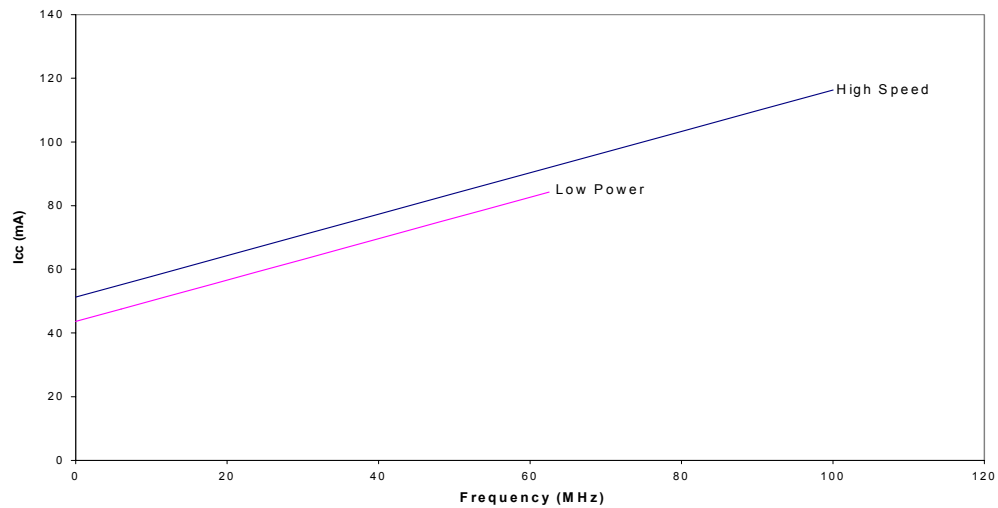
Switching Characteristics Over the Operating Range (continued)^[12]

Parameter	Description	Unit
Product Term Clocking Parameters		
$t_{COPT}^{[13, 14, 15]}$	Product Term Clock or Latch Enable (PTCLK) to Output	ns
t_{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{HPT}	Register or Latch Data Hold Time	ns
$t_{ISPT}^{[13]}$	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time	ns
$t_{CO2PT}^{[13, 14, 15]}$	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)	ns
Pipelined Mode Parameters		
$t_{ICS}^{[13]}$	Input Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃)	ns
Operating Frequency Parameters		
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$) ^[5]	MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$) ^[5]	MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$) ^[5]	MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$) ^[5]	MHz
Reset/Preset Parameters		
t_{RW}	Asynchronous Reset Width ^[5]	ns
$t_{RR}^{[13]}$	Asynchronous Reset Recovery Time ^[5]	ns
$t_{RO}^{[13, 14, 15]}$	Asynchronous Reset to Output	ns
t_{PW}	Asynchronous Preset Width ^[5]	ns
$t_{PR}^{[13]}$	Asynchronous Preset Recovery Time ^[5]	ns
$t_{PO}^{[13, 14, 15]}$	Asynchronous Preset to Output	ns
User Option Parameters		
t_{LP}	Low Power Adder	ns
t_{SLEW}	Slow Output Slew Rate Adder	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder ^[5]	ns
JTAG Timing Parameters		
$t_{S JTAG}$	Set-up Time from TDI and TMS to TCK ^[5]	ns
$t_{H JTAG}$	Hold Time on TDI and TMS ^[5]	ns
$t_{CO JTAG}$	Falling Edge of TCK to TDO ^[5]	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency ^[5]	ns

Switching Waveforms (continued)
Latched Input and Output

Asynchronous Reset

Asynchronous Preset

Output Enable/Disable


Typical 3.3V Power Consumption (continued)
CY37192V


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

CY37256V


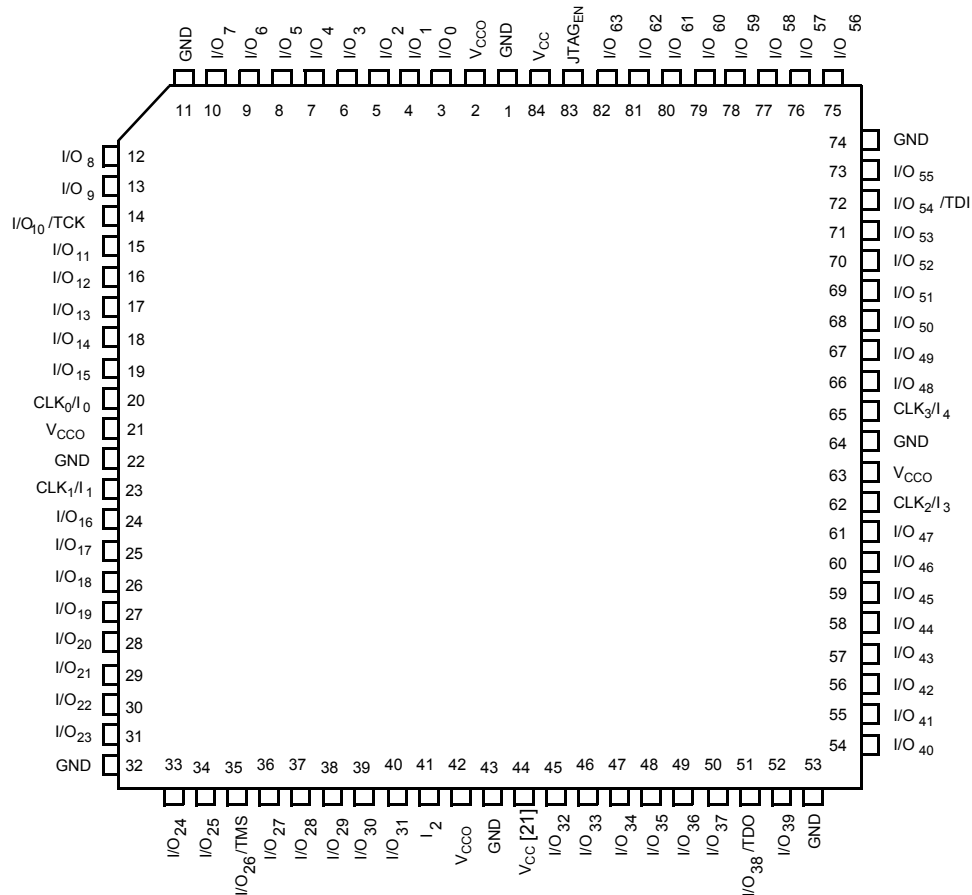
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

Pin Configurations^[20] (continued)
48-ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O ₅ TCK	V _{CC}	I/O ₃	I/O ₁	I/O ₃₁	I/O ₃₀	V _{CC}	I/O ₂₇ TDI
B	V _{CC}	I/O ₄	I/O ₂	I/O ₀	I/O ₂₉	I/O ₂₈	I/O ₂₆	CLK ₁ /I ₄
C	CLK ₂ /I ₀	I/O ₇	I/O ₆	GND	GND	I/O ₂₅	I/O ₂₄	I ₃
D	JTAG _{EN}	I/O ₈	I/O ₉	GND	GND	I/O ₂₂	I/O ₂₃	CLK ₃ /I ₂
E	CLK ₀ /I ₁	I/O ₁₂	I/O ₁₁	I/O ₁₀	I/O ₁₆	I/O ₂₀	I/O ₂₁	V _{CC}
F	I/O ₁₃ TMS	V _{CC}	I/O ₁₄	I/O ₁₅	I/O ₁₇	I/O ₁₈	V _{CC}	I/O ₁₉ TDO

Note:

20. For 3.3V versions (Ultra37000V), V_{CCO} = V_{CC}.

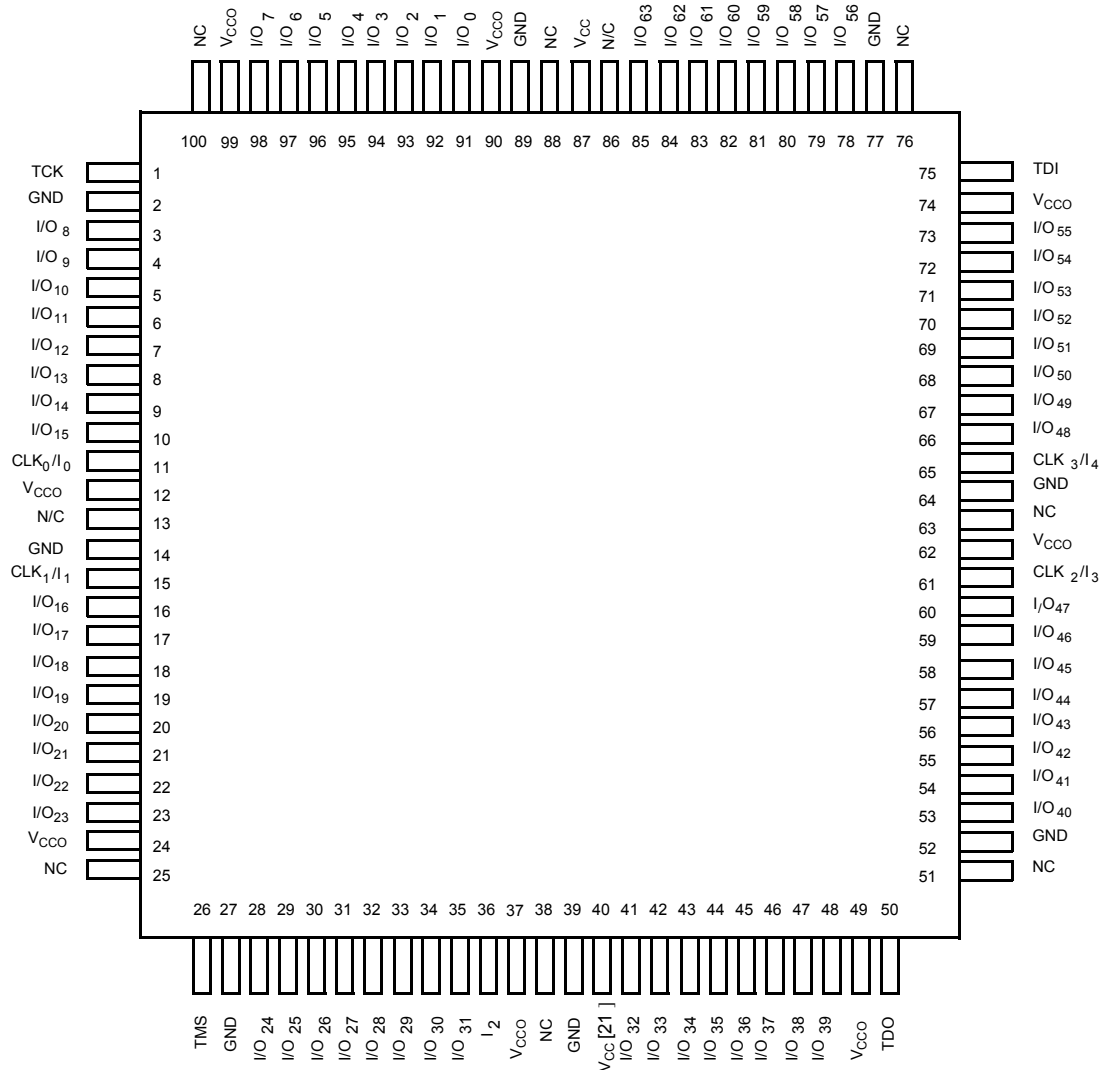
84-lead PLCC (J83) / CLCC (Y84)
Top View

Note:

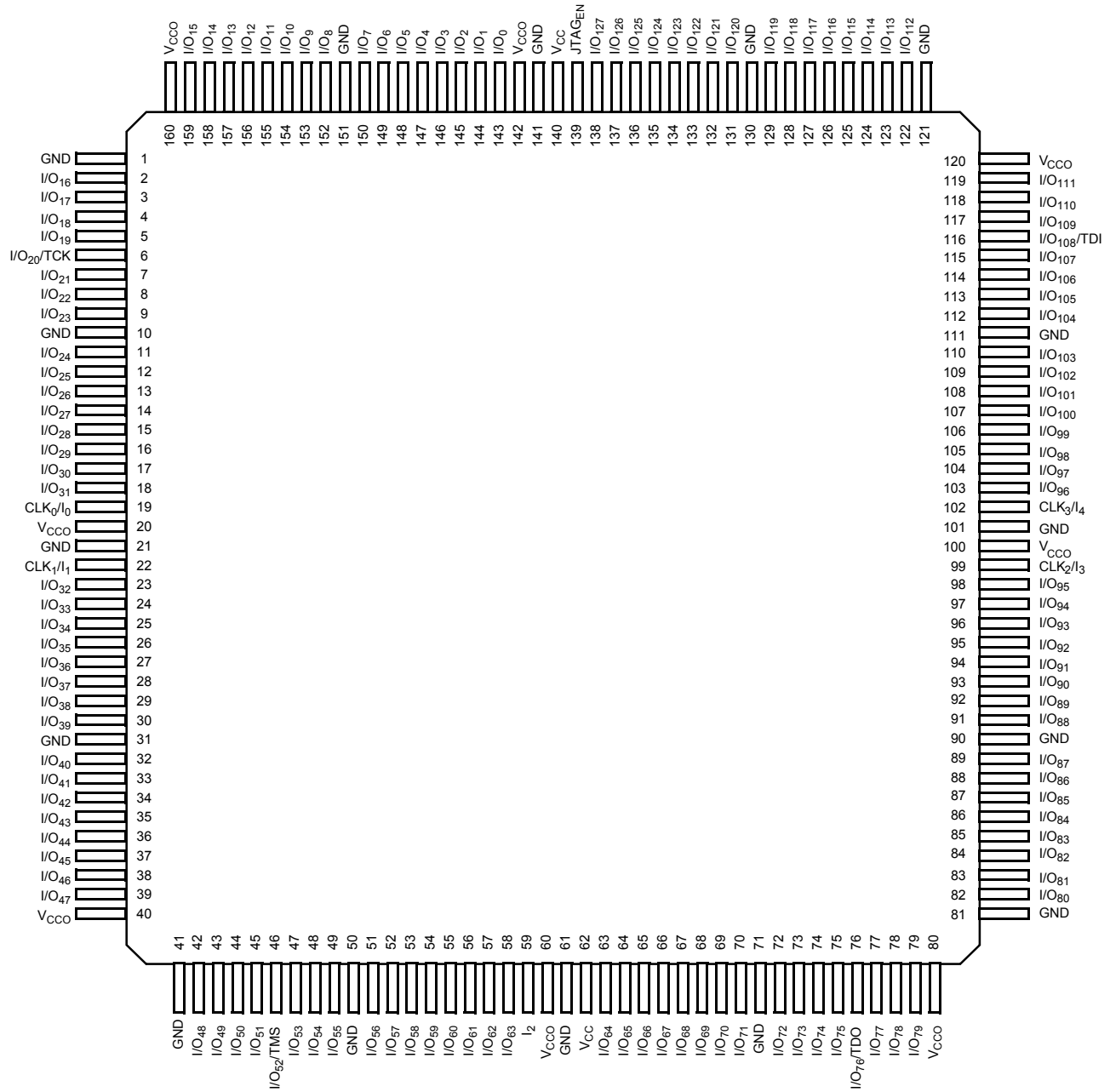
21. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations^[20] (continued)

100-lead TQFP (A100)

Top View



Pin Configurations^[20] (continued)
**160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View**


5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
128	167	CY37128P84-167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-167JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-167AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-167AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-167AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-167AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	125	CY37128P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-125JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P84-125JXI	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-125AI	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		5962-9952102QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
	100	CY37128P84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P84-100JXC	J83	84-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37128P100-100AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-100AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-100AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128P84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-100AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P100-100AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128P160-100AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952101QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	154	CY37192P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-154AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	125	CY37192P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37192P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	83	CY37192P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37192P160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	154	CY37256P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-154AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-154NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-154BGC	BG292	292-Ball Plastic Ball Grid Array	
	125	CY37256P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952302QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
	83	CY37256P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952301QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	125	CY37384P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
	83	CY37384P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-125BGC	BG388	388-Ball Plastic Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

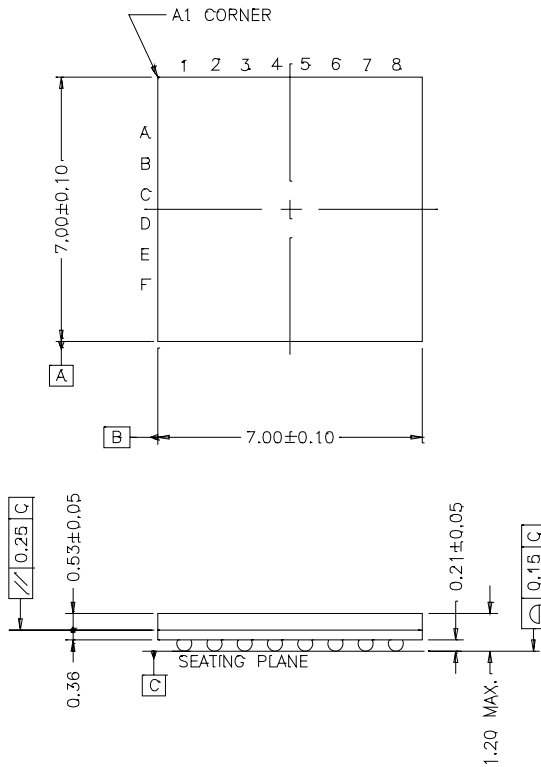
3.3V Ordering Information

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-143BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAI	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP44-100JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	

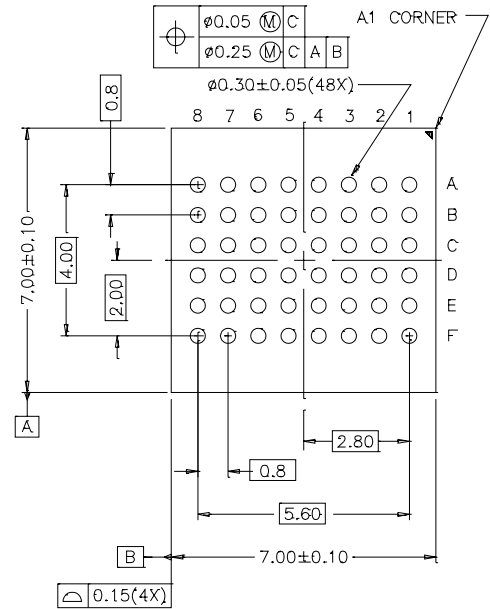
Package Diagrams (continued)

48-Ball (7.0 mm x 7.0 mm x 1.2 mm, 0.80 pitch) Thin BGA BA48D

TOP VIEW



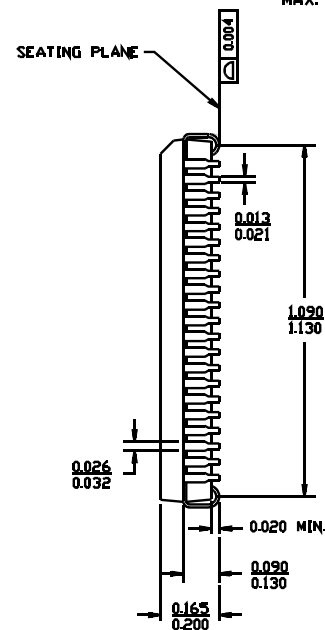
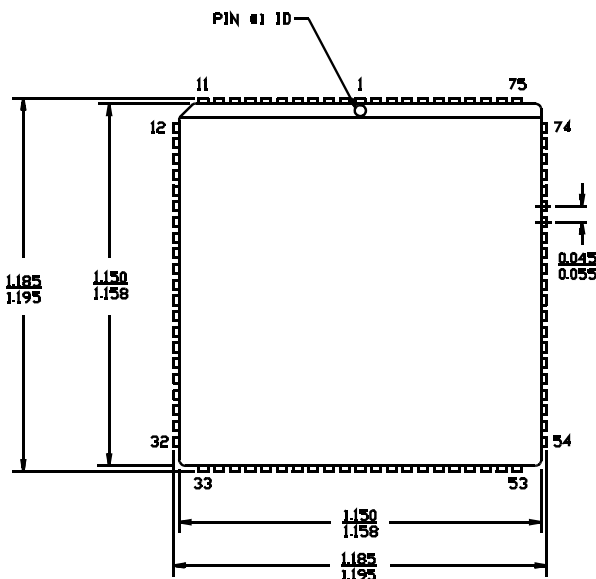
BOTTOM VIEW



51-85109-°C

84-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J83

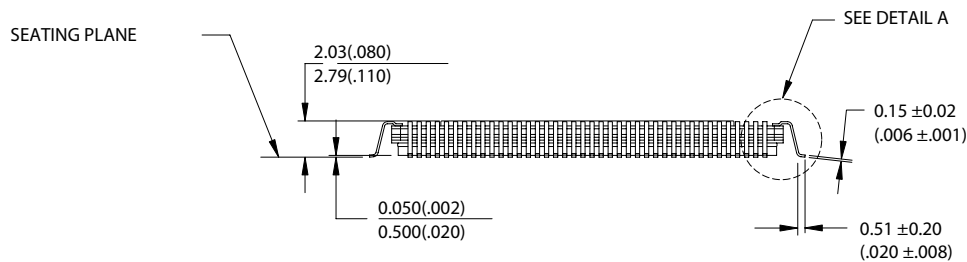
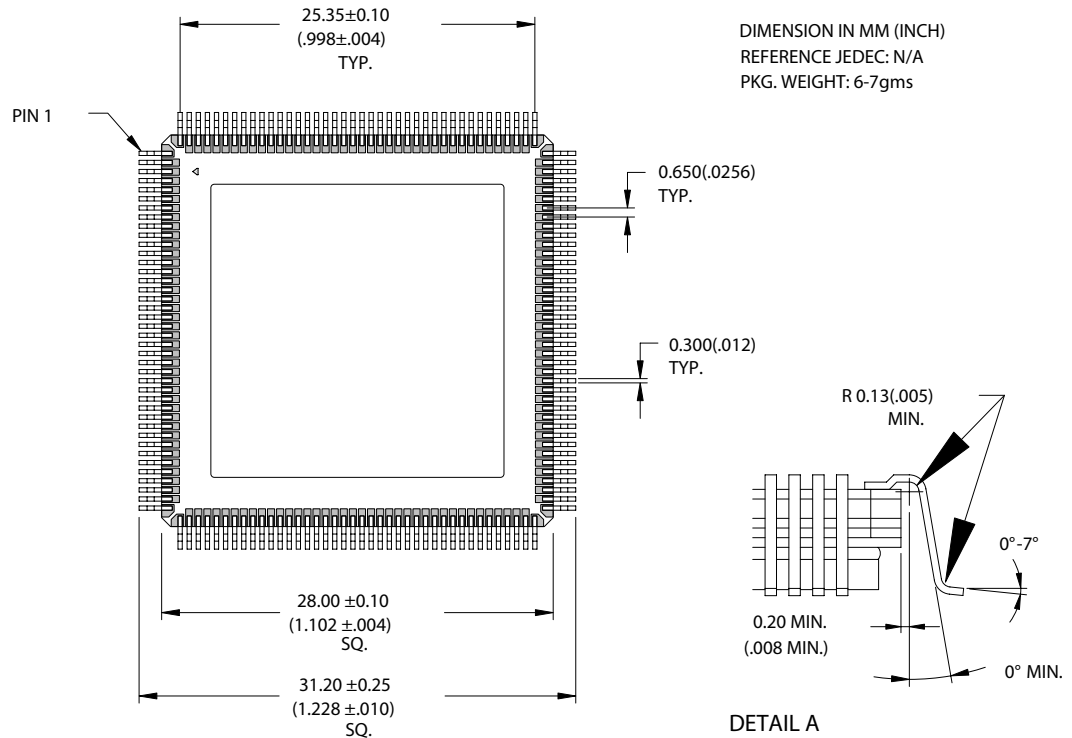
DIMENSIONS IN INCHES MIN. MAX.



51-85006-°A

Package Diagrams (continued)

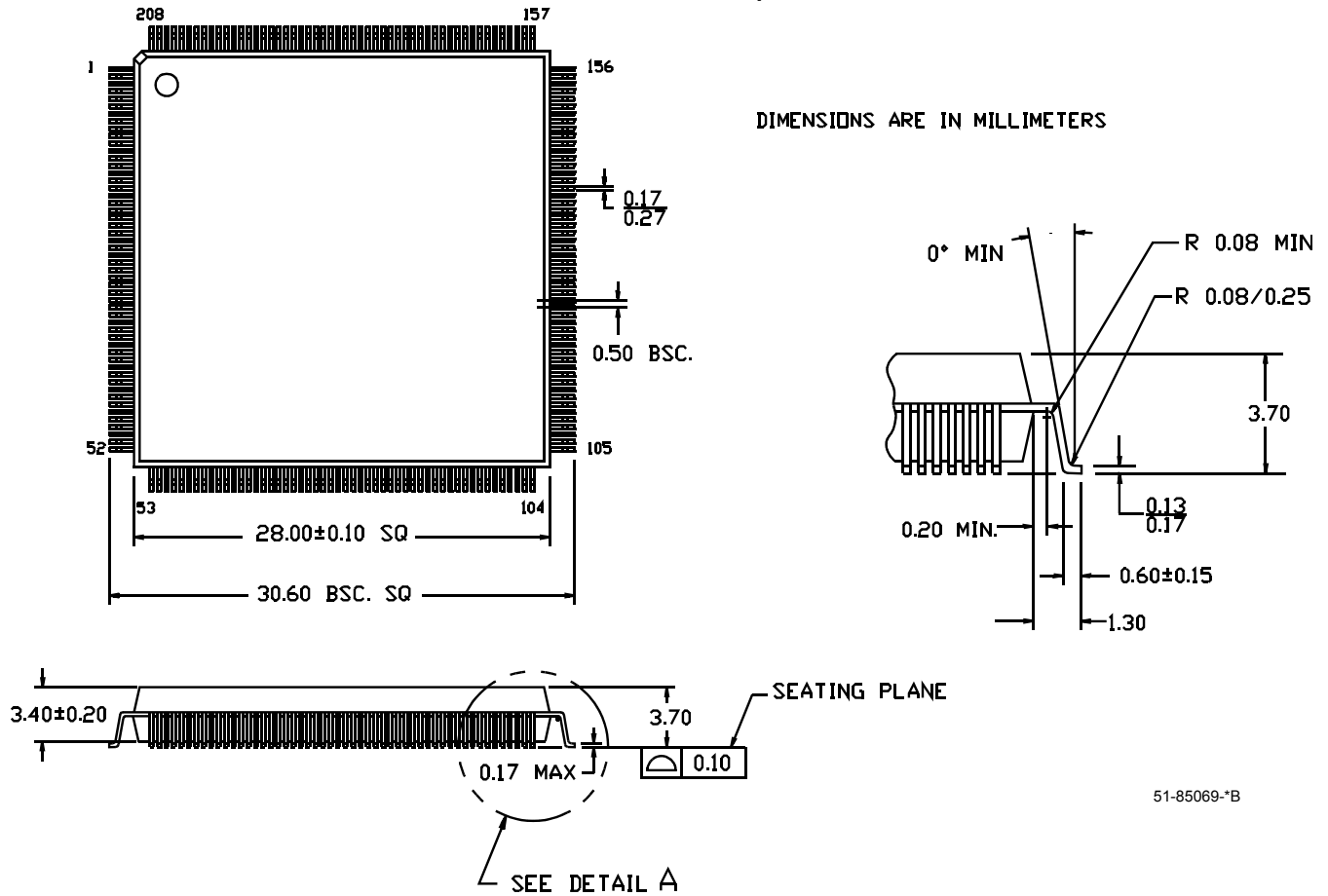
160-Lead Ceramic Quad Flatpack (Cavity Up) U162



51-80106-*A

Package Diagrams (continued)

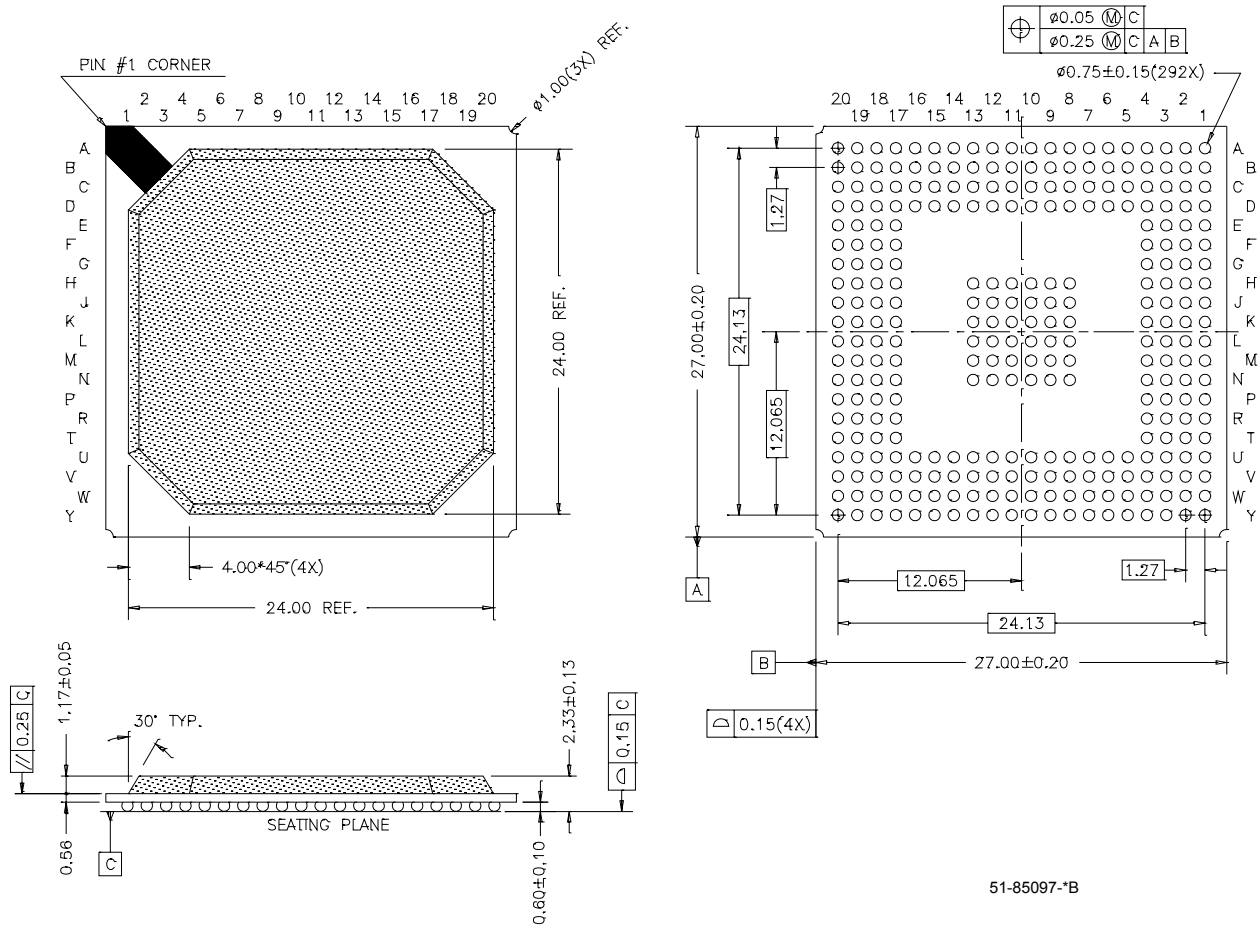
208-Lead Plastic Quad Flatpack N208



51-85069-*B

Package Diagrams (continued)

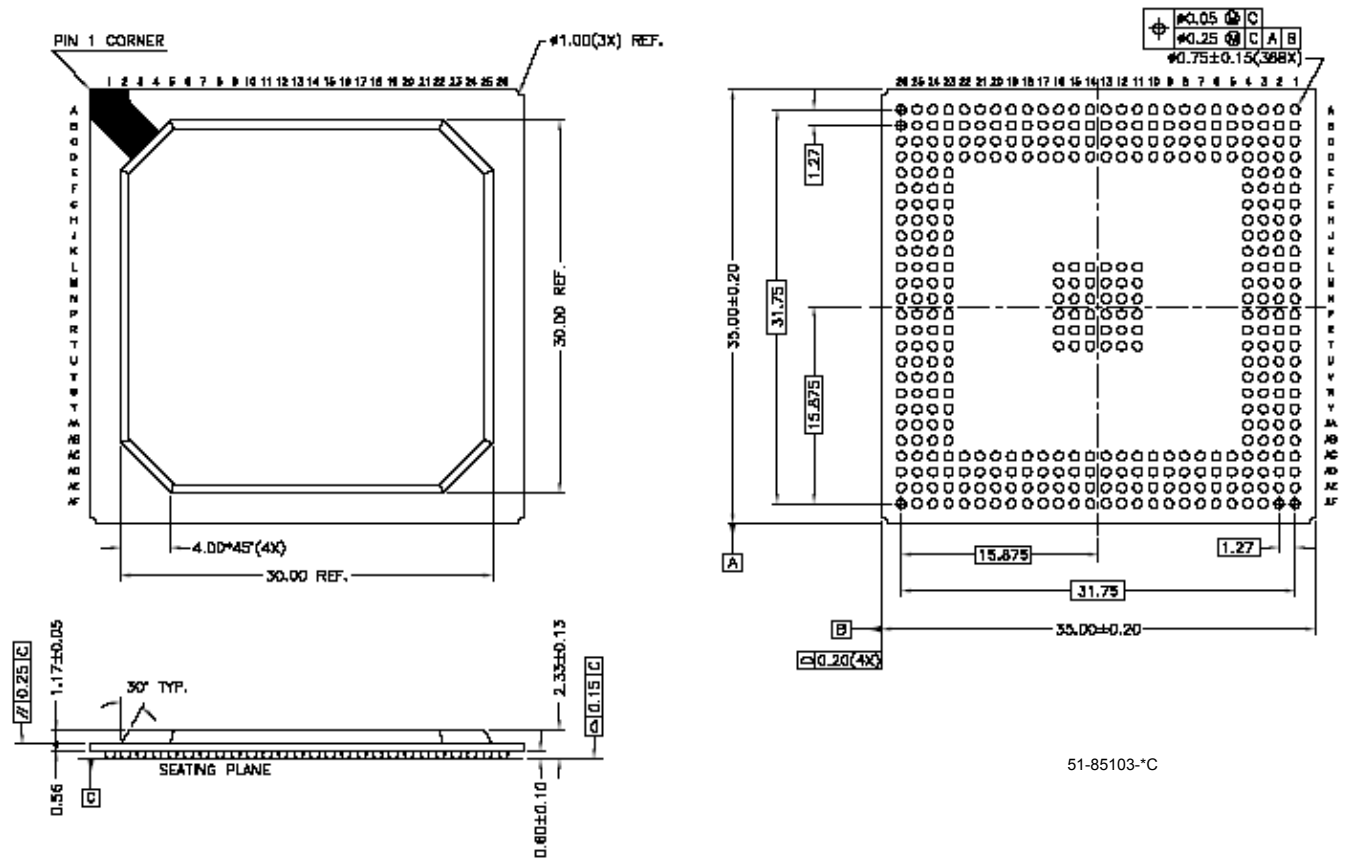
292-Ball Plastic Ball Grid Array PBGA (27 x 27 x 2.33 mm) BG292



51-85097-*B

Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388



51-85103-°C

Addendum**3.3V Operating Range****(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)**

Range	Ambient Temperature ^[2]	Junction Temperature	V _{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.16V

Document History Page

Document Title: Ultra37000 CPLD Family 5V, 3.3V, ISR™ High-Performance CPLDs Document Number: 38-03007				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106272	04/18/01	SZV	Change from Spec number: 38-00475 to 38-03007
*A	124942	03/21/03	OOR	Updated 3.3V V _{CC} requirements for –144 speeds Added an Addendum
*B	126262	05/09/03	TEH	Changed pinout for CY37128V BB100 package
*C	128125	07/16/03	HOM	Obsoleted following 3.3V PLCC packaged devices: CY37032VP44-143JC CY37032VP44-100JC CY37032VP44-100JI CY37064VP44-143JC CY37064VP84-143JC CY37064VP44-100JC CY37064VP84-100JC CY37064VP44-100JI CY37064VP84-100JI CY37128VP84-125JC CY37128VP84-83JC CY37128VP84-83JI
*D	282709	See ECN	YDT	Changed package diagrams and labels for consistency Added Lead (Pb)-free logo on first page, as well as a note in Features Added Lead (Pb)-free package diagram labels Added Lead-free Parts to Ordering Information CY37032P44-200AXC, CY37032P44-200JXC, CY37032P44-154AXI, CY37032P44-154JXI, CY37032P44-125AXC, CY37032P44-125JXC, CY37064P44-200AXC, CY37064P44-200JXC, CY37064P100-200AXC, CY37064P44-154AXI, CY37064P44-154JXI, CY37064P44-125AXC, CY37064P44-125JXC, CY37064P100-125AXC, CY37064P44-125AXI, CY37064P100-125AXI, CY37128P84-167JXC, CY37128P100-167AXC, CY37128P160-167AXC, CY37128P84-125JXC, CY37128P100-125AXC, CY37128P160-125AXC, CY37128P84-125JXI, CY37128P100-125AXI, CY37128P160-125AXI, CY37128P84-100JXC, CY37128P100-100AXC, CY37128P160-100AXC, CY37128P100-100AXI, CY37192P160-154AXC, CY37192P160-125AXC, CY37192P160-125AXI, CY37192P160-83AXC, CY37192P160-83AXI, CY37256P160-154AXC, CY37256P160-125AXC, CY37256P160-125AXI, CY37256P160-83AXC, CY37256P160-83AXI, CY37032VP44-143AXC, CY37032VP44-100AXC, CY37032VP44-100AXI, CY37032VP44-100JXI, CY37064VP44-143AXC, CY37064VP100-143AXC, CY37064VP44-100AXC, CY37064VP100-100AXC, CY37064VP44-100AXI, CY37064VP100-100AXI, CY37128VP100-125AXC, CY37128VP160-125AXC, CY37128VP160-125AXI, CY37128VP100-83AXC, CY37128VP160-83AXC, CY37128VP100-83AXI, CY37128VP160-83AXI, CY37192VP160-100AXC, CY37192VP160-66AXC, CY37256VP160-100AXC, CY37256VP160-100AXI, CY37256VP160-66AXC
*E	321635	See ECN	PCX	Added Package Diagram BG292 Updated all PBGA package type information (BG292 & BG388)