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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

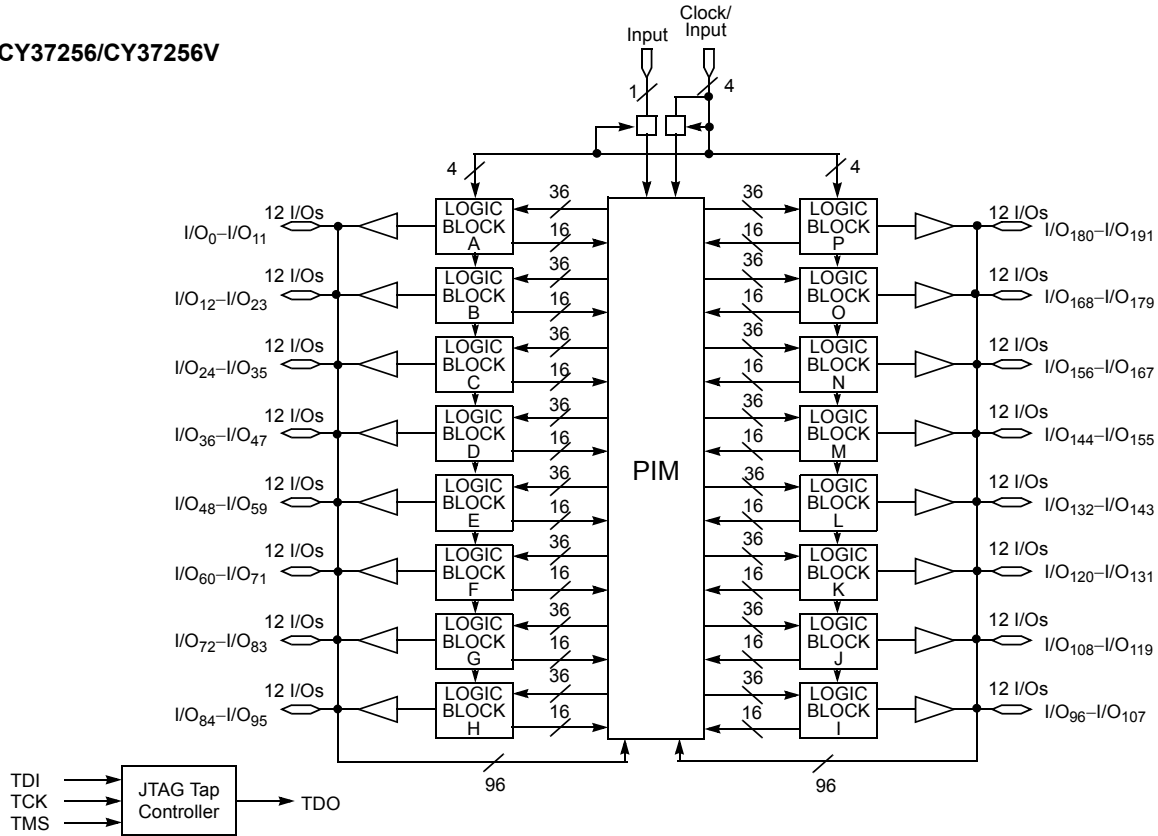
Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	133
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37128p160-100axc

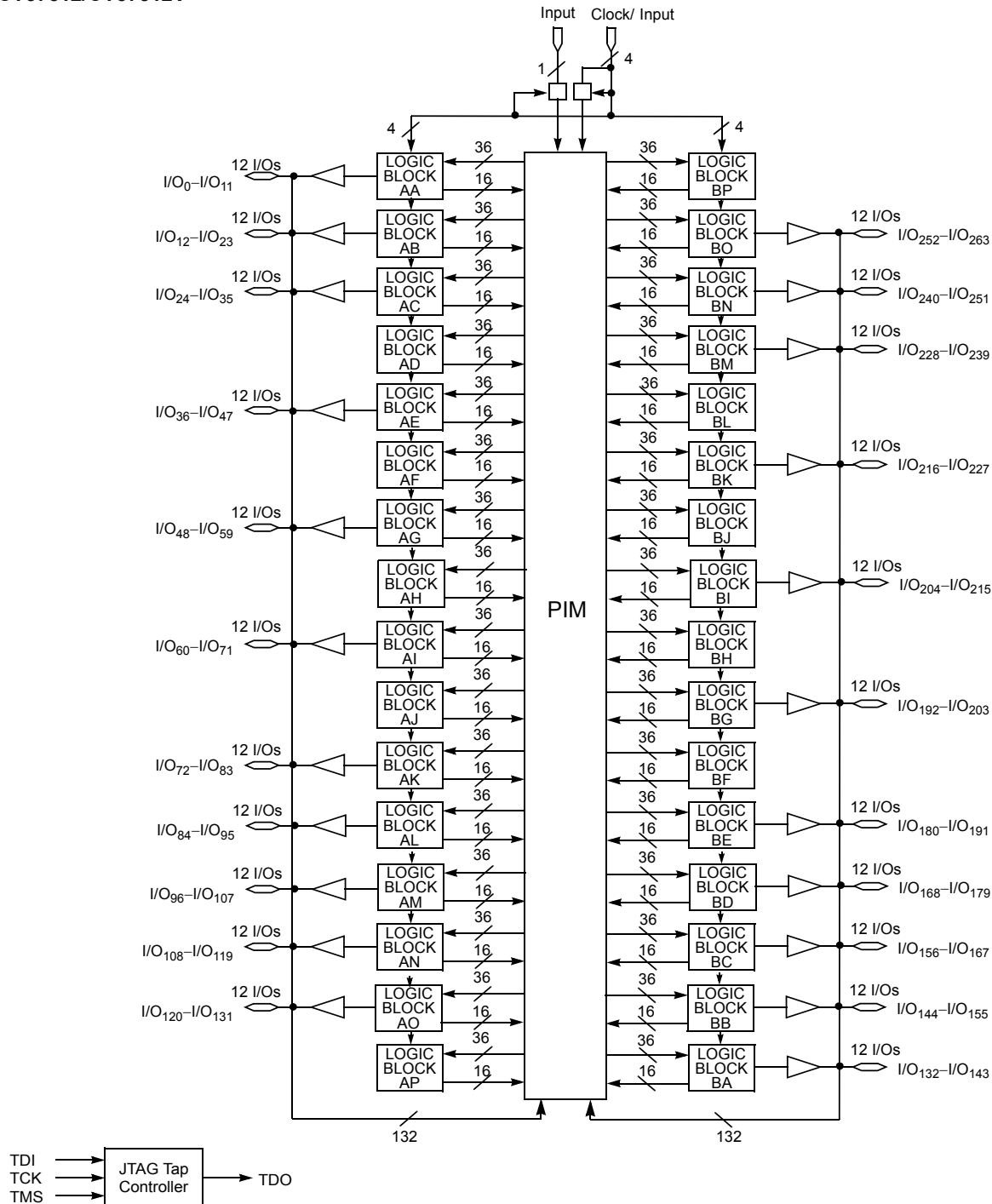
Logic Block Diagrams (continued)

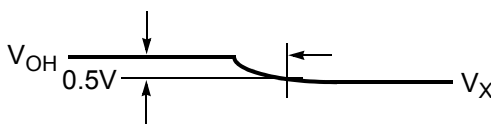
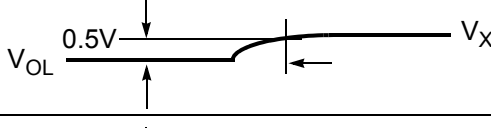
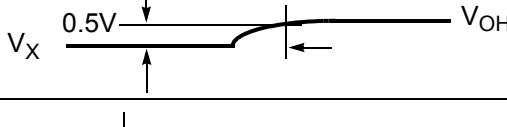
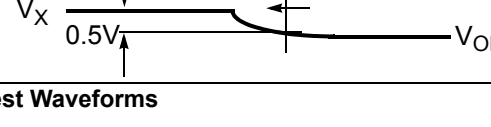
CY37256/CY37256V



Logic Block Diagrams (continued)

CY37512/CY37512V



Parameter ^[11]	V _X	Output Waveform—Measurement Level
t _{ER} (-)	1.5V	
t _{ER} (+)	2.6V	
t _{EA} (+)	1.5V	
t _{EA} (-)	V _{the}	

(d) Test Waveforms

Switching Characteristics Over the Operating Range ^[12]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t _{PD} ^[13, 14, 15]	Input to Combinatorial Output	ns
t _{PDL} ^[13, 14, 15]	Input to Output Through Transparent Input or Output Latch	ns
t _{PDLL} ^[13, 14, 15]	Input to Output Through Transparent Input and Output Latches	ns
t _{EA} ^[13, 14, 15]	Input to Output Enable	ns
t _{ER} ^[11, 13]	Input to Output Disable	ns
Input Register Parameters		
t _{WL}	Clock or Latch Enable Input LOW Time ^[8]	ns
t _{WH}	Clock or Latch Enable Input HIGH Time ^[8]	ns
t _{IS}	Input Register or Latch Set-up Time	ns
t _{IH}	Input Register or Latch Hold Time	ns
t _{CO} ^[13, 14, 15]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t _{COL} ^[13, 14, 15]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t _{CO} ^[14, 15]	Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output	ns
t _S ^[13]	Set-Up Time from Input to Sync. Clk (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	ns
t _H	Register or Latch Data Hold Time	ns
t _{CO2} ^[13, 14, 15]	Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t _{SCS} ^[13]	Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable to Output Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable (Through Logic Array)	ns
t _{SL} ^[13]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK ₀ , CLK ₁ , CLK ₂ , or CLK ₃) or Latch Enable	ns

Notes:

11. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
12. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
13. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
14. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
15. When V_{CCO} = 3.3V, add t_{3.3IO} to this spec.

Switching Characteristics Over the Operating Range ^[12]

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t _{PD} ^[13, 14, 15]		6		6.5		7.5		8.5		10		12		15		20	ns
t _{PDL} ^[13, 14, 15]		11		12.5		14.5		16		16.5		17		19		22	ns
t _{PDLL} ^[13, 14, 15]		12		13.5		15.5		17		17.5		18		20		24	ns
t _{EA} ^[13, 14, 15]		8		8.5		11		13		14		16		19		24	ns
t _{ER} ^[11, 13]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t _{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t _{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t _{IS}	2		2		2		2		2		2.5		3		4		ns
t _{IH}	2		2		2		2		2		2.5		3		4		ns
t _{ICO} ^[13, 14, 15]		11		11		11		12.5		12.5		16		19		24	ns
t _{ICOL} ^[13, 14, 15]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t _{CO} ^[14, 15]		4		4		4.5		6		6.5 ^[16]		6.5 ^[17]		8 ^[18]		10	ns
t _S ^[13]	4		4		5		5		5.5 ^[16]		6 ^[17]		8 ^[18]		10		ns
t _H	0		0		0		0		0		0		0		0		ns
t _{CO2} ^[13, 14, 15]		9.5		10		11		12		14		16		19		24	ns
t _{SCS} ^[13]	5		6		6.5		7		8 ^[16]		10		12		15		ns
t _{SL} ^[13]	7.5		7.5		8.5		9		10		12		15		15		ns
t _{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t _{COPT} ^[13, 14, 15]		7		10		10		13		13		13		15		20	ns
t _{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t _{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t _{ISPT} ^[13]	0		0		0		0		0		0		0		0		ns
t _{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t _{CO2PT} ^[13, 14, 15]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t _{ICS} ^[13]	5		6		6		7		8 ^[16]		10		12		15		ns
Operating Frequency Parameters																	
f _{MAX1}	200		167		154		143		125 ^[16]		100		83		66		MHz
f _{MAX2}	200		200		200		167		154		153 ^[17]		125 ^[18]		100		MHz
f _{MAX3}	125		125		105		91		83		80 ^[17]		62.5		50		MHz
f _{MAX4}	167		167		154		125		118		100		83		66		MHz
Reset/Preset Parameters																	
t _{RW}	8		8		8		8		10		12		15		20		ns
t _{RR} ^[13]	10		10		10		10		12		14		17		22		ns

Notes:

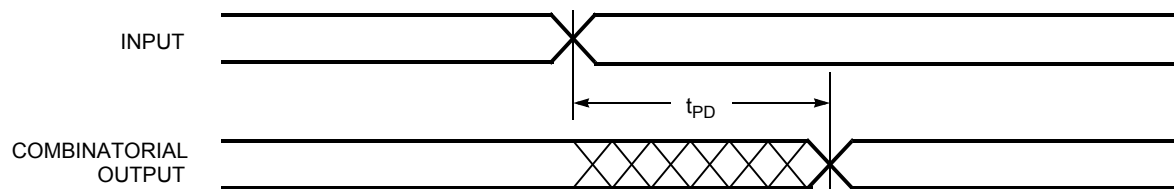
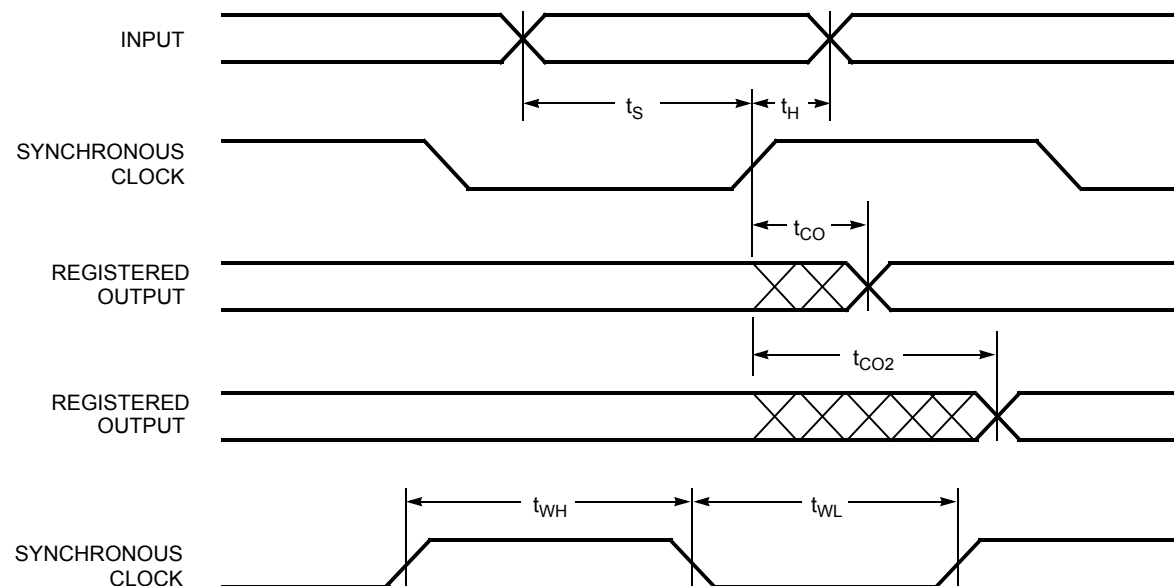
16. The following values correspond to the CY37512 and CY37384 devices: $t_{CO} = 5$ ns, $t_S = 6.5$ ns, $t_{SCS} = 8.5$ ns, $t_{ICS} = 8.5$ ns, $f_{MAX1} = 118$ MHz.

17. The following values correspond to the CY37192V and CY37256V devices: $t_{CO} = 6$ ns, $t_S = 7$ ns, $f_{MAX2} = 143$ MHz, $f_{MAX3} = 77$ MHz, and $f_{MAX4} = 100$ MHz; and for the CY37512 devices: $t_S = 7$ ns.

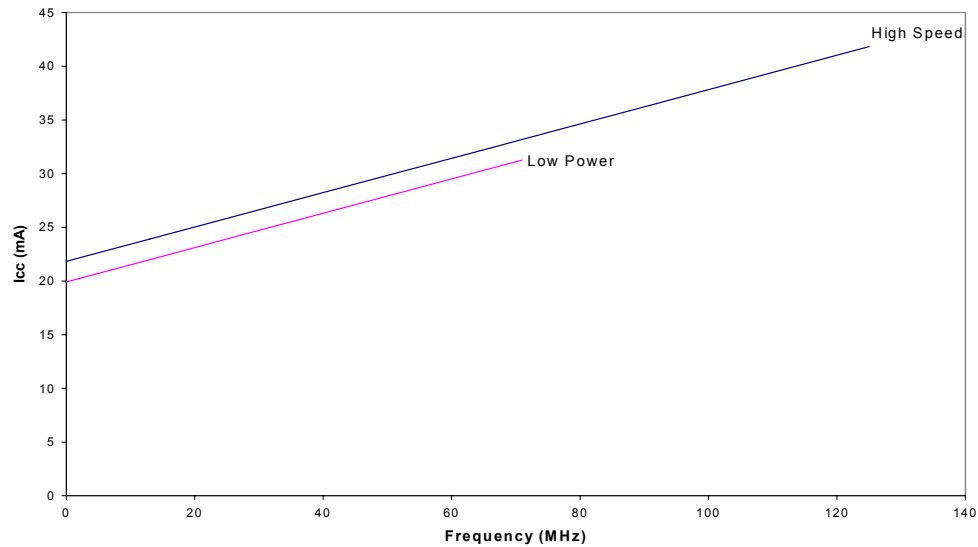
18. The following values correspond to the CY37512V and CY37384V devices: $t_{CO} = 6.5$ ns, $t_S = 9.5$ ns, and $f_{MAX2} = 105$ MHz.

Switching Characteristics Over the Operating Range (continued)^[12]

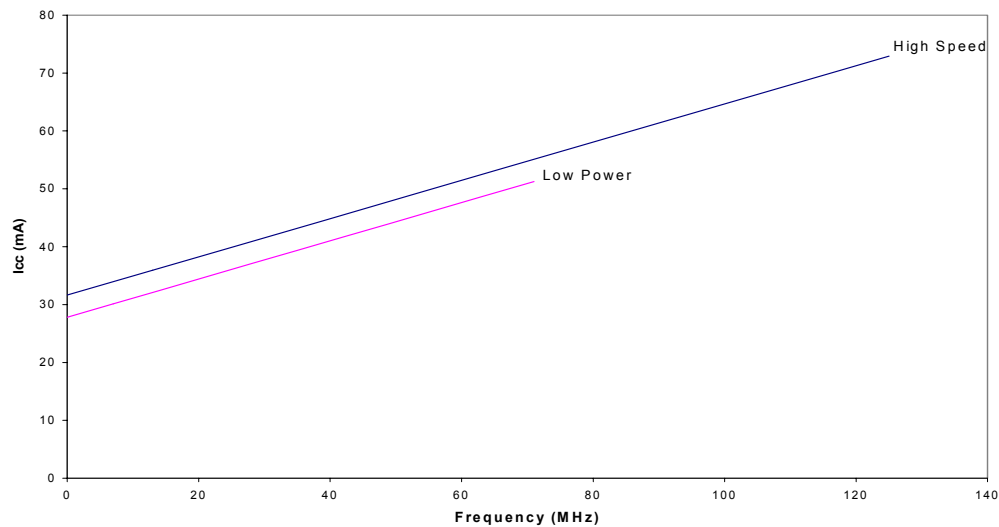
Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RO}^{[13, 14, 15]}$		12		13		13		14		15		18		21		26	ns
t_{PW}	8		8		8		8		10		12		15		20		ns
$t_{PR}^{[13]}$	10		10		10		10		12		14		17		22		ns
$t_{PO}^{[13, 14, 15]}$		12		13		13		14		15		18		21		26	ns
User Option Parameters																	
t_{LP}		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{SLEW}		3		3		3		3		3		3		3		3	ns
$t_{3.3IO}^{[19]}$		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
JTAG Timing Parameters																	
$t_{S\ JTAG}$	0		0		0		0		0		0		0		0		ns
$t_{H\ JTAG}$	20		20		20		20		20		20		20		20		ns
$t_{CO\ JTAG}$		20		20		20		20		20		20		20		20	ns
f_{JTAG}		20		20		20		20		20		20		20		20	MHz

Switching Waveforms
Combinatorial Output

Registered Output with Synchronous Clocking

Note:

19. Only applicable to the 5V devices.

Typical 3.3V Power Consumption (continued)
CY37064V


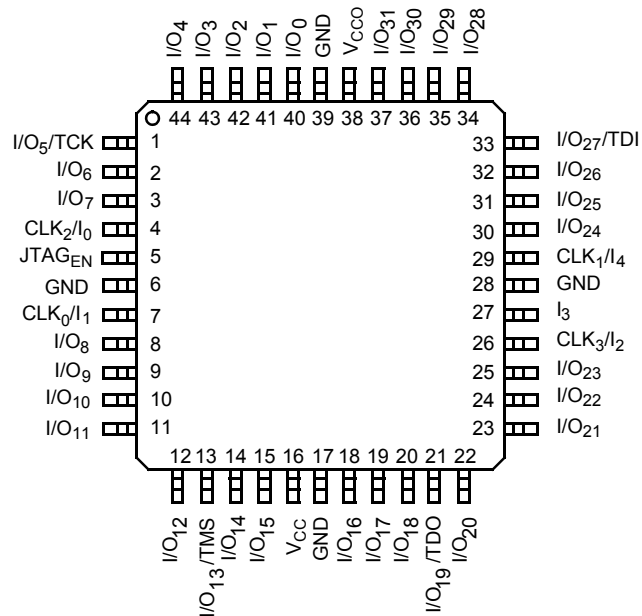
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

CY37128V


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

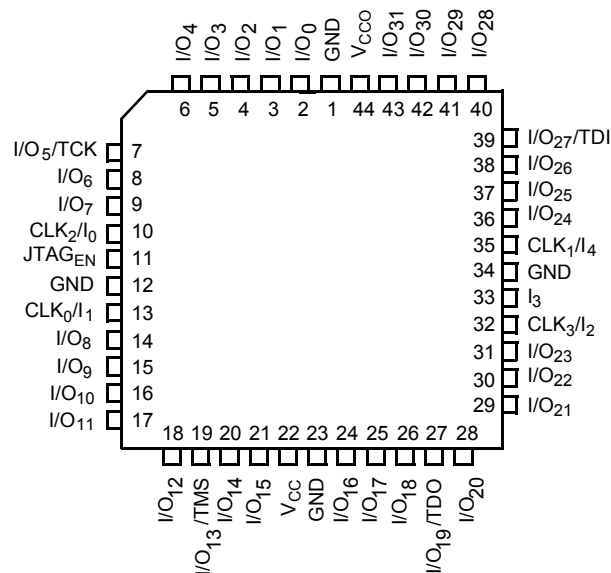
44-pin TQFP (A44)

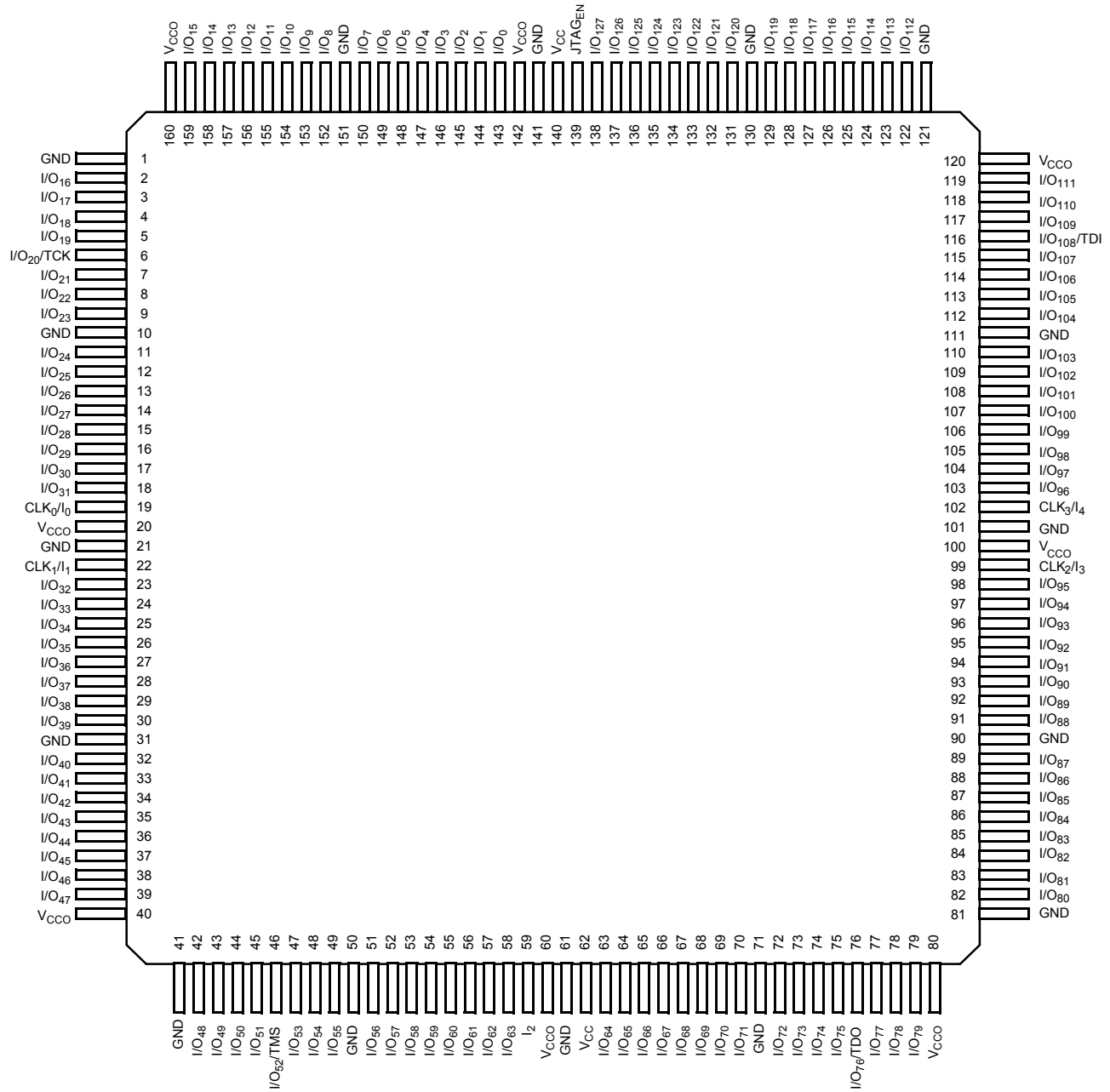
Top View



44-pin PLCC (J67) / CLCC (Y67)

Top View



Pin Configurations^[20] (continued)
**160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View**


Pin Configurations^[20] (continued)
**292-Ball PBGA (BG292)
Top View**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O ₂₁	NC	I/O ₁₆	I/O ₁₂	I/O ₉	I/O ₇	I/O ₄	I/O ₀	I/O ₁₉₀	I/O ₁₈₉	I/O ₁₈₆	I/O ₁₈₂	NC	I/O ₁₇₈	I/O ₁₇₅	NC	NC	I/O ₁₆₉	I/O ₁₆₈	A
B	I/O ₂₃	I/O ₂₀	I/O ₁₉	I/O ₁₈	I/O ₁₅	I/O ₁₁	I/O ₈	I/O ₅	I/O ₁	I/O ₁₉₁	I/O ₁₈₇	I/O ₁₈₅	I/O ₁₈₁	NC	NC	I/O ₁₇₄	I/O ₁₇₁	I/O ₁₇₀	NC	I/O ₁₆₆	B
C	NC	NC	I/O ₂₂	NC	I/O ₁₇	I/O ₁₄	I/O ₁₀	I/O ₆	I/O ₂	NC	I/O ₁₈₈	I/O ₁₈₄	I/O ₁₈₀	I/O ₁₇₉	I/O ₁₇₆	I/O ₁₇₃	I/O ₁₇₂	I/O ₁₆₇	I/O ₁₆₅	I/O ₁₆₂	C
D	I/O ₂₄	NC	NC	GND	NC	V _{CC0}	I/O ₁₃	GND	I/O ₃	NC	V _{CC}	I/O ₁₈₃	GND	I/O ₁₇₇	V _{CC0}	NC	GND	I/O ₁₆₄	TDI	I/O ₁₆₀	D
E	I/O ₂₇	I/O ₂₆	I/O ₂₅	NC													I/O ₁₆₃	I/O ₁₆₁	I/O ₁₅₉	I/O ₁₅₆	E
F	I/O ₃₀	TCK	I/O ₂₈	V _{CC0}													V _{CC0}	I/O ₁₅₈	NC	I/O ₁₅₄	F
G	I/O ₃₃	I/O ₃₂	I/O ₃₁	I/O ₂₉													I/O ₁₅₇	I/O ₁₅₅	I/O ₁₅₃	I/O ₁₅₂	G
H	I/O ₃₅	NC	I/O ₃₄	GND	GND												GND	I/O ₁₅₁	I/O ₁₅₀	I/O ₁₄₉	H
J	I/O ₃₉	I/O ₃₈	I/O ₃₇	I/O ₃₆	GND												I/O ₁₄₈	I/O ₁₄₇	I/O ₁₄₆	I/O ₁₄₅	J
K	I/O ₄₂	I/O ₄₀	I/O ₄₁	V _{CC}	GND												I/O ₁₄₄	CLK ₃ /I ₄	NC	NC	K
L	I/O ₄₃	I/O ₄₄	I/O ₄₅	I/O ₄₆	GND												V _{CC}	CLK ₂ /I ₃	I/O ₁₄₃	NC	L
M	I/O ₄₇	CLK ₀ /I ₀	CLK ₁ /I ₁	I/O ₄₈	GND												I/O ₁₃₉	I/O ₁₄₀	I/O ₁₄₁	I/O ₁₄₂	M
N	I/O ₄₉	I/O ₅₀	I/O ₅₁	GND	GND												GND	I/O ₁₃₆	I/O ₁₃₇	I/O ₁₃₈	N
P	I/O ₅₂	I/O ₅₃	I/O ₅₅	I/O ₅₈													I/O ₁₃₁	I/O ₁₃₃	I/O ₁₃₄	I/O ₁₃₅	P
R	I/O ₅₄	I/O ₅₆	I/O ₅₉	V _{CC0}													V _{CC0}	I/O ₁₃₀	NC	I/O ₁₃₂	R
T	I/O ₅₇	I/O ₆₀	I/O ₆₂	I/O ₆₅													I/O ₁₂₄	I/O ₁₂₇	I/O ₁₂₈	I/O ₁₂₉	T
U	I/O ₆₁	I/O ₆₃	I/O ₆₆	GND	I/O ₇₆	V _{CC0}	I/O ₈₂	GND	I/O ₉₁	V _{CC}	I/O ₉₈	I/O ₁₀₂	GND	I/O ₁₁₂	V _{CC0}	NC	GND	I/O ₁₂₃	I/O ₁₂₂	I/O ₁₂₆	U
V	I/O ₆₄	I/O ₆₇	I/O ₆₉	I/O ₇₅	I/O ₇₈	I/O ₈₁	I/O ₈₅	I/O ₈₈	I/O ₉₂	I ₂	I/O ₉₇	I/O ₁₀₁	I/O ₁₀₅	I/O ₁₀₉	I/O ₁₁₃	TD0	I/O ₁₁₄	I/O ₁₁₇	I/O ₁₂₁	I/O ₁₂₅	V
W	I/O ₆₈	I/O ₇₀	I/O ₇₂	I/O ₇₄	I/O ₇₉	I/O ₈₃	I/O ₈₆	I/O ₈₉	I/O ₉₃	I/O ₉₅	I/O ₉₆	I/O ₁₀₀	I/O ₁₀₄	I/O ₁₀₇	I/O ₁₁₀	NC	NC	I/O ₁₁₅	I/O ₁₁₈	I/O ₁₂₀	W
Y	I/O ₇₁	I/O ₇₃	I/O ₇₇	TMS	I/O ₈₀	I/O ₈₄	I/O ₈₇	I/O ₉₀	I/O ₉₄	NC	NC	I/O ₉₉	I/O ₁₀₃	I/O ₁₀₆	I/O ₁₀₈	I/O ₁₁₁	NC	NC	I/O ₁₁₆	I/O ₁₁₉	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Pin Configurations^[20] (continued)
256-Ball Fine-Pitch BGA (BB256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	I/O ₂₆	I/O ₂₄	I/O ₂₀	V _{CC}	I/O ₁₁	GND	GND	I/O ₁₈₆	V _{CC}	I/O ₁₇₇	I/O ₁₇₂	I/O ₁₆₇	GND	GND
B	GND	I/O ₂₇	I/O ₂₅	I/O ₂₃	I/O ₁₉	I/O ₁₅	I/O ₁₀	GND	GND	I/O ₁₈₅	I/O ₁₈₁	I/O ₁₇₆	I/O ₁₇₁	I/O ₁₆₆	I/O ₁₆₅	GND
C	I/O ₂₉	I/O ₂₈	NC	I/O ₂₂	I/O ₁₈	I/O ₁₄	I/O ₉	I/O ₄	I/O ₁₉₁	I/O ₁₈₄	I/O ₁₈₀	I/O ₁₇₅	I/O ₁₇₀	NC	I/O ₁₆₃	I/O ₁₆₄
D	I/O ₃₂	I/O ₃₁	I/O ₃₀	NC	I/O ₁₇	I/O ₁₃	I/O ₈	I/O ₃	I/O ₁₉₀	I/O ₁₈₃	I/O ₁₇₉	I/O ₁₇₄	I/O ₁₆₉	I/O ₁₆₀	I/O ₁₆₁	I/O ₁₆₂
E	I/O ₃₅	I/O ₃₄	I/O ₃₃	I/O ₂₁	I/O ₁₆	I/O ₁₂	I/O ₇	I/O ₂	I/O ₁₈₉	V _{CC}	I/O ₁₇₈	I/O ₁₇₃	I/O ₁₆₈	I/O ₁₅₇	I/O ₁₅₈	I/O ₁₅₉
F	V _{CC}	I/O ₃₈	I/O ₃₇	I/O ₃₆	TCK	V _{CC}	I/O ₆	I/O ₁	I/O ₁₈₈	I/O ₁₈₂	V _{CC}	TDI	I/O ₁₅₄	I/O ₁₅₅	I/O ₁₅₆	V _{CC}
G	I/O ₄₃	I/O ₄₂	I/O ₄₁	I/O ₄₀	V _{CC}	I/O ₃₉	I/O ₅	I/O ₀	I/O ₁₈₇	I/O ₁₄₈	I/O ₁₄₉	CLK ₃ /I ₄	I/O ₁₅₀	I/O ₁₅₁	I/O ₁₅₂	I/O ₁₅₃
H	GND	GND	I/O ₄₇	I/O ₄₆	CLK ₀ /I ₀	I/O ₄₅	I/O ₄₄	GND	GND	I/O ₁₄₄	I/O ₁₄₅	CLK ₂ /I ₃	I/O ₁₄₆	I/O ₁₄₇	GND	GND
J	GND	GND	I/O ₅₁	I/O ₅₀	NC	I/O ₄₉	I/O ₄₈	GND	GND	I/O ₁₄₀	I/O ₁₄₁	I ₂	I/O ₁₄₂	I/O ₁₄₃	GND	GND
K	I/O ₅₇	I/O ₅₆	I/O ₅₅	I/O ₅₄	CLK ₁ /I ₁	I/O ₅₃	I/O ₅₂	I/O ₉₁	I/O ₉₆	I/O ₁₀₁	I/O ₁₃₅	V _{CC}	I/O ₁₃₆	I/O ₁₃₇	I/O ₁₃₈	I/O ₁₃₉
L	V _{CC}	I/O ₆₀	I/O ₅₉	I/O ₅₈	TMS	V _{CC}	I/O ₈₆	I/O ₉₂	I/O ₉₇	I/O ₁₀₂	V _{CC}	TDO	I/O ₁₃₂	I/O ₁₃₃	I/O ₁₃₄	V _{CC}
M	I/O ₆₃	I/O ₆₂	I/O ₆₁	I/O ₇₂	I/O ₇₇	I/O ₈₂	V _{CC}	I/O ₉₃	I/O ₉₈	I/O ₁₀₃	I/O ₁₀₈	I/O ₁₁₂	I/O ₁₁₇	I/O ₁₂₉	I/O ₁₃₀	I/O ₁₃₁
N	I/O ₆₆	I/O ₆₅	I/O ₆₄	I/O ₇₃	I/O ₇₈	I/O ₈₃	I/O ₈₇	I/O ₉₄	I/O ₉₉	I/O ₁₀₄	I/O ₁₀₉	I/O ₁₁₃	NC	I/O ₁₂₆	I/O ₁₂₇	I/O ₁₂₈
P	I/O ₆₈	I/O ₆₇	NC	I/O ₇₄	I/O ₇₉	I/O ₈₄	I/O ₈₈	I/O ₉₅	I/O ₁₀₀	I/O ₁₀₅	I/O ₁₁₀	I/O ₁₁₄	I/O ₁₁₈	NC	I/O ₁₂₄	I/O ₁₂₅
R	GND	I/O ₆₉	I/O ₇₀	I/O ₇₅	I/O ₈₀	I/O ₈₅	I/O ₈₉	GND	GND	I/O ₁₀₆	I/O ₁₁₁	I/O ₁₁₅	I/O ₁₁₉	I/O ₁₂₁	I/O ₁₂₃	GND
T	GND	GND	I/O ₇₁	I/O ₇₆	I/O ₈₁	V _{CC}	I/O ₉₀	GND	GND	I/O ₁₀₇	V _{CC}	I/O ₁₁₆	I/O ₁₂₀	I/O ₁₂₂	GND	GND

Pin Configurations^[20] (continued)
388-Lead PBGA (BG388)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	GND	I/O ₁₉	I/O ₁₅	I/O ₁₃	I/O ₃₄	I/O ₃₁	I/O ₂₈	I/O ₂₅	I/O ₁₀	I/O ₇	I/O ₄	I/O ₁	I/O ₂₆₃	I/O ₂₆₀	I/O ₂₅₇	I/O ₂₅₄	I/O ₂₃₉	I/O ₂₃₇	I/O ₂₃₂	I/O ₂₂₉	I/O ₂₅₀	I/O ₂₄₈	I/O ₂₄₄	GND	GND
B	GND	NC	I/O ₁₈	I/O ₁₇	I/O ₁₄	I/O ₃₅	I/O ₃₂	I/O ₂₉	I/O ₂₆	I/O ₁₁	I/O ₈	I/O ₅	I/O ₂	V _{CC}	I/O ₂₆₁	I/O ₂₅₈	I/O ₂₅₅	I/O ₂₅₂	I/O ₂₃₄	I/O ₂₃₁	I/O ₂₂₈	I/O ₂₄₉	I/O ₂₄₆	I/O ₂₄₅	I/O ₂₄₀	GND
C	I/O ₂₃	I/O ₃₈	I/O ₃₇	I/O ₁₆	I/O ₁₂	I/O ₃₃	I/O ₃₀	I/O ₂₇	I/O ₂₄	I/O ₉	I/O ₆	I/O ₃	I/O ₀	I/O ₂₆₂	I/O ₂₅₉	I/O ₂₅₆	I/O ₂₅₃	I/O ₂₃₈	I/O ₂₃₅	I/O ₂₃₃	I/O ₂₃₀	I/O ₂₅₁	I/O ₂₄₇	I/O ₂₂₅	I/O ₂₂₄	I/O ₂₂₇
D	I/O ₃₉	I/O ₄₀	I/O ₃₆	NC	NC	I/O ₂₁	I/O ₂₀	V _{CCO}	V _{CCO}	NC	GND	GND	V _{CCO}	V _{CCO}	GND	GND	NC	V _{CCO}	V _{CCO}	I/O ₂₃₆	I/O ₂₄₃	NC	NC	I/O ₂₂₆	I/O ₂₂₂	I/O ₂₂₃
E	I/O ₄₂	TCK	I/O ₄₁	NC																			NC	TDI	I/O ₂₂₁	I/O ₂₂₀
F	I/O ₄₅	I/O ₄₄	I/O ₄₃	I/O ₂₂																			I/O ₂₄₂	I/O ₂₁₉	I/O ₂₁₈	I/O ₂₁₇
G	I/O ₄₈	I/O ₄₇	I/O ₄₆	I/O ₆₃																			I/O ₂₄₁	I/O ₂₁₆	I/O ₂₁₅	I/O ₂₁₄
H	I/O ₄₉	I/O ₅₀	I/O ₅₁	V _{CCO}																			V _{CCO}	I/O ₂₁₁	I/O ₂₁₂	I/O ₂₁₃
J	I/O ₅₂	I/O ₅₃	I/O ₅₄	V _{CCO}																			V _{CCO}	I/O ₂₀₈	I/O ₂₀₉	I/O ₂₁₀
K	I/O ₅₅	I/O ₅₆	I/O ₅₇	NC																			NC	I/O ₂₀₅	I/O ₂₀₆	I/O ₂₀₇
L	I/O	I/O ₅₉	I/O ₅₈	GND																			GND	I/O ₂₀₄	I/O	I/O ₁₉₇
M	I/O ₆₁	I/O ₆₀	I/O	GND																			GND	I/O	I/O ₂₀₃	I/O ₂₀₂
N	I/O ₆₄	V _{CC}	I/O ₆₂	V _{CCO}																			V _{CCO}	I/O ₂₀₁	I/O ₂₀₀	I/O ₁₉₉
P	I/O ₆₅	I/O ₆₆	I/O ₆₇	V _{CCO}																			V _{CCO}	I/O ₁₉₆	V _{CC}	I/O ₁₉₈
R	I/O ₆₈	I/O ₆₉	I/O ₇₀	GND																			GND	I/O ₁₉₃	I/O ₁₉₄	I/O ₁₉₅
T	I/O ₇₁	I/O ₈₄	I/O ₈₅	GND																			GND	I/O ₁₇₈	I/O ₁₇₉	I/O ₁₉₂
U	I/O ₈₈	I/O ₈₇	I/O ₈₆	NC																			NC	I/O ₁₇₇	I/O ₁₇₆	I/O ₁₇₅
V	I/O ₉₁	I/O ₉₀	I/O ₈₉	V _{CCO}																			V _{CCO}	I/O ₁₇₄	I/O ₁₇₃	I/O ₁₇₂
W	I/O ₉₄	I/O ₉₃	I/O ₉₂	V _{CCO}																			V _{CCO}	I/O ₁₇₁	I/O ₁₇₀	I/O ₁₆₉
Y	I/O ₉₅	I/O ₇₂	I/O ₇₃	I/O ₁₁₀																			I/O ₁₅₃	I/O ₁₉₀	I/O ₁₉₁	I/O ₁₆₈
AA	I/O ₇₄	I/O ₇₅	I/O ₇₆	I/O ₁₁₁																			I/O ₁₅₂	I/O ₁₈₇	I/O ₁₈₈	I/O ₁₈₉
AB	I/O ₇₇	I/O ₇₈	I/O ₇₉	NC																			NC	I/O ₁₈₄	I/O ₁₈₅	I/O ₁₈₆
AC	I/O ₈₁	I/O ₈₀	I/O ₁₀₈	NC	NC	I/O ₁₁₂	I/O ₁₁₃	V _{CCO}	V _{CCO}	NC	GND	GND	V _{CCO}	V _{CCO}	GND	GND	NC	V _{CCO}	V _{CCO}	I/O ₁₅₀	I/O ₁₅₁	NC	NC	I/O ₁₅₅	I/O ₁₈₃	I/O ₁₈₂
AD	I/O ₁₀₉	I/O ₈₂	I/O ₈₃	I/O ₁₁₇	I/O ₉₇	I/O ₁₀₀	I/O ₁₀₂	I/O ₁₀₅	I/O ₁₂₀	I/O ₁₂₃	I/O ₁₂₆	I/O ₁₂₉	I/O	I/O ₁₃₃	I/O ₁₃₆	I/O ₁₃₉	I/O ₁₄₂	I/O ₁₅₇	I/O ₁₅₉	I/O ₁₆₁	I/O ₁₆₃	I/O ₁₆₆	I/O ₁₄₆	I/O ₁₈₀	I/O ₁₈₁	I/O ₁₅₄
AE	GND	NC	I/O ₁₁₅	I/O ₁₁₆	I/O ₁₁₉	I/O ₉₈	I/O ₁₀₁	I/O ₁₀₃	I/O ₁₀₆	I/O ₁₂₁	I/O ₁₂₄	I/O ₁₂₇	V _{CC}	I/O ₁₃₀	I/O ₁₃₄	I/O ₁₃₇	I/O ₁₄₀	I/O ₁₄₃	I/O ₁₆₀	I/O ₁₆₂	I/O ₁₆₅	I/O ₁₄₄	I/O ₁₄₇	I/O ₁₄₈	NC	GND
AF	GND	GND	I/O ₁₁₄	I/O ₁₁₈	I/O ₉₆	I/O ₉₉	TMS	I/O ₁₀₄	I/O ₁₀₇	I/O ₁₂₂	I/O ₁₂₅	I/O ₁₂₈	I/O ₁₃₁	I/O ₁₃₂	I/O ₁₃₅	I/O ₁₃₈	I/O ₁₄₁	I/O ₁₅₆	I/O ₁₅₈	TDO	I/O ₁₆₄	I/O ₁₆₇	I/O ₁₄₅	I/O ₁₄₉	GND	GND

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	154	CY37256P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-154AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-154NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-154BGC	BG292	292-Ball Plastic Ball Grid Array	
	125	CY37256P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952302QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
	83	CY37256P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952301QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	125	CY37384P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
	83	CY37384P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	

5.0V Ordering Information (continued)

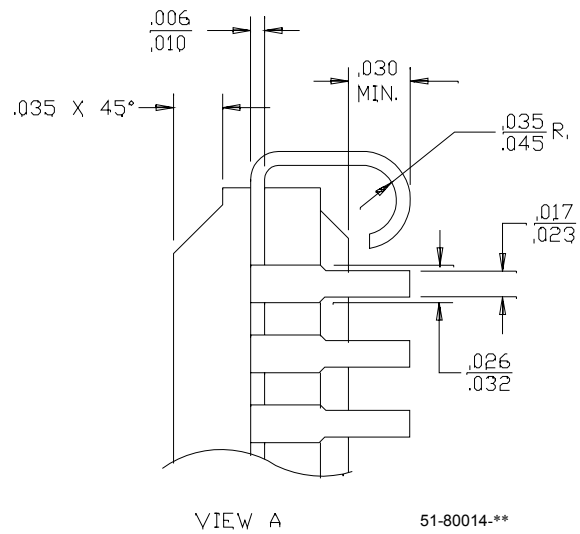
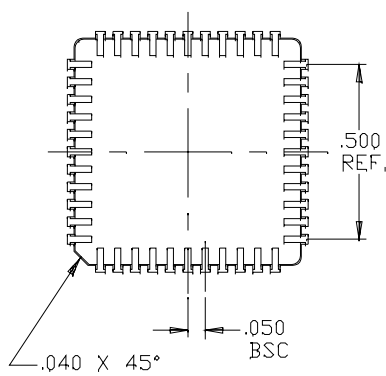
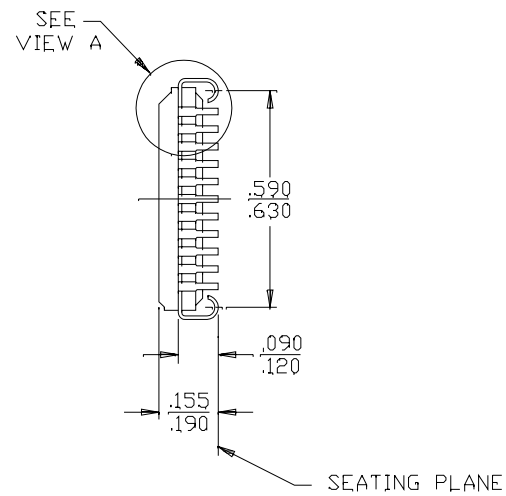
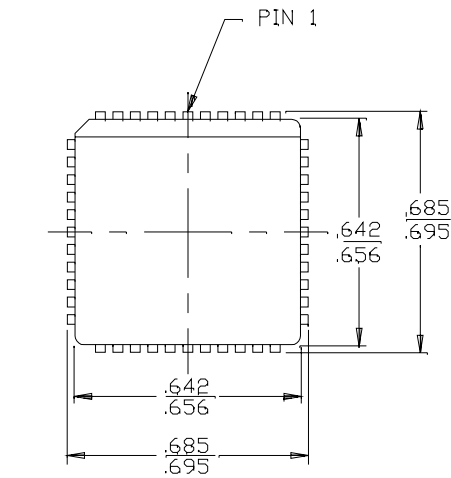
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-125BGC	BG388	388-Ball Plastic Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

3.3V Ordering Information

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-143BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAI	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP44-100JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	

Package Diagrams (continued)

44-Lead Ceramic Leaded Chip Carrier Y67



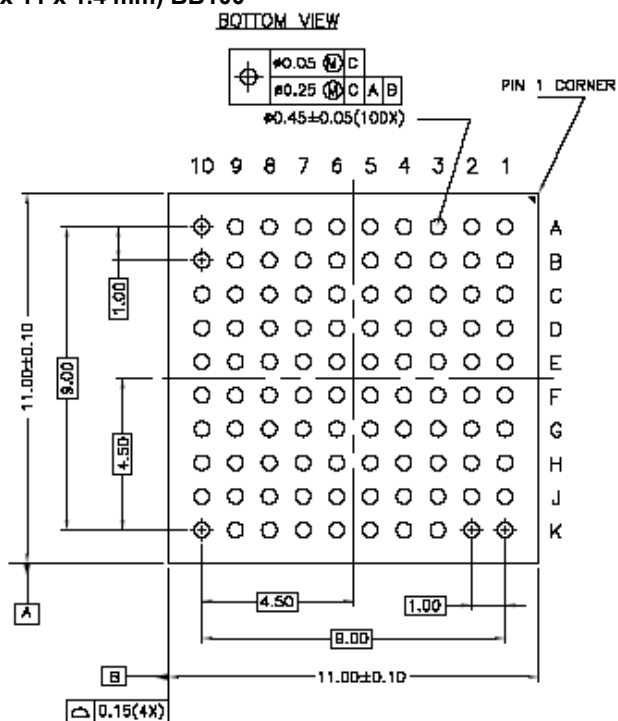
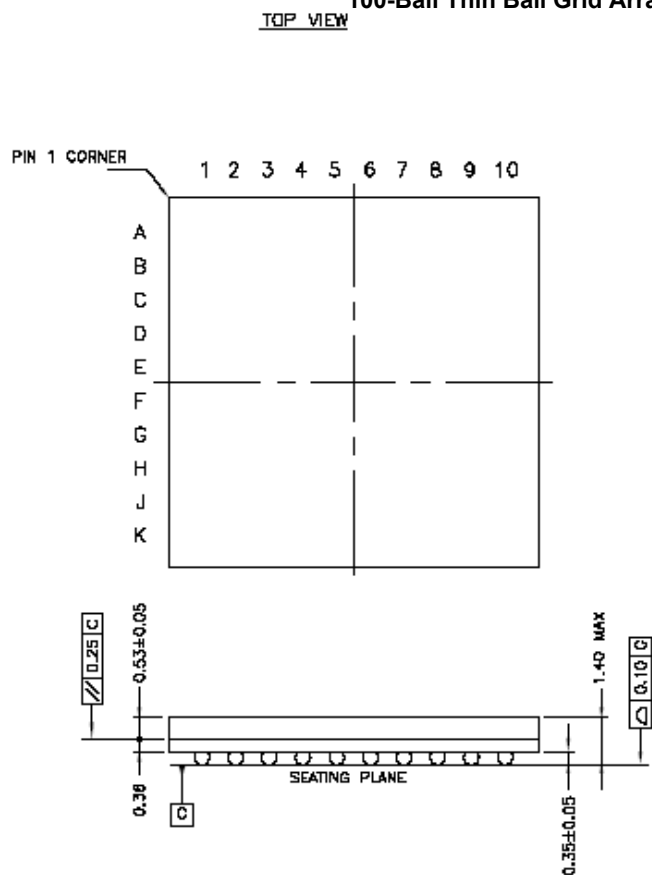




Ultra37000 CPLD Family

Package Diagrams (continued)

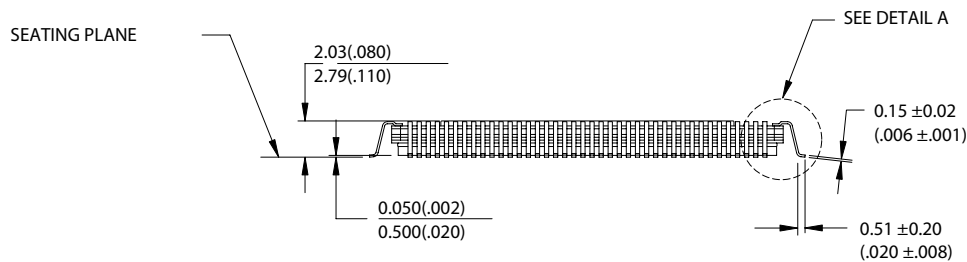
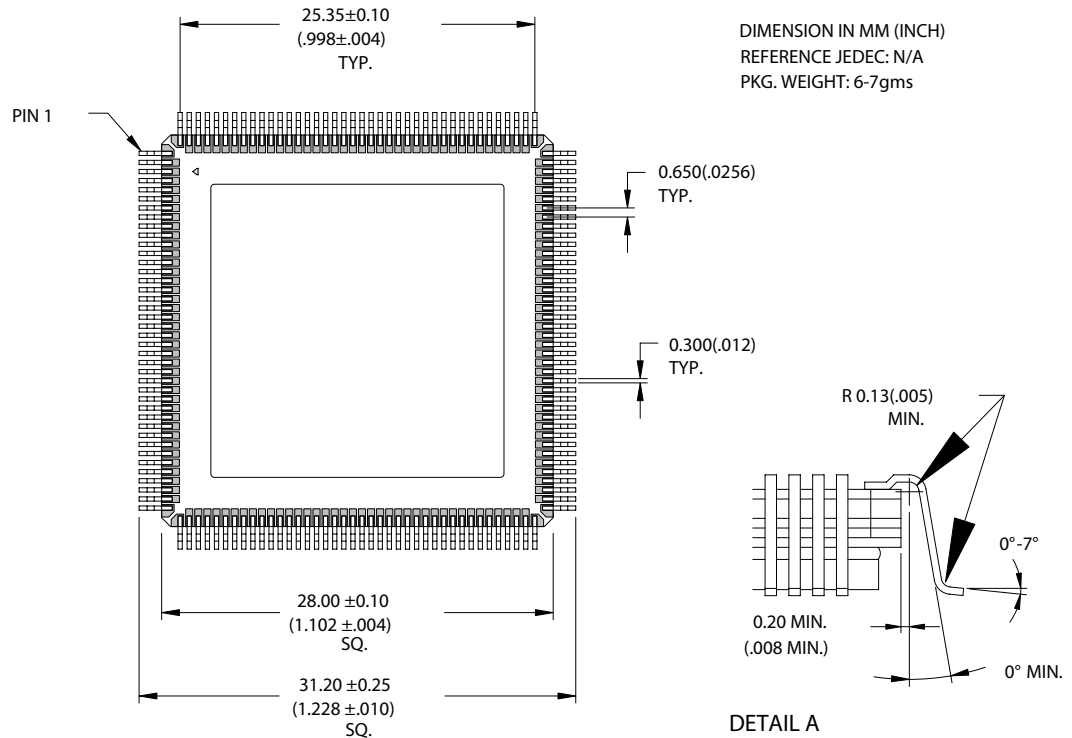
100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



51-85107-*B

Package Diagrams (continued)

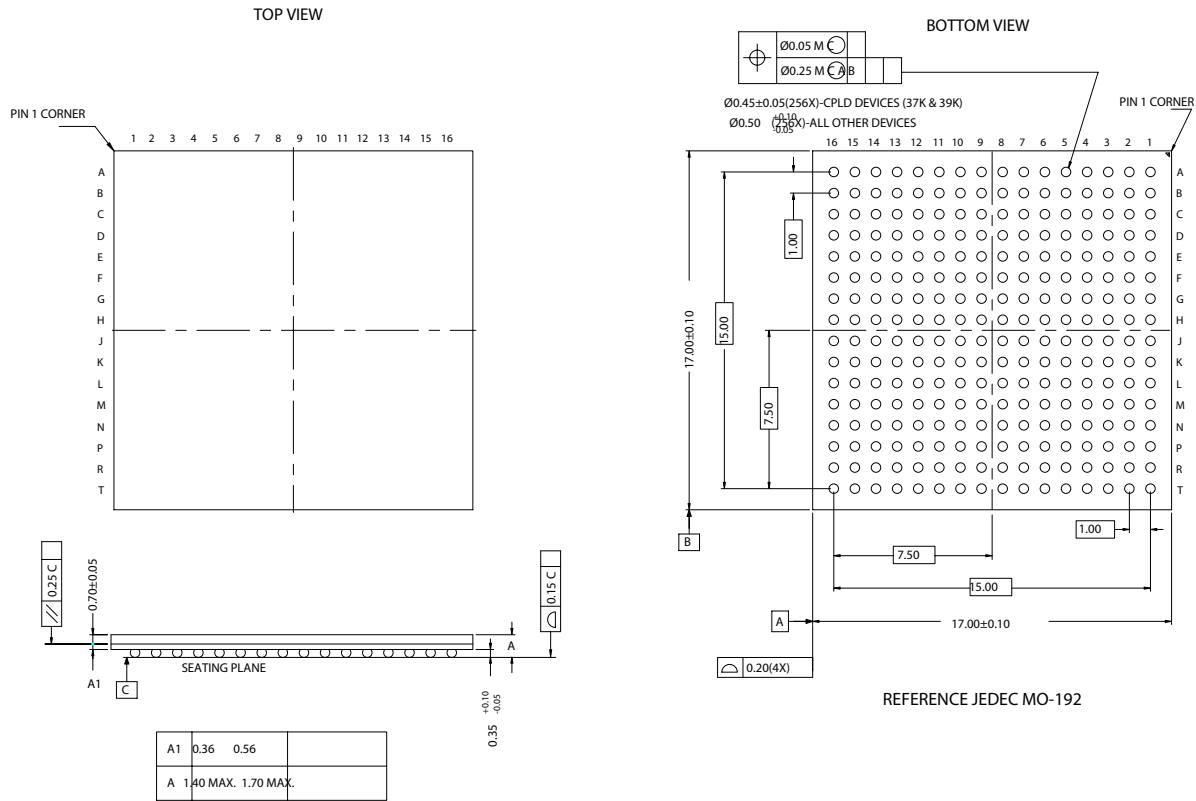
160-Lead Ceramic Quad Flatpack (Cavity Up) U162



51-80106-*A

Package Diagrams (continued)

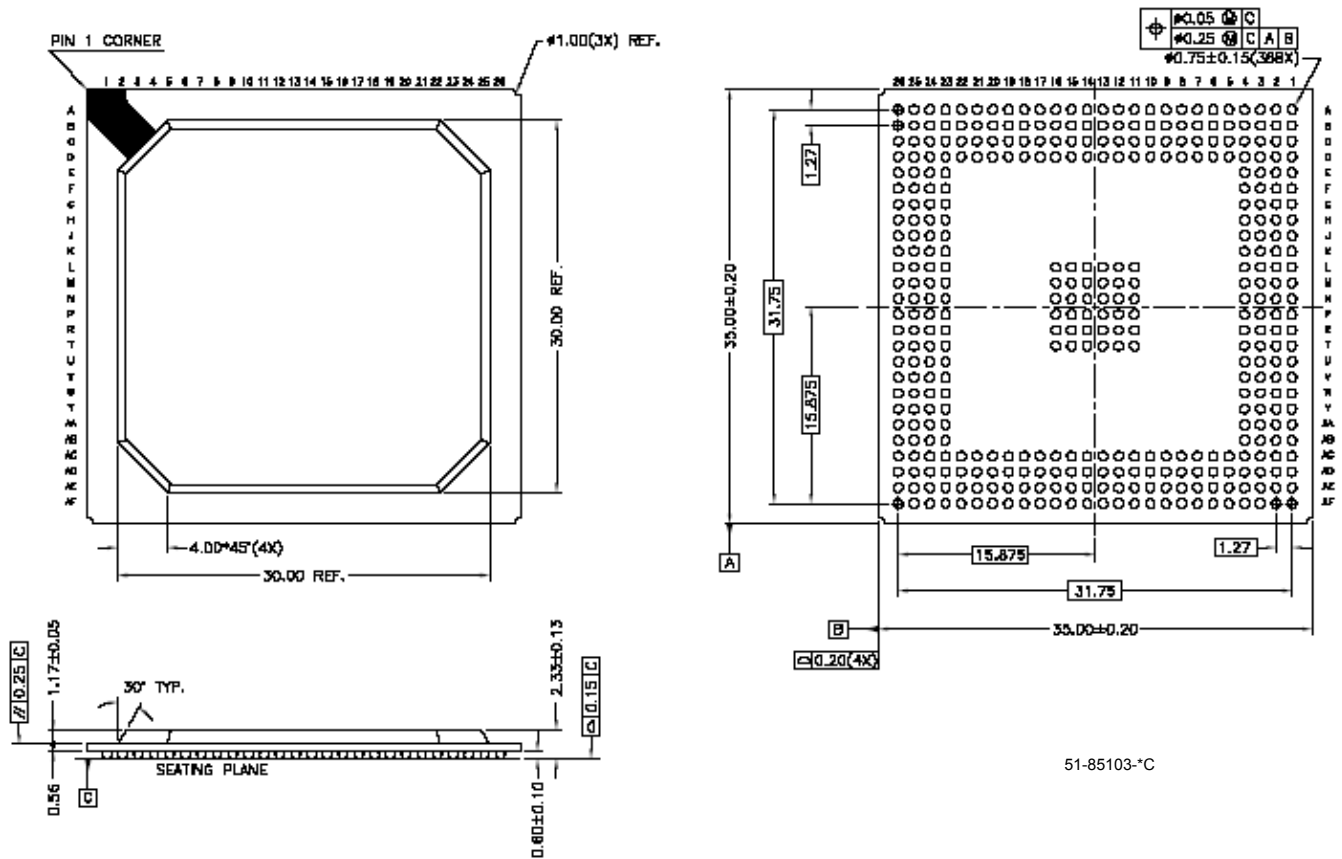
256-Ball FBGA (17 x 17 mm) BB256



51-85108-7F

Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388



51-85103-°C

Document History Page

Document Title: Ultra37000 CPLD Family 5V, 3.3V, ISR™ High-Performance CPLDs Document Number: 38-03007				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106272	04/18/01	SZV	Change from Spec number: 38-00475 to 38-03007
*A	124942	03/21/03	OOR	Updated 3.3V V _{CC} requirements for –144 speeds Added an Addendum
*B	126262	05/09/03	TEH	Changed pinout for CY37128V BB100 package
*C	128125	07/16/03	HOM	Obsoleted following 3.3V PLCC packaged devices: CY37032VP44-143JC CY37032VP44-100JC CY37032VP44-100JI CY37064VP44-143JC CY37064VP84-143JC CY37064VP44-100JC CY37064VP84-100JC CY37064VP44-100JI CY37064VP84-100JI CY37128VP84-125JC CY37128VP84-83JC CY37128VP84-83JI
*D	282709	See ECN	YDT	Changed package diagrams and labels for consistency Added Lead (Pb)-free logo on first page, as well as a note in Features Added Lead (Pb)-free package diagram labels Added Lead-free Parts to Ordering Information CY37032P44-200AXC, CY37032P44-200JXC, CY37032P44-154AXI, CY37032P44-154JXI, CY37032P44-125AXC, CY37032P44-125JXC, CY37064P44-200AXC, CY37064P44-200JXC, CY37064P100-200AXC, CY37064P44-154AXI, CY37064P44-154JXI, CY37064P44-125AXC, CY37064P44-125JXC, CY37064P100-125AXC, CY37064P44-125AXI, CY37064P100-125AXI, CY37128P84-167JXC, CY37128P100-167AXC, CY37128P160-167AXC, CY37128P84-125JXC, CY37128P100-125AXC, CY37128P160-125AXC, CY37128P84-125JXI, CY37128P100-125AXI, CY37128P160-125AXI, CY37128P84-100JXC, CY37128P100-100AXC, CY37128P160-100AXC, CY37128P100-100AXI, CY37192P160-154AXC, CY37192P160-125AXC, CY37192P160-125AXI, CY37192P160-83AXC, CY37192P160-83AXI, CY37256P160-154AXC, CY37256P160-125AXC, CY37256P160-125AXI, CY37256P160-83AXC, CY37256P160-83AXI, CY37032VP44-143AXC, CY37032VP44-100AXC, CY37032VP44-100AXI, CY37032VP44-100JXI, CY37064VP44-143AXC, CY37064VP100-143AXC, CY37064VP44-100AXC, CY37064VP100-100AXC, CY37064VP44-100AXI, CY37064VP100-100AXI, CY37128VP100-125AXC, CY37128VP160-125AXC, CY37128VP160-125AXI, CY37128VP100-83AXC, CY37128VP160-83AXC, CY37128VP100-83AXI, CY37128VP160-83AXI, CY37192VP160-100AXC, CY37192VP160-66AXC, CY37256VP160-100AXC, CY37256VP160-100AXI, CY37256VP160-66AXC
*E	321635	See ECN	PCX	Added Package Diagram BG292 Updated all PBGA package type information (BG292 & BG388)