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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	69
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37128vp100-83axi

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	388-Lead PBGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83

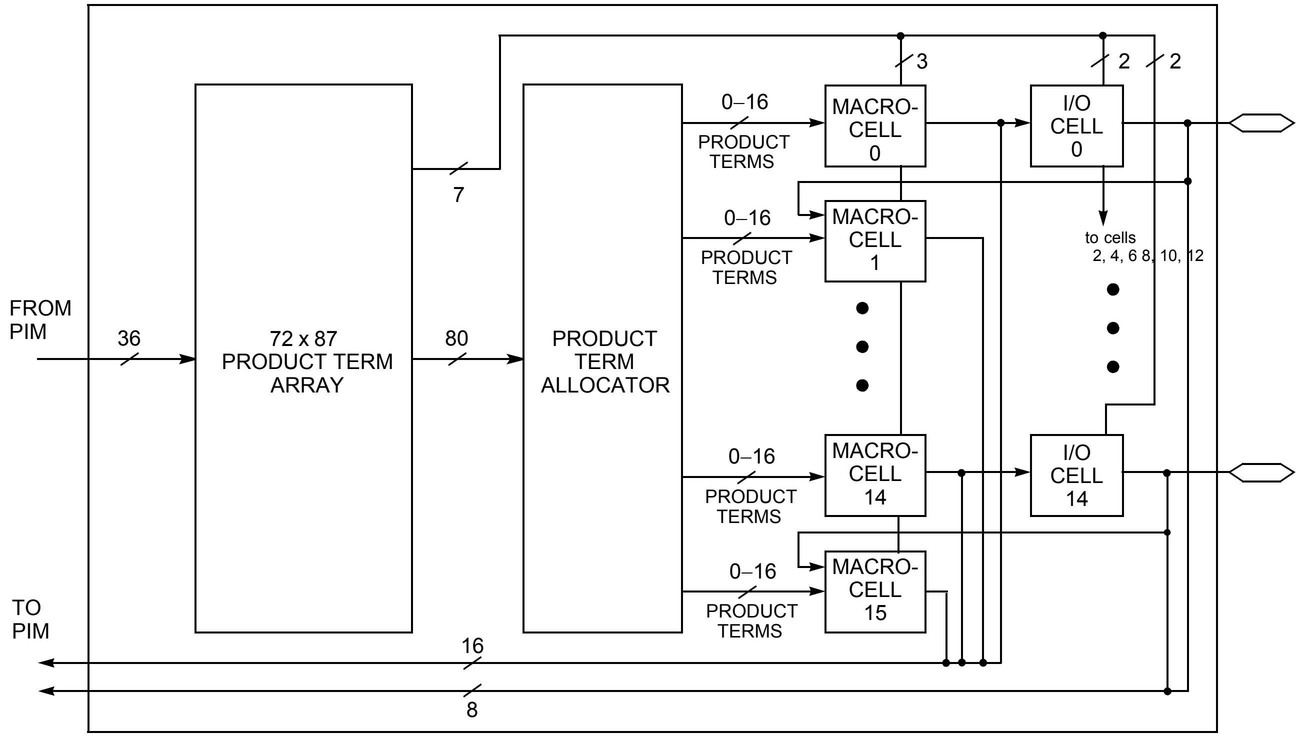


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

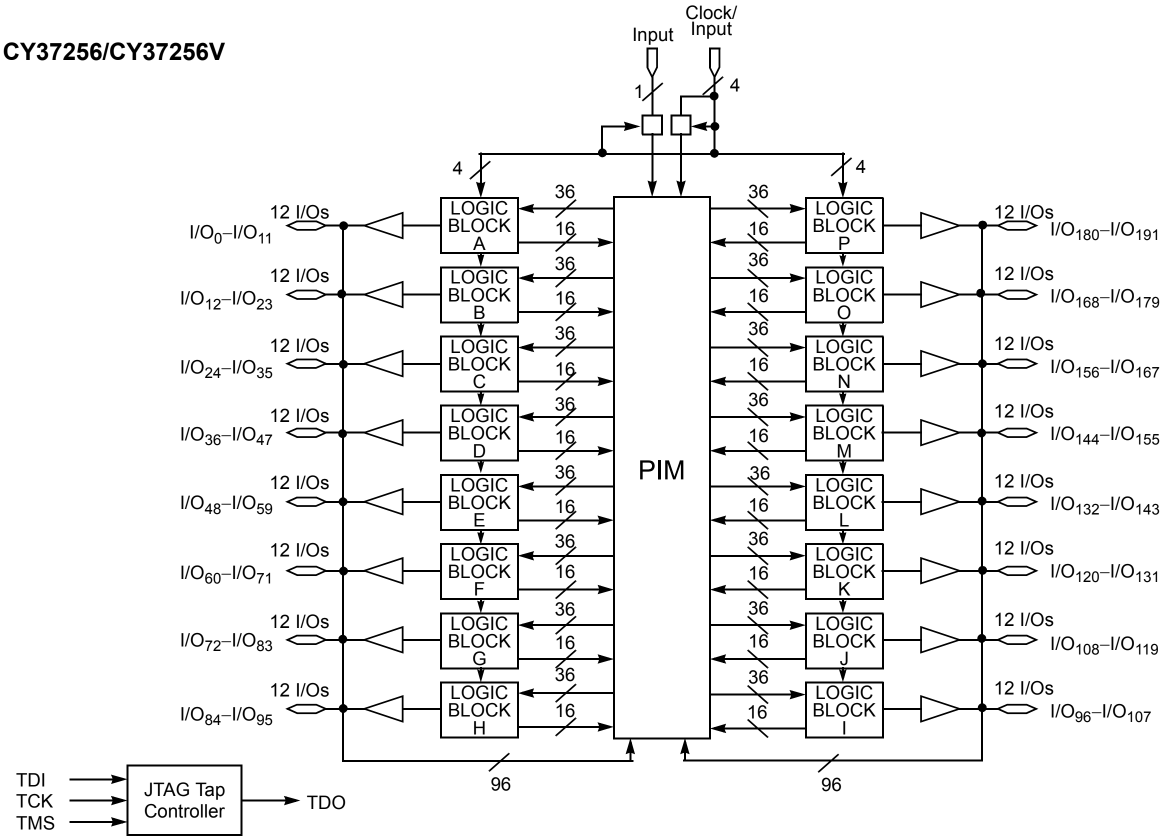
Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

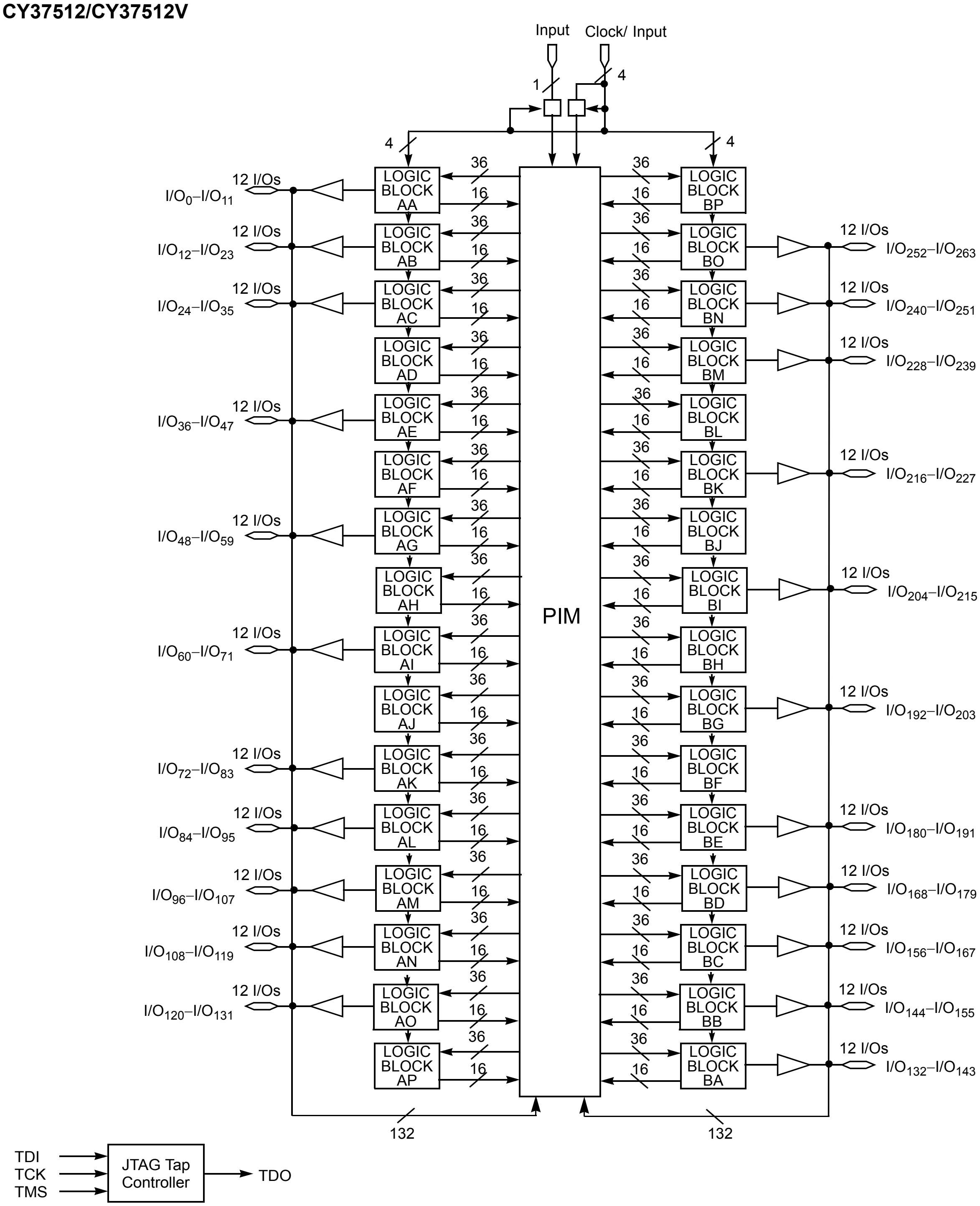
Logic Block Diagrams (continued)

CY37256/CY37256V



Logic Block Diagrams (continued)

CY37512/CY37512V



Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

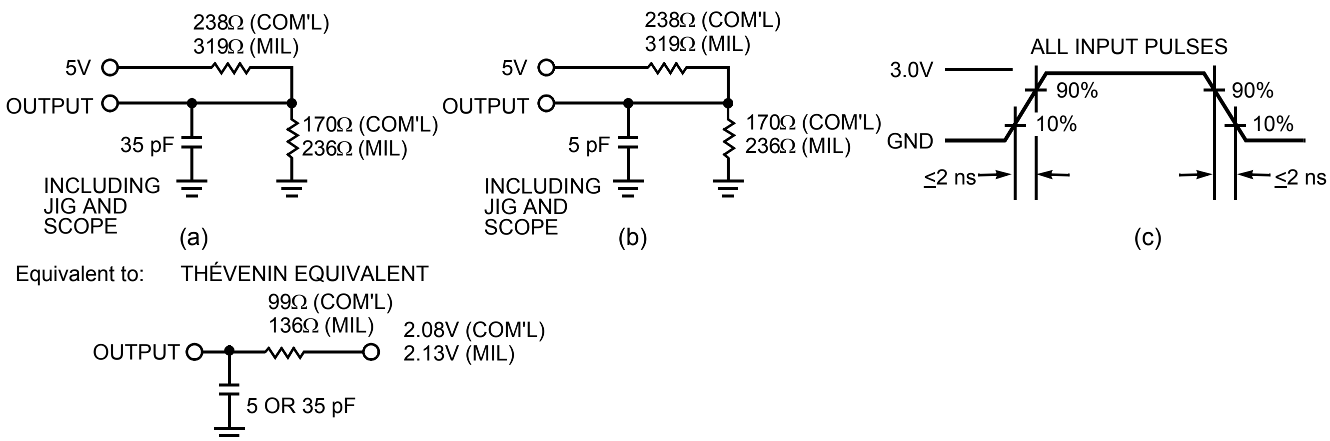
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

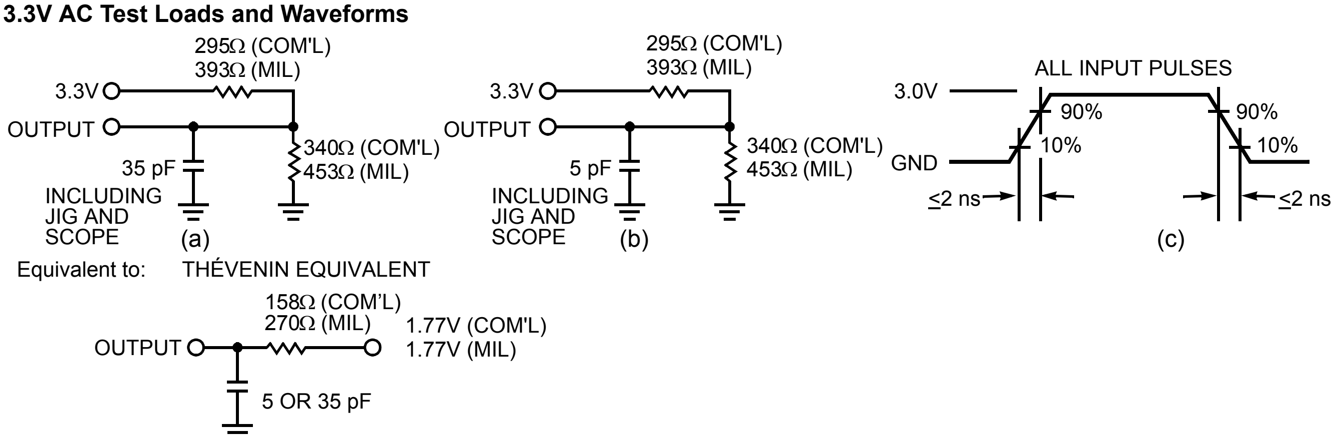
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Characteristics

5.0V AC Test Loads and Waveforms

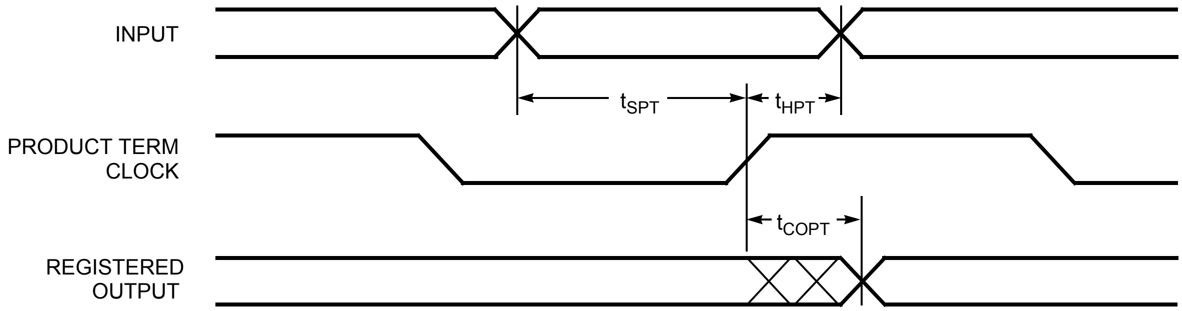


3.3V AC Test Loads and Waveforms

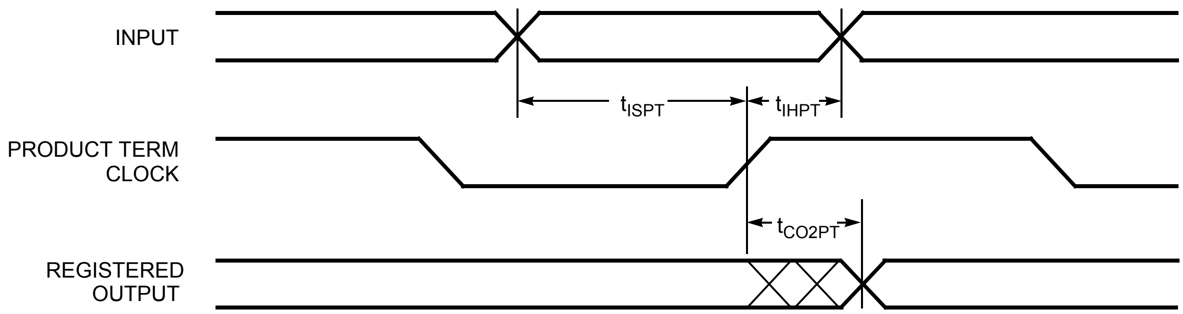


Switching Waveforms (continued)

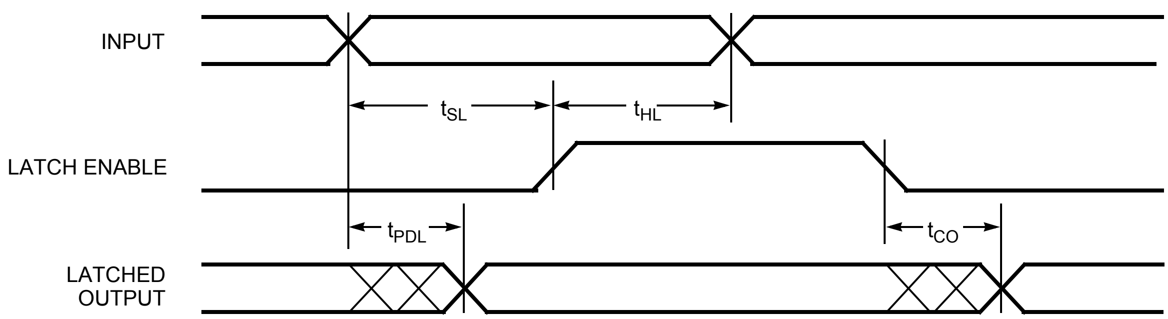
Registered Output with Product Term Clocking Input Going Through the Array



Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register

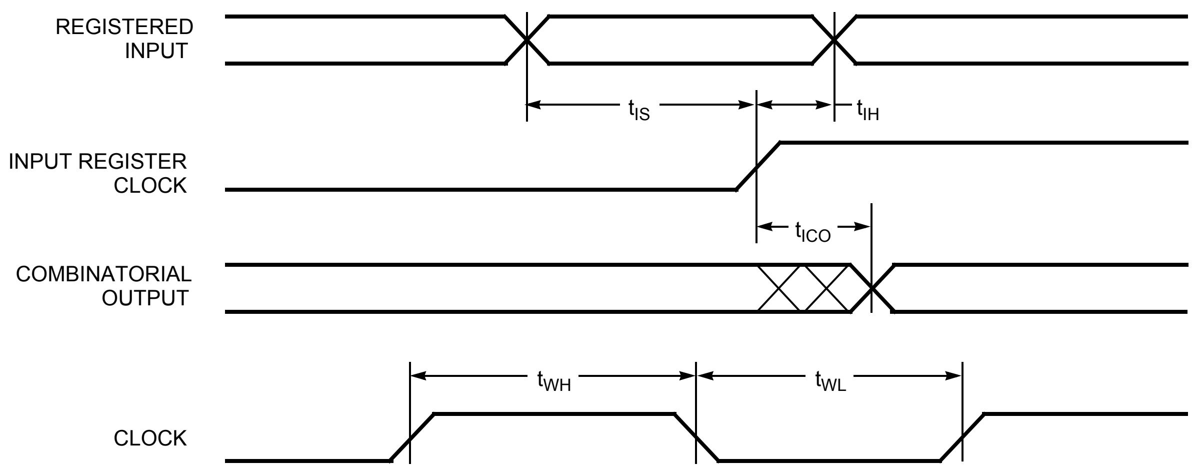


Latched Output

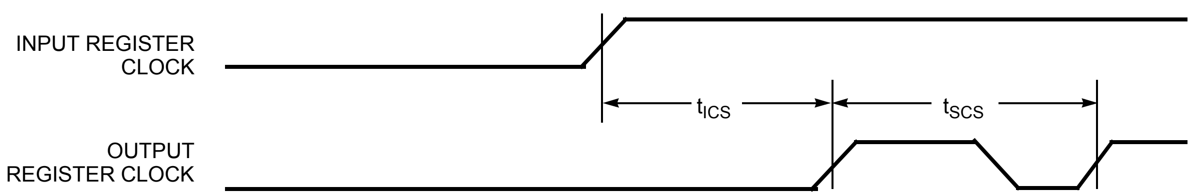


Switching Waveforms (continued)

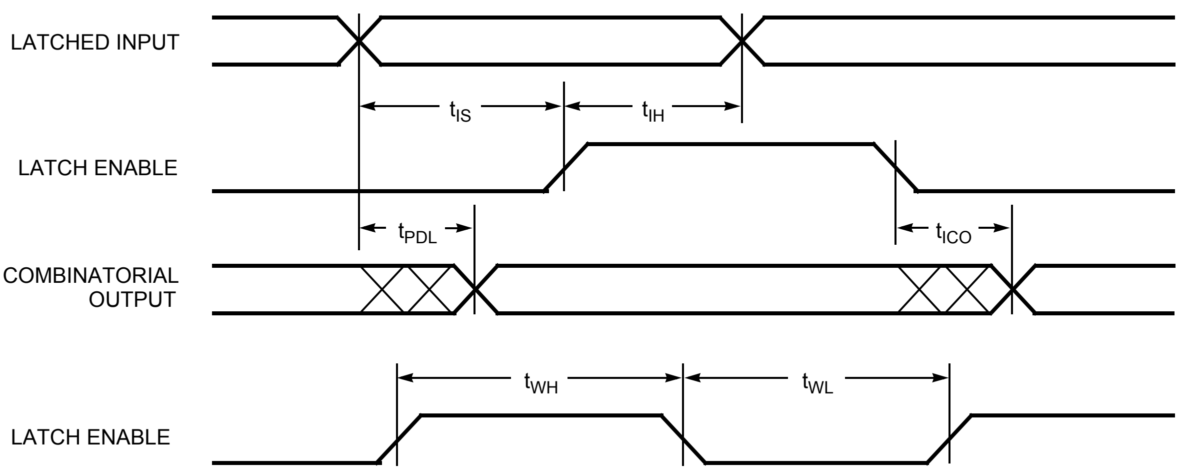
Registered Input



Clock to Clock

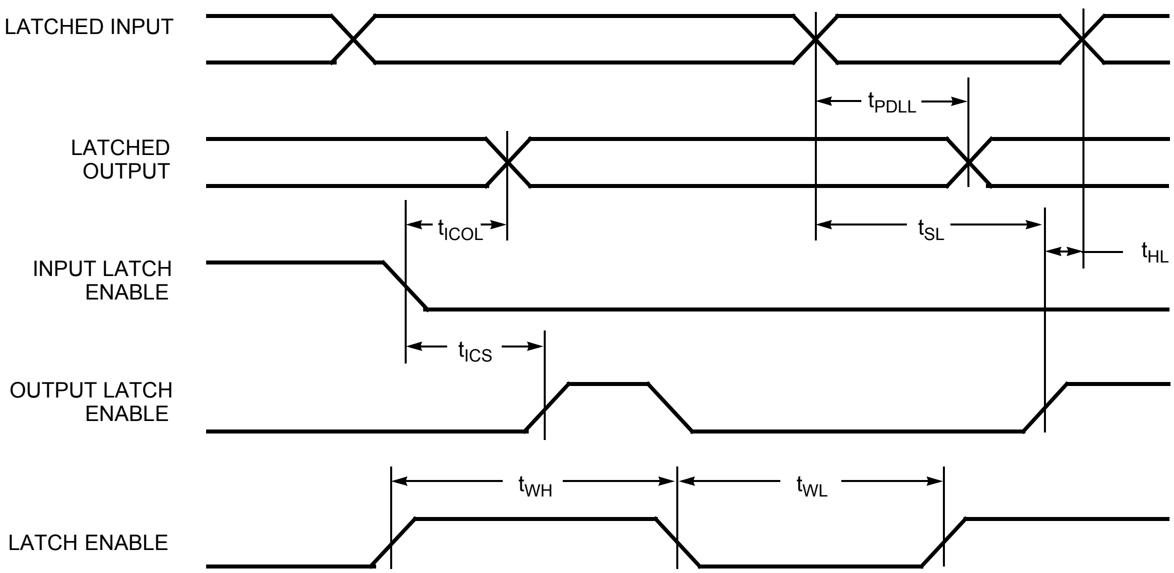


Latched Input

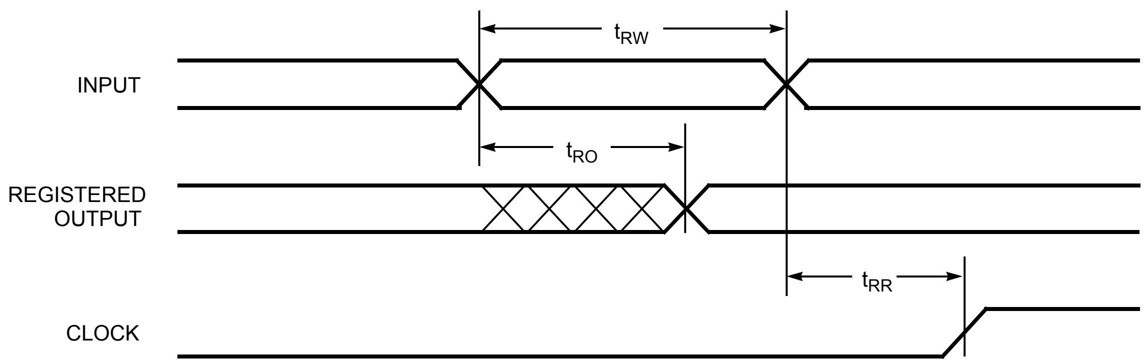


Switching Waveforms (continued)

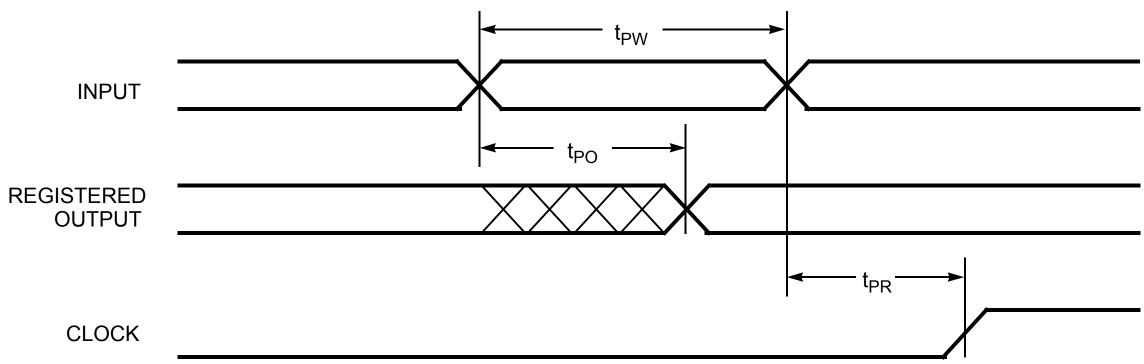
Latched Input and Output



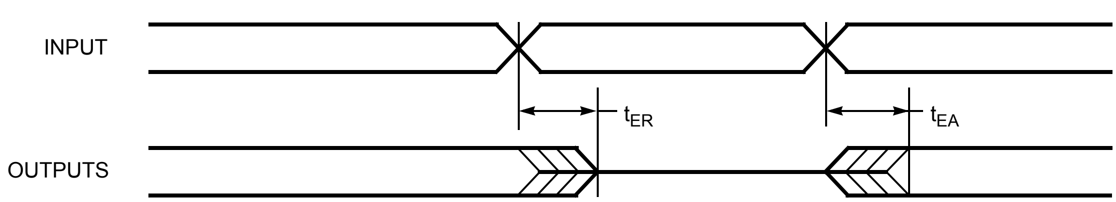
Asynchronous Reset



Asynchronous Preset



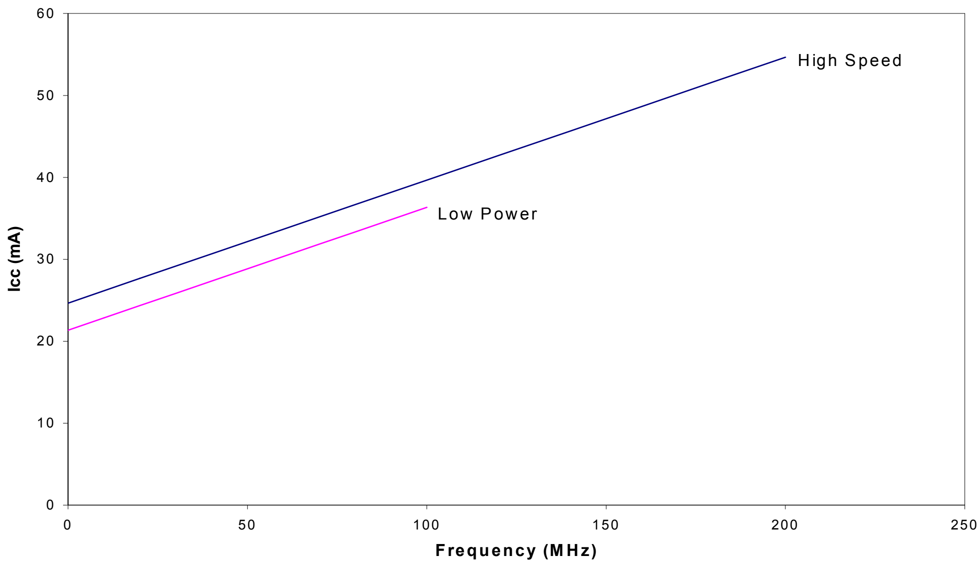
Output Enable/Disable



Power Consumption

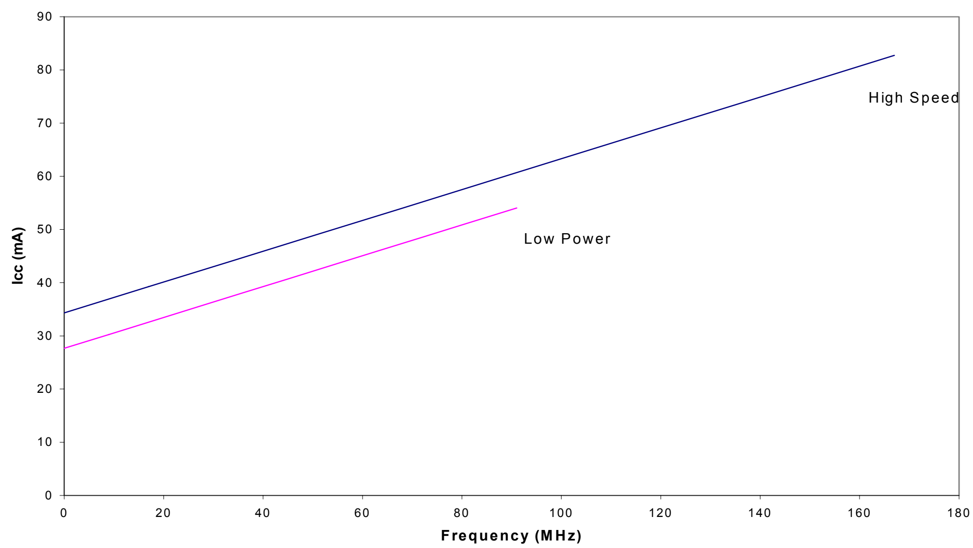
Typical 5.0V Power Consumption

CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

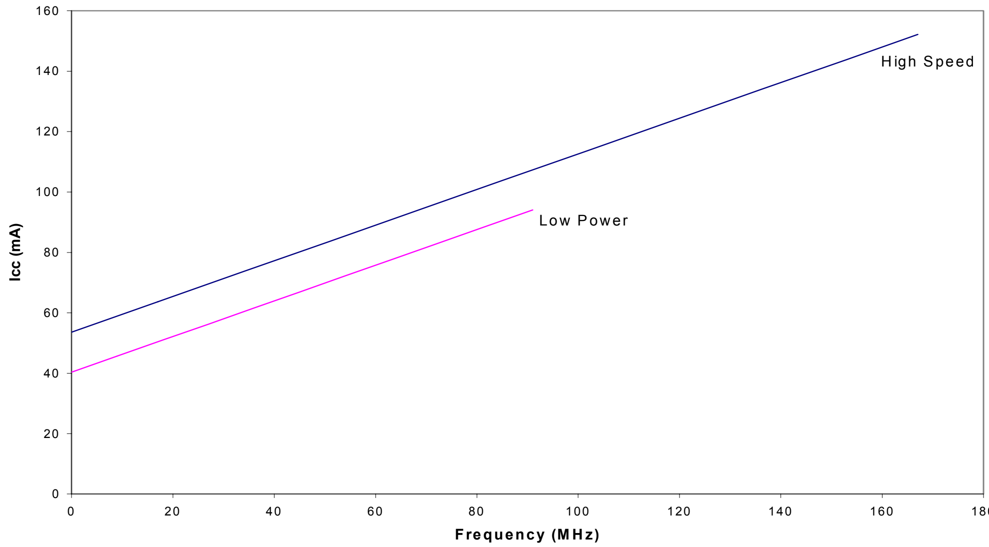
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

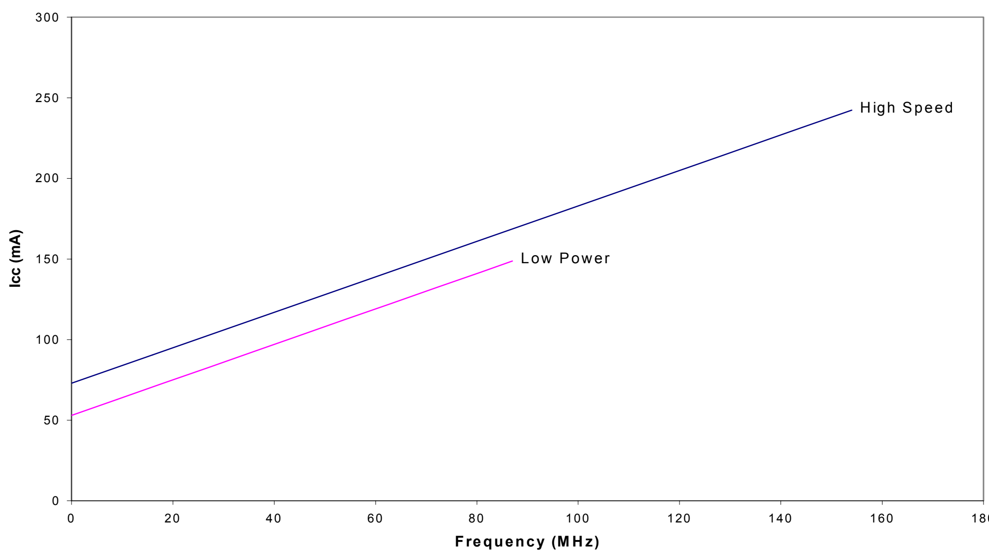
Typical 5.0V Power Consumption (continued)

CY37128



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

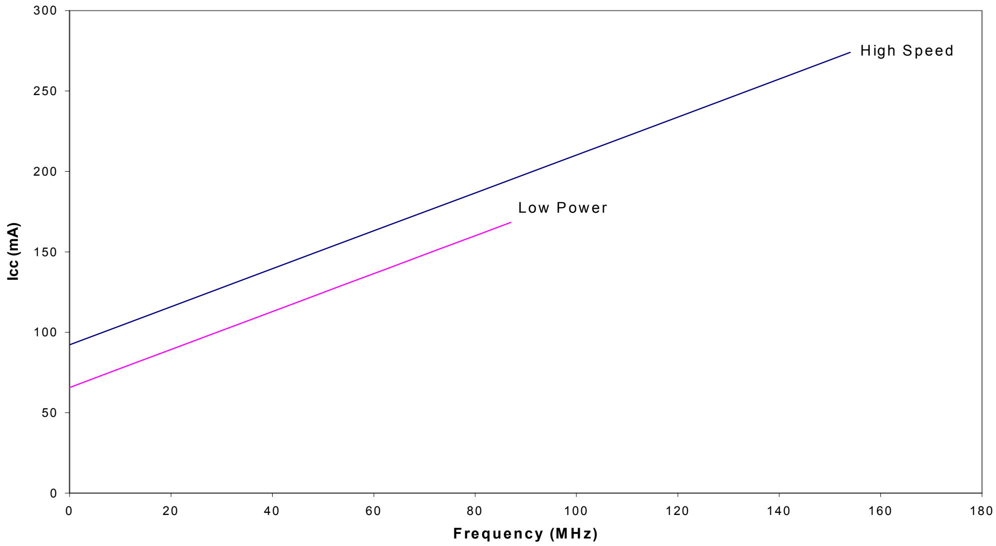
CY37192



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

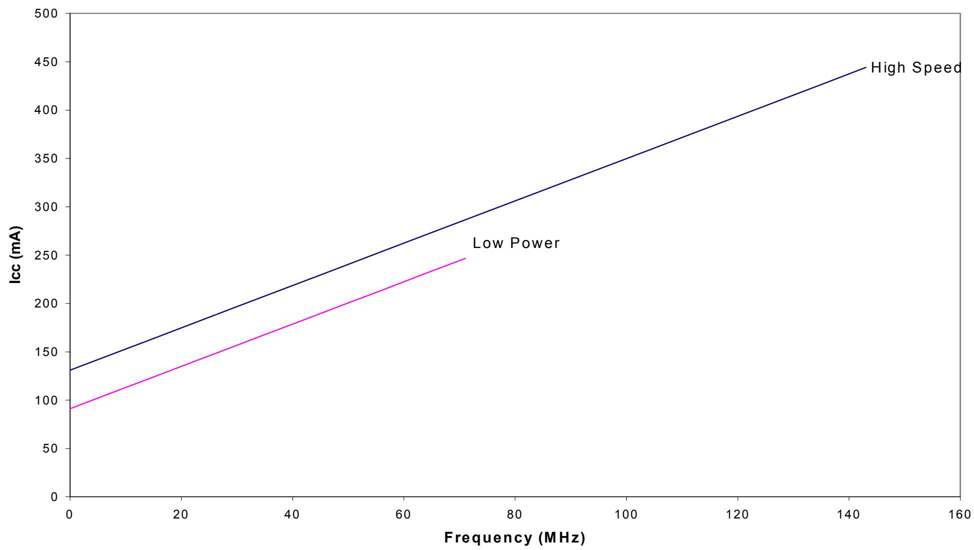
Typical 5.0V Power Consumption (continued)

CY37256



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

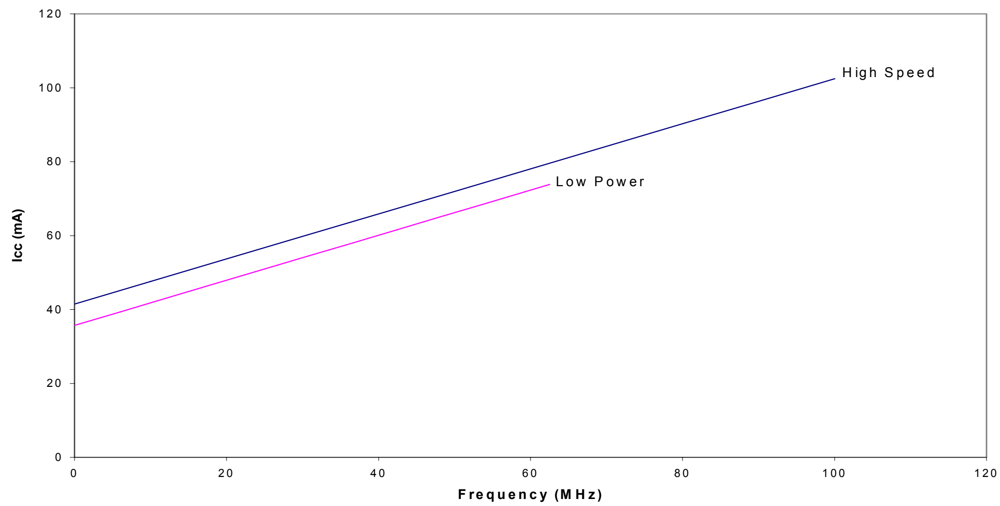
CY37384



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

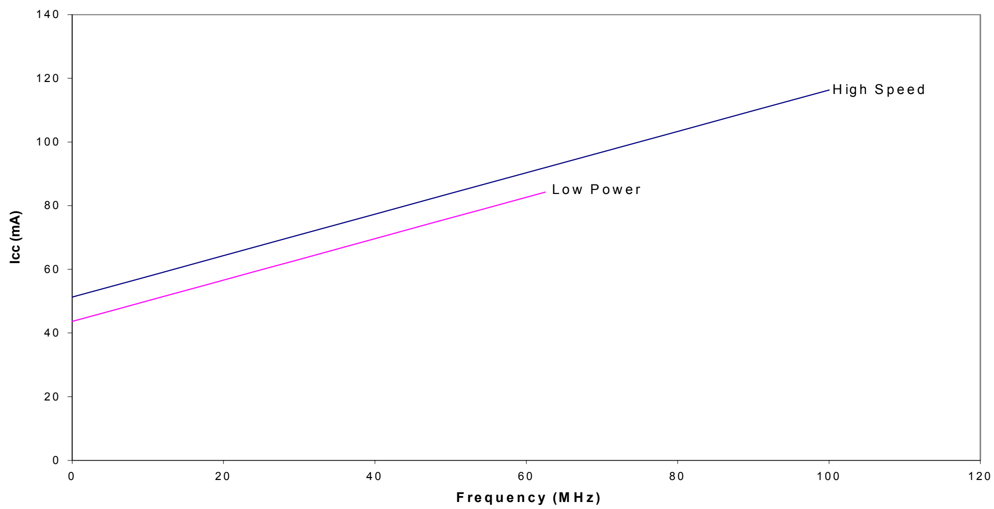
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

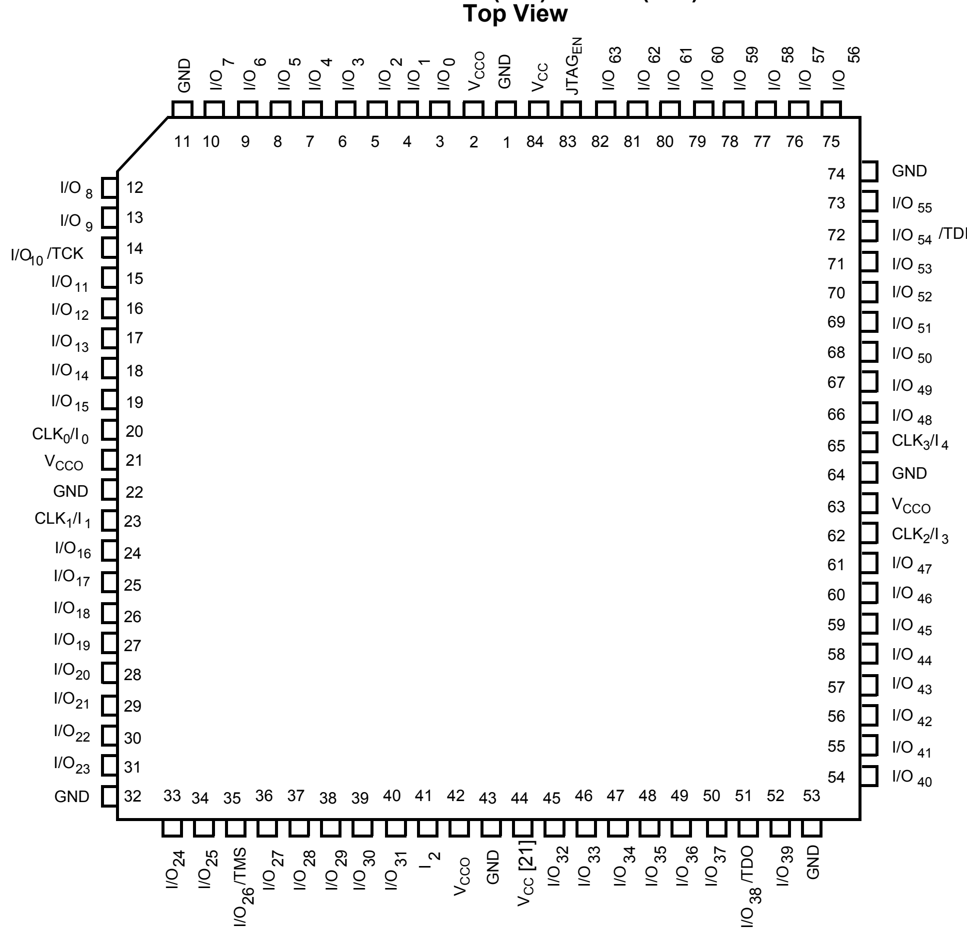
Pin Configurations[20] (continued)

48-ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O_5 TCK	V_{CC}	I/O_3	I/O_1	I/O_{31}	I/O_{30}	V_{CC}	I/O_{27} TDI
B	V_{CC}	I/O_4	I/O_2	I/O_0	I/O_{29}	I/O_{28}	I/O_{26}	CLK_1/I_4
C	CLK_2/I_0	I/O_7	I/O_6	GND	GND	I/O_{25}	I/O_{24}	I_3
D	$JTAG_{EN}$	I/O_8	I/O_9	GND	GND	I/O_{22}	I/O_{23}	CLK_3/I_2
E	CLK_0/I_1	I/O_{12}	I/O_{11}	I/O_{10}	I/O_{16}	I/O_{20}	I/O_{21}	V_{CC}
F	I/O_{13} TMS	V_{CC}	I/O_{14}	I/O_{15}	I/O_{17}	I/O_{18}	V_{CC}	I/O_{19} TDO

Note:
20. For 3.3V versions (Ultra37000V), $V_{CCO} = V_{CC}$.

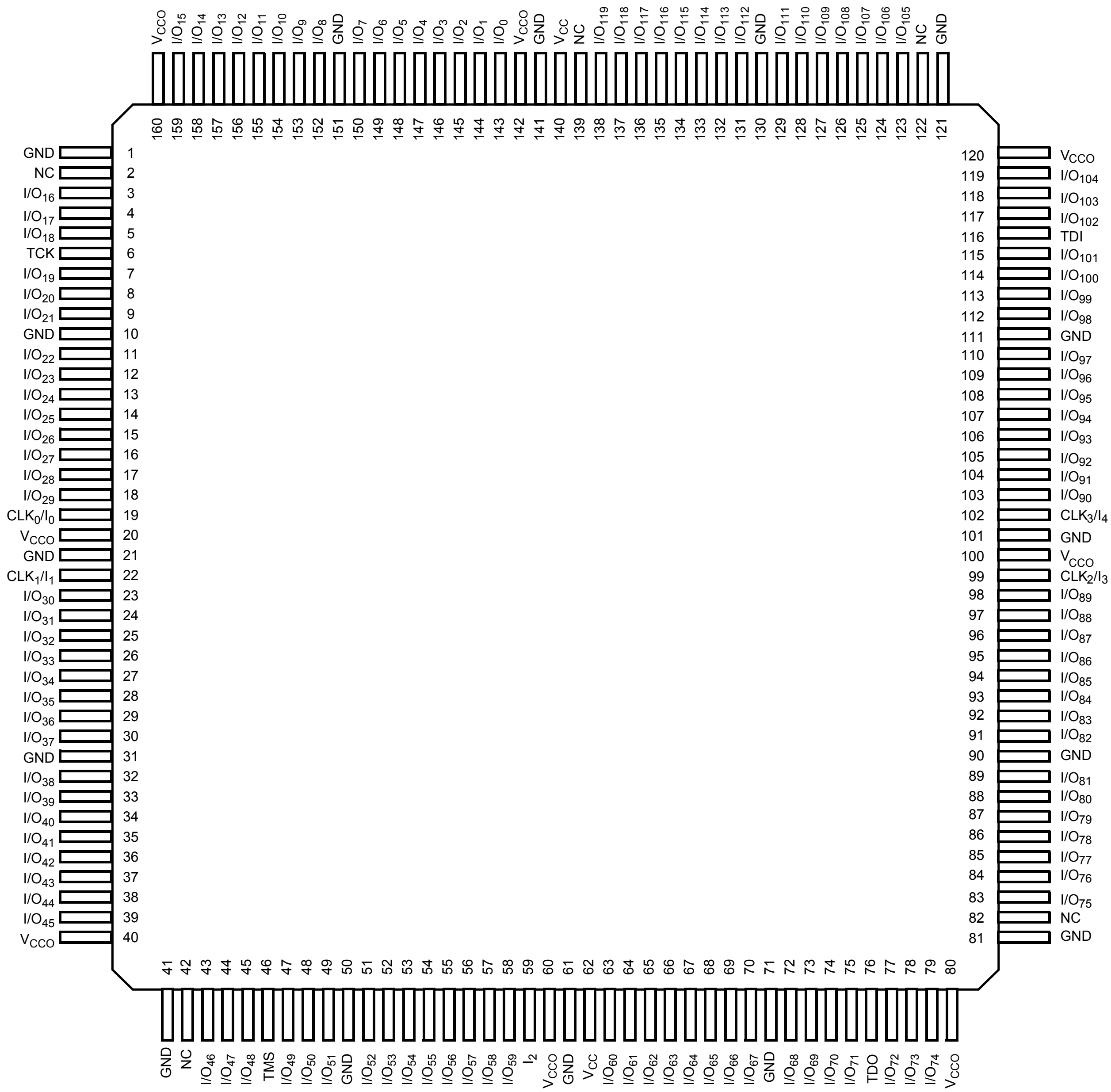
84-lead PLCC (J83) / CLCC (Y84)
Top View



Note:
21. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[20] (continued)

256-Ball Fine-Pitch BGA (BB256)

Top View

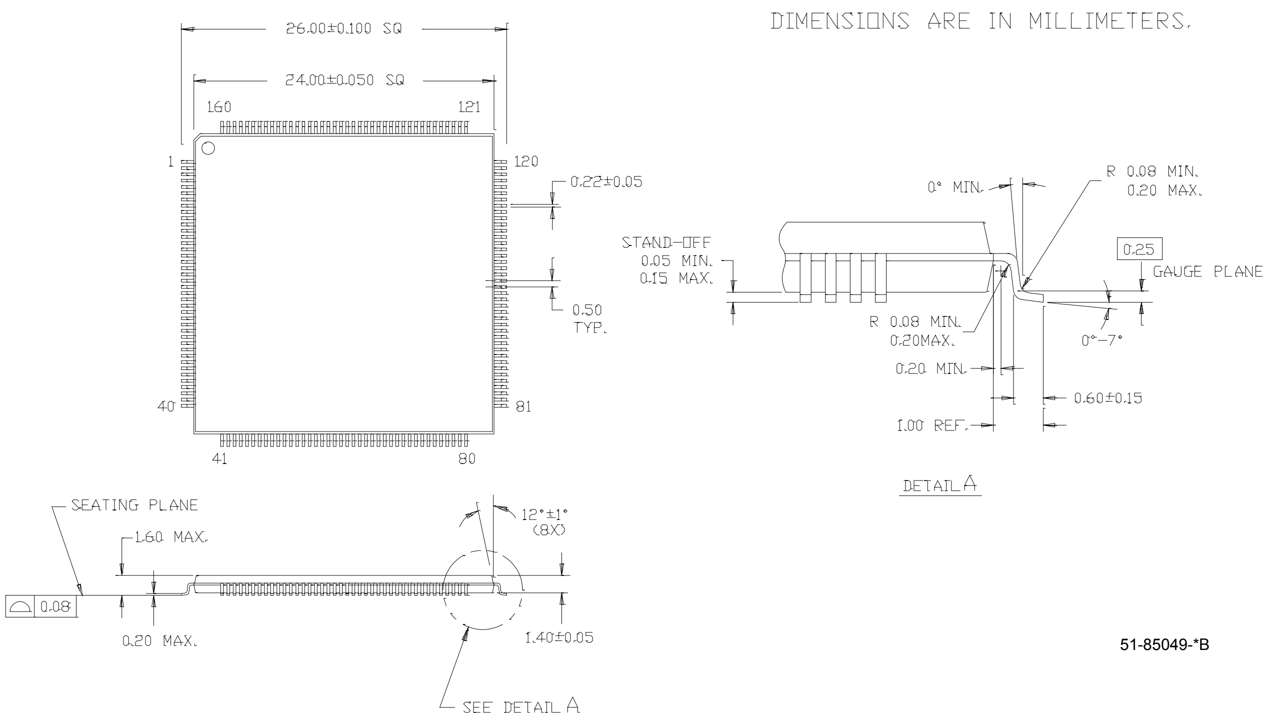
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	I/O$_{26}$	I/O$_{24}$	I/O$_{20}$	V$_{CC}$	I/O$_{11}$	GND	GND	I/O$_{186}$	V$_{CC}$	I/O$_{177}$	I/O$_{172}$	I/O$_{167}$	GND	GND
B	GND	I/O$_{27}$	I/O$_{25}$	I/O$_{23}$	I/O$_{19}$	I/O$_{15}$	I/O$_{10}$	GND	GND	I/O$_{185}$	I/O$_{181}$	I/O$_{176}$	I/O$_{171}$	I/O$_{166}$	I/O$_{165}$	GND
C	I/O$_{29}$	I/O$_{28}$	NC	I/O$_{22}$	I/O$_{18}$	I/O$_{14}$	I/O$_{9}$	I/O$_{4}$	I/O$_{191}$	I/O$_{184}$	I/O$_{180}$	I/O$_{175}$	I/O$_{170}$	NC	I/O$_{163}$	I/O$_{164}$
D	I/O$_{32}$	I/O$_{31}$	I/O$_{30}$	NC	I/O$_{17}$	I/O$_{13}$	I/O$_{8}$	I/O$_{3}$	I/O$_{190}$	I/O$_{183}$	I/O$_{179}$	I/O$_{174}$	I/O$_{169}$	I/O$_{160}$	I/O$_{161}$	I/O$_{162}$
E	I/O$_{35}$	I/O$_{34}$	I/O$_{33}$	I/O$_{21}$	I/O$_{16}$	I/O$_{12}$	I/O$_{7}$	I/O$_{2}$	I/O$_{189}$	V$_{CC}$	I/O$_{178}$	I/O$_{173}$	I/O$_{168}$	I/O$_{157}$	I/O$_{158}$	I/O$_{159}$
F	V$_{CC}$	I/O$_{38}$	I/O$_{37}$	I/O$_{36}$	TCK	V$_{CC}$	I/O$_{6}$	I/O$_{1}$	I/O$_{188}$	I/O$_{182}$	V$_{CC}$	TDI	I/O$_{154}$	I/O$_{155}$	I/O$_{156}$	V$_{CC}$
G	I/O$_{43}$	I/O$_{42}$	I/O$_{41}$	I/O$_{40}$	V$_{CC}$	I/O$_{39}$	I/O$_{5}$	I/O$_{0}$	I/O$_{187}$	I/O$_{148}$	I/O$_{149}$	CLK$_{3}$ /I$_{4}$	I/O$_{150}$	I/O$_{151}$	I/O$_{152}$	I/O$_{153}$
H	GND	GND	I/O$_{47}$	I/O$_{46}$	CLK$_{0}$ /I$_{0}$	I/O$_{45}$	I/O$_{44}$	GND	GND	I/O$_{144}$	I/O$_{145}$	CLK$_{2}$ /I$_{3}$	I/O$_{146}$	I/O$_{147}$	GND	GND
J	GND	GND	I/O$_{51}$	I/O$_{50}$	NC	I/O$_{49}$	I/O$_{48}$	GND	GND	I/O$_{140}$	I/O$_{141}$	I$_{2}$	I/O$_{142}$	I/O$_{143}$	GND	GND
K	I/O$_{57}$	I/O$_{56}$	I/O$_{55}$	I/O$_{54}$	CLK$_{1}$ /I$_{1}$	I/O$_{53}$	I/O$_{52}$	I/O$_{91}$	I/O$_{96}$	I/O$_{101}$	I/O$_{135}$	V$_{CC}$	I/O$_{136}$	I/O$_{137}$	I/O$_{138}$	I/O$_{139}$
L	V$_{CC}$	I/O$_{60}$	I/O$_{59}$	I/O$_{58}$	TMS	V$_{CC}$	I/O$_{86}$	I/O$_{92}$	I/O$_{97}$	I/O$_{102}$	V$_{CC}$	TDO	I/O$_{132}$	I/O$_{133}$	I/O$_{134}$	V$_{CC}$
M	I/O$_{63}$	I/O$_{62}$	I/O$_{61}$	I/O$_{72}$	I/O$_{77}$	I/O$_{82}$	V$_{CC}$	I/O$_{93}$	I/O$_{98}$	I/O$_{103}$	I/O$_{108}$	I/O$_{112}$	I/O$_{117}$	I/O$_{129}$	I/O$_{130}$	I/O$_{131}$
N	I/O$_{66}$	I/O$_{65}$	I/O$_{64}$	I/O$_{73}$	I/O$_{78}$	I/O$_{83}$	I/O$_{87}$	I/O$_{94}$	I/O$_{99}$	I/O$_{104}$	I/O$_{109}$	I/O$_{113}$	NC	I/O$_{126}$	I/O$_{127}$	I/O$_{128}$
P	I/O$_{68}$	I/O$_{67}$	NC	I/O$_{74}$	I/O79	I/O$_{84}$	I/O$_{88}$	I/O$_{95}$	I/O$_{100}$	I/O$_{105}$	I/O$_{110}$	I/O$_{114}$	I/O$_{118}$	NC	I/O$_{124}$	I/O$_{125}$
R	GND	I/O$_{69}$	I/O$_{70}$	I/O$_{75}$	I/O$_{80}$	I/O$_{85}$	I/O$_{89}$	GND	GND	I/O$_{106}$	I/O$_{111}$	I/O$_{115}$	I/O$_{119}$	I/O$_{121}$	I/O$_{123}$	GND
T	GND	GND	I/O$_{71}$	I/O$_{76}$	I/O$_{81}$	V$_{CC}$	I/O$_{90}$	GND	GND	I/O$_{107}$	V$_{CC}$	I/O$_{116}$	I/O$_{120}$	I/O$_{122}$	GND	GND

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military

Package Diagrams (continued)

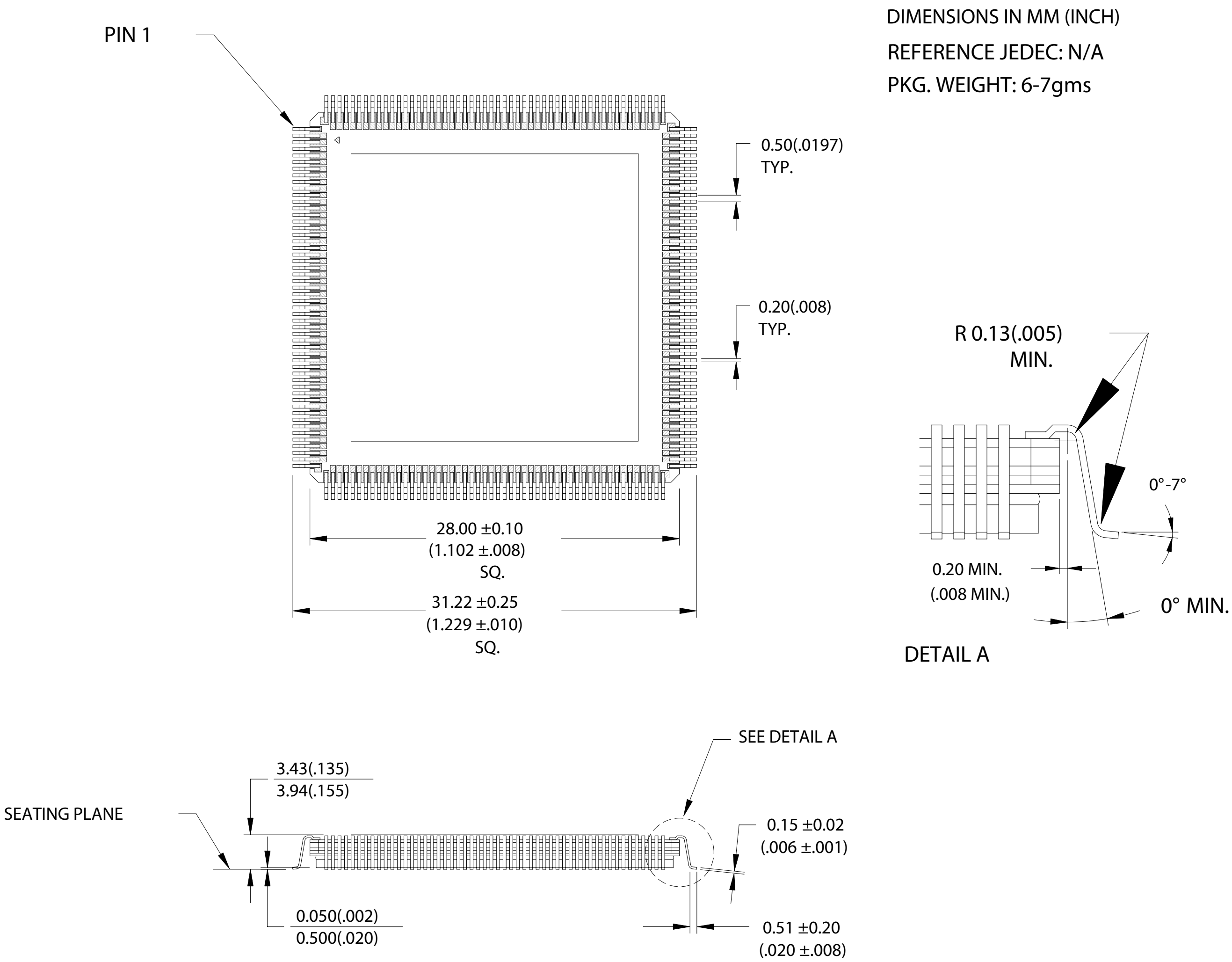
160-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (24 x 24 x 1.4 mm) (TQFP) A160



51-85049-*B

Package Diagrams (continued)

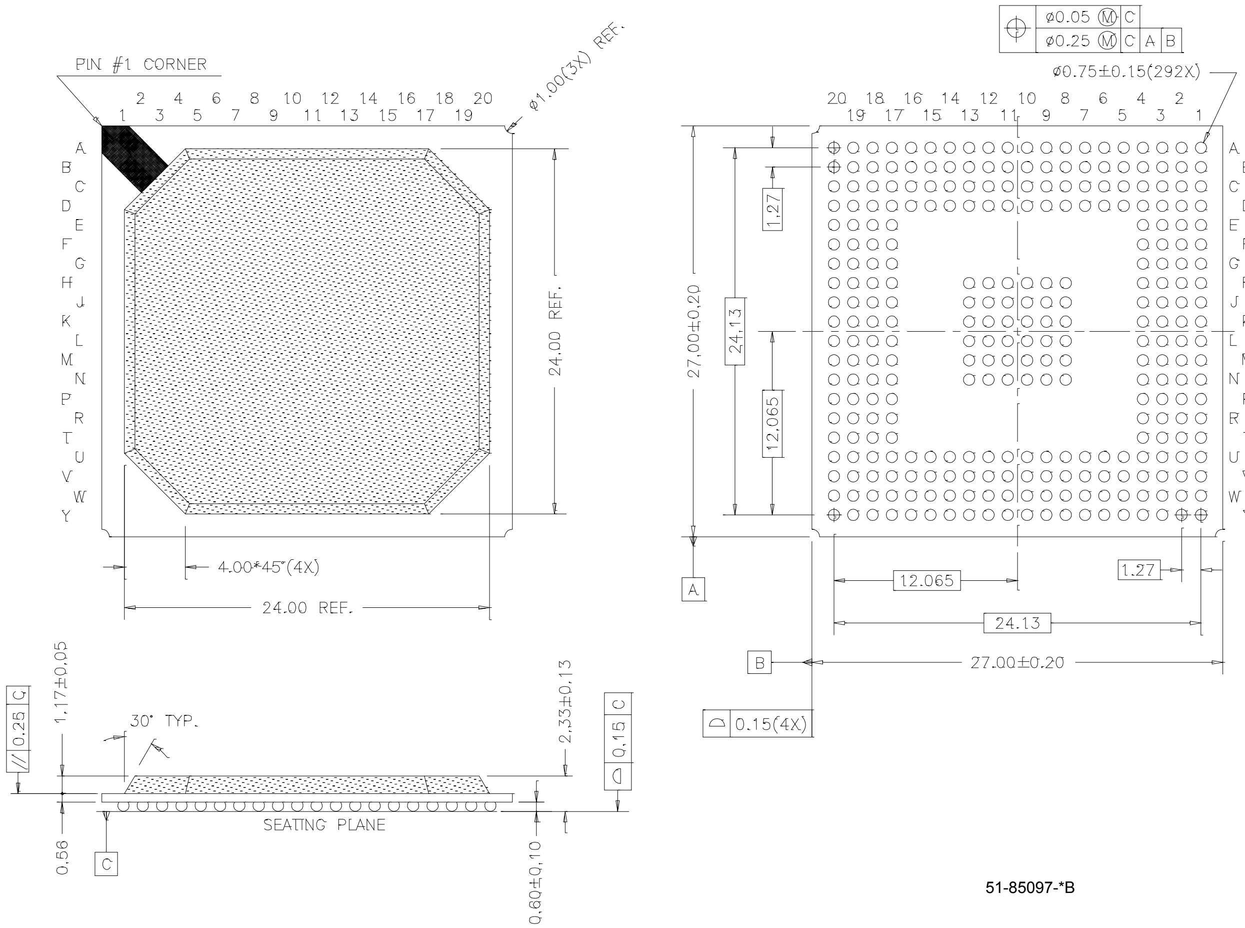
208-Lead Ceramic Quad Flatpack (Cavity Up) U208



51-80105-*B

Package Diagrams (continued)

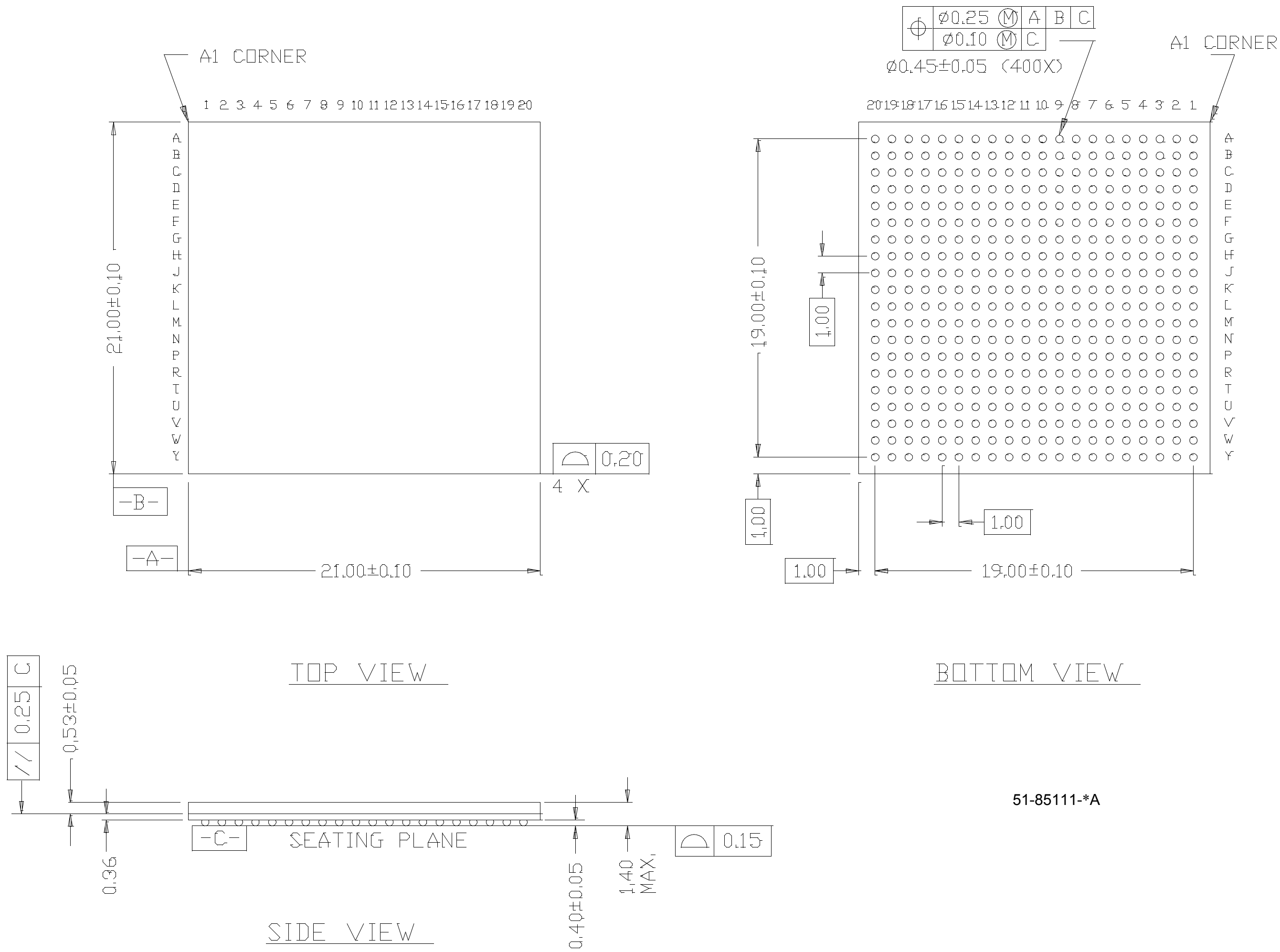
292-Ball Plastic Ball Grid Array PBGA (27 x 27 x 2.33 mm) BG292



51-85097-*B

Package Diagrams (continued)

400-Ball FBGA (21 x 21 x 1.4 mm) BB400



51-85111-*A

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