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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	192
Number of Gates	-
Number of I/O	125
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37192vp160-100ac

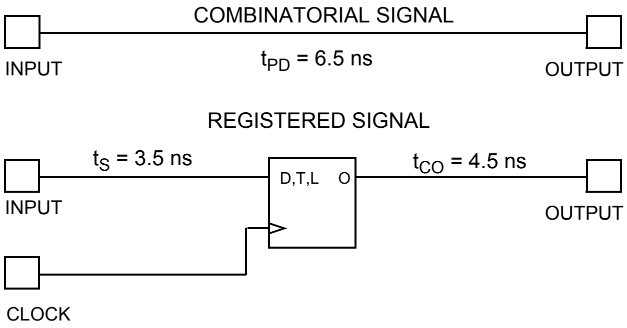


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

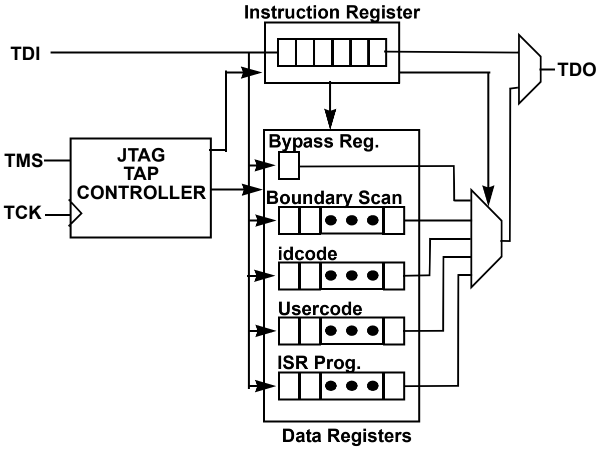


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC, *Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

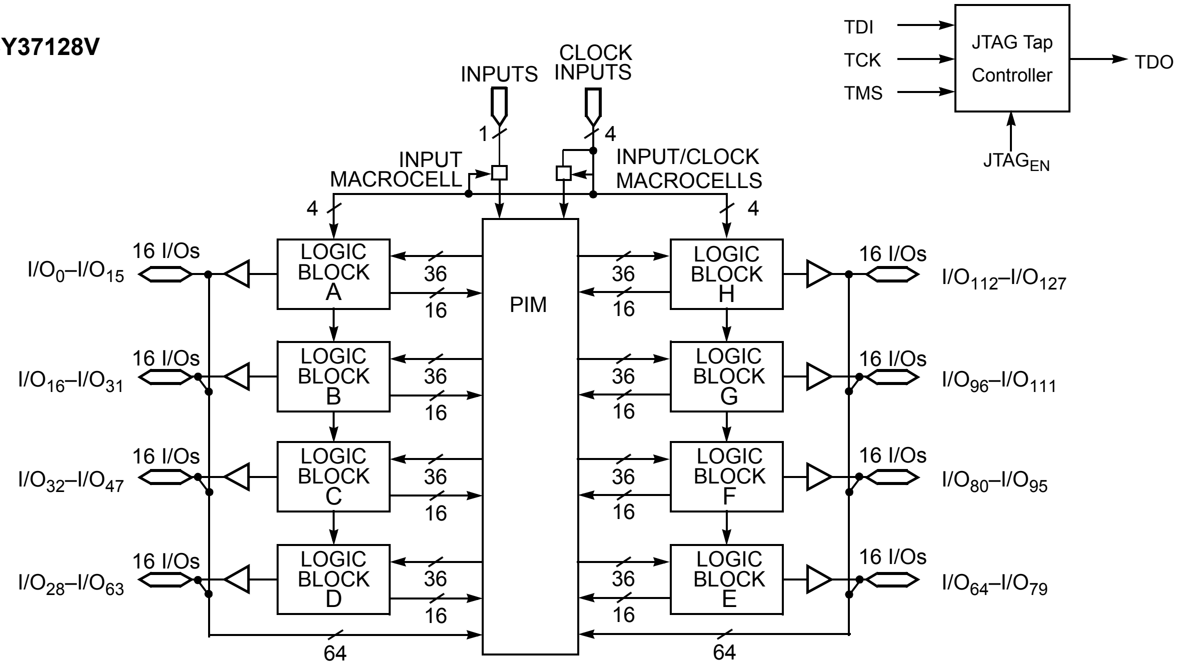
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

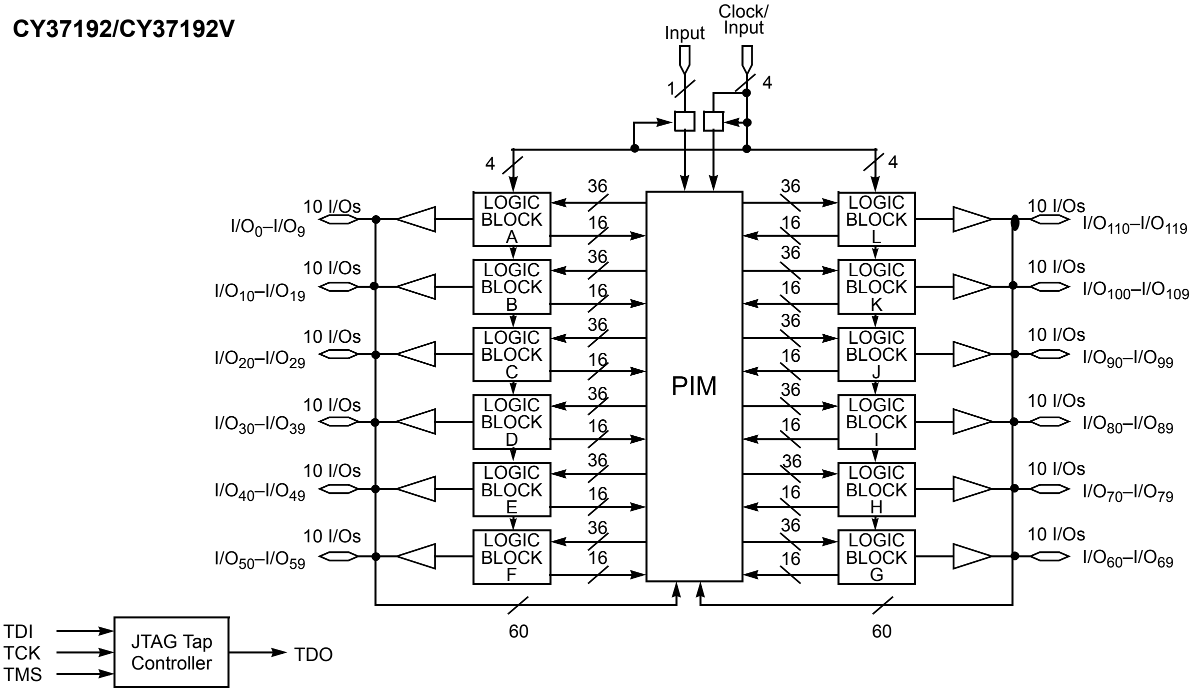
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams (continued)

CY37128/CY37128V



CY37192/CY37192V



5.0V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage to Ground Potential ....–0.5V to +7.0V

DC Voltage Applied to Outputs
in High-Z State...–0.5V to +7.0V

DC Input Voltage ....–0.5V to +7.0V

DC Program Voltage.. 4.5 to 5.5V

Current into Outputs .... 16 mA

Static Discharge Voltage.. > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current... > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[5]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l)[6]			4.2	V
			I_{OH} = 0 µA (Ind/Mil)[6]			4.5	V
			I_{OH} = –100 µA (Com'l)[6]			3.6	V
			I_{OH} = –150 µA (Ind/Mil)[6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled "An Introduction to In System Reprogramming with the Ultra37000."
3. T_A is the "Instant On" case temperature.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual-Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

3.3V Device Characteristics
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State...–0.5V to +7.0V

DC Input Voltage ....–0.5V to +7.0V

DC Program Voltage... 3.0 to 3.6V

Current into Outputs .... 8 mA

Static Discharge Voltage.. > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}[10]
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

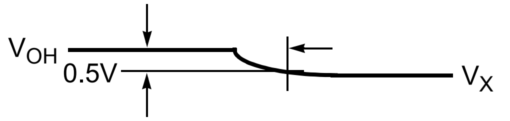
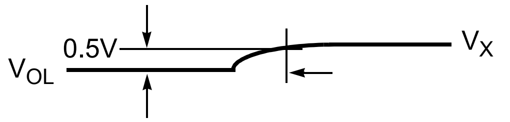
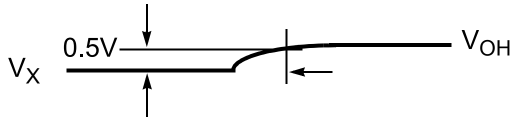
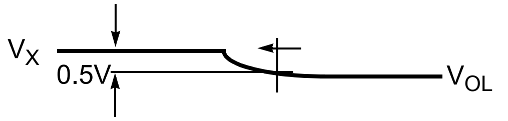
3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Notes:

[9] Dual pins are I/O with JTAG pins.

[10] For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V± 0.16V.

Parameter[11]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Switching Characteristics Over the Operating Range [12]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t_{PD}[13, 14, 15]	Input to Combinatorial Output	ns
t_{PDL}[13, 14, 15]	Input to Output Through Transparent Input or Output Latch	ns
t_{PDLL}[13, 14, 15]	Input to Output Through Transparent Input and Output Latches	ns
t_{EA}[13, 14, 15]	Input to Output Enable	ns
t_{ER}[11, 13]	Input to Output Disable	ns
Input Register Parameters		
t_{WL}	Clock or Latch Enable Input LOW Time[8]	ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	ns
t_{IS}	Input Register or Latch Set-up Time	ns
t_{IH}	Input Register or Latch Hold Time	ns
t_{ICO}[13, 14, 15]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t_{ICOL}[13, 14, 15]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t_{CO}[14, 15]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output	ns
t_S[13]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_H	Register or Latch Data Hold Time	ns
t_{CO2}[13, 14, 15]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t_{SCS}[13]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	ns
t_{SL}[13]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns

Notes:

[11] t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

[12] All AC parameters are measured with two outputs switching and 35-pF AC Test Load.

[13] Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.

[14] Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.

[15] When V_{CCO} = 3.3V, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range [12]

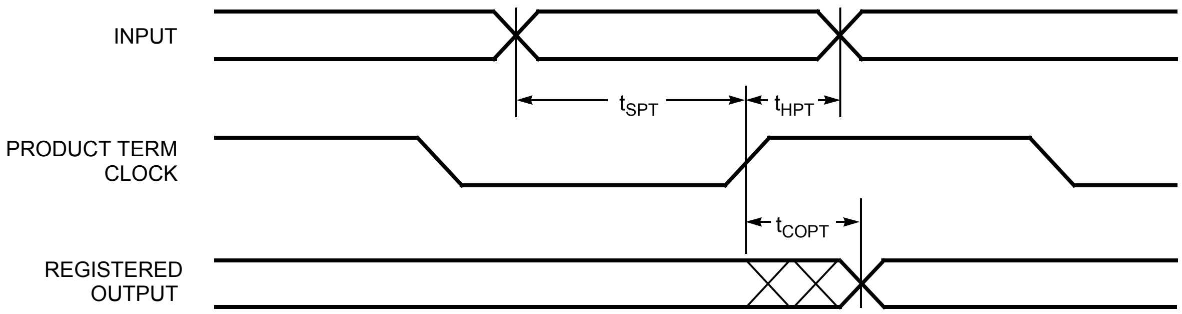
Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t_{PD}[13, 14, 15]		6		6.5		7.5		8.5		10		12		15		20	ns
t_{PDL}[13, 14, 15]		11		12.5		14.5		16		16.5		17		19		22	ns
t_{PDLL}[13, 14, 15]		12		13.5		15.5		17		17.5		18		20		24	ns
t_{EA}[13, 14, 15]		8		8.5		11		13		14		16		19		24	ns
t_{ER}[11, 13]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t_{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{IS}	2		2		2		2		2		2.5		3		4		ns
t_{IH}	2		2		2		2		2		2.5		3		4		ns
t_{ICO}[13, 14, 15]		11		11		11		12.5		12.5		16		19		24	ns
t_{ICOL}[13, 14, 15]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t_{CO} [14, 15]		4		4		4.5		6		6.5[16]		6.5[17]		8[18]		10	ns
t_S[13]	4		4		5		5		5.5[16]		6[17]		8[18]		10		ns
t_H	0		0		0		0		0		0		0		0		ns
t_{CO2}[13, 14, 15]		9.5		10		11		12		14		16		19		24	ns
t_{SCS}[13]	5		6		6.5		7		8[16]		10		12		15		ns
t_{SL} [13]	7.5		7.5		8.5		9		10		12		15		15		ns
t_{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t_{COPT}[13, 14, 15]		7		10		10		13		13		13		15		20	ns
t_{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{ISPT}[13]	0		0		0		0		0		0		0		0		ns
t_{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t_{CO2PT}[13, 14, 15]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t_{ICS}[13]	5		6		6		7		8[16]		10		12		15		ns
Operating Frequency Parameters																	
f_{MAX1}	200		167		154		143		125[16]		100		83		66		MHz
f_{MAX2}	200		200		200		167		154		153[17]		125[18]		100		MHz
f_{MAX3}	125		125		105		91		83		80[17]		62.5		50		MHz
f_{MAX4}	167		167		154		125		118		100		83		66		MHz
Reset/Preset Parameters																	
t_{RW}	8		8		8		8		10		12		15		20		ns
t_{RR}[13]	10		10		10		10		12		14		17		22		ns

Notes:

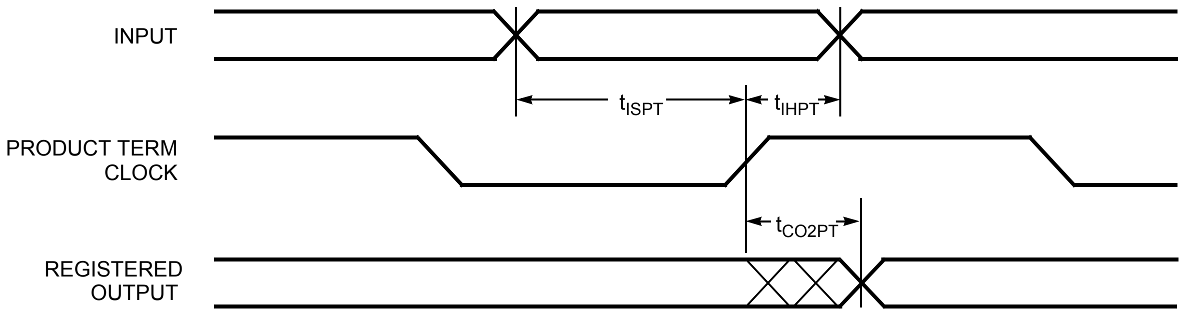
16. The following values correspond to the CY37512 and CY37384 devices: t_{CO} = 5 ns, t_S = 6.5 ns, t_{SCS} = 8.5 ns, t_{ICS} = 8.5 ns, f_{MAX1} = 118 MHz.
17. The following values correspond to the CY37192V and CY37256V devices: t_{CO} = 6 ns, t_S = 7 ns, f_{MAX2} = 143 MHz, f_{MAX3} = 77 MHz, and f_{MAX4} = 100 MHz; and for the CY37512 devices: t_S = 7 ns.
18. The following values correspond to the CY37512V and CY37384V devices: t_{CO} = 6.5 ns, t_S = 9.5 ns, and f_{MAX2} = 105 MHz.

Switching Waveforms (continued)

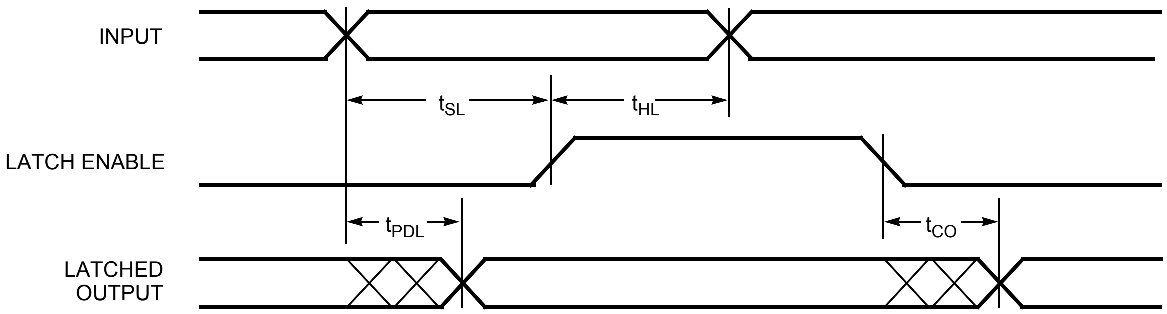
Registered Output with Product Term Clocking Input Going Through the Array



Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register

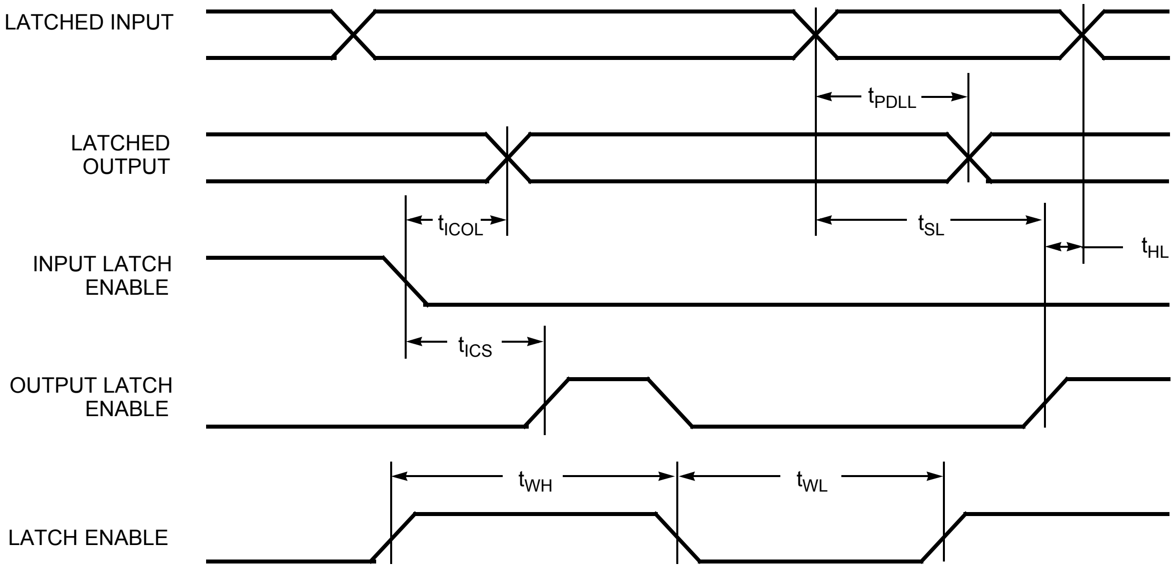


Latched Output

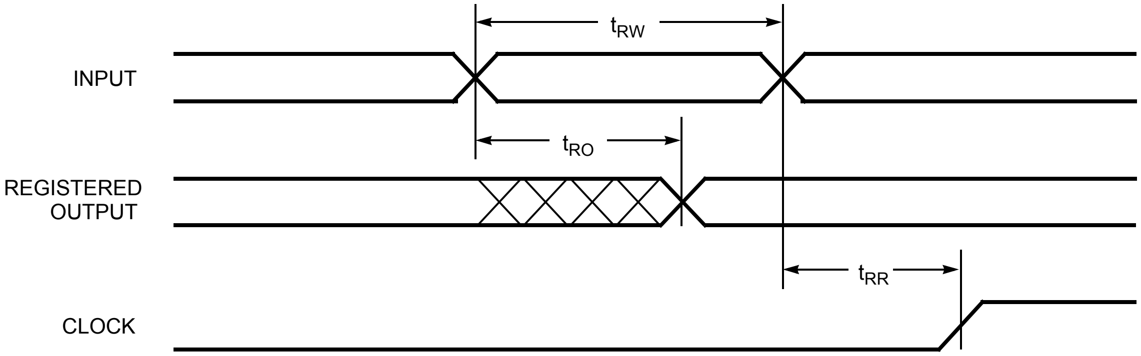


Switching Waveforms (continued)

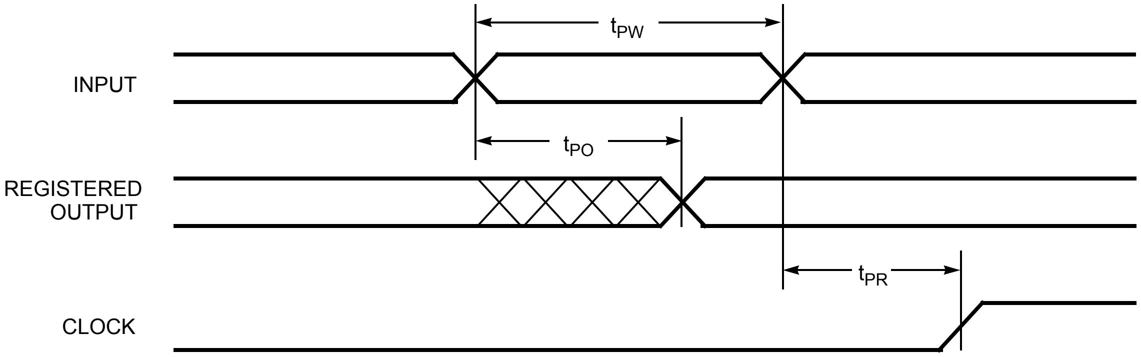
Latched Input and Output



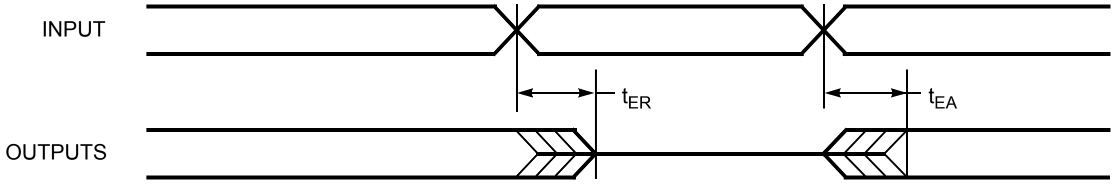
Asynchronous Reset



Asynchronous Preset

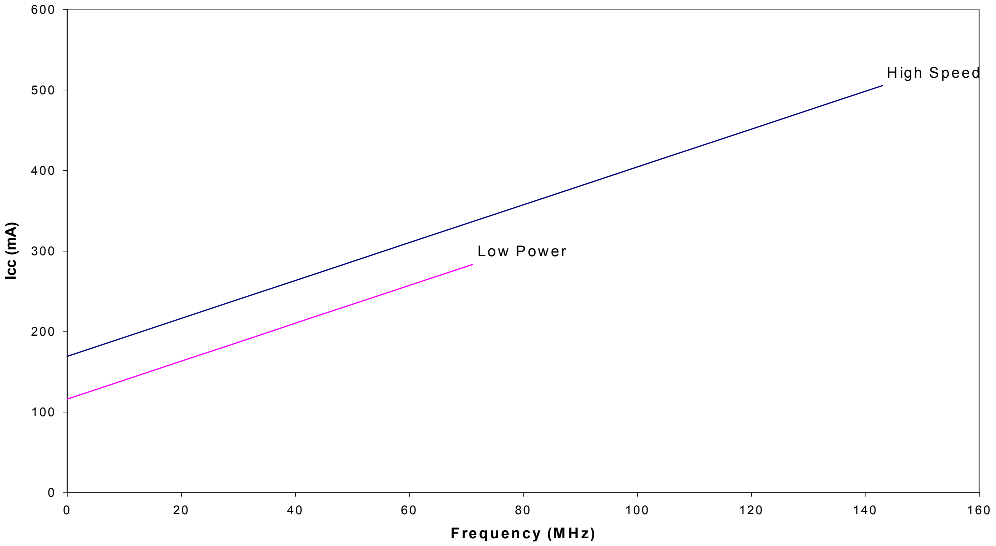


Output Enable/Disable



Typical 5.0V Power Consumption (continued)

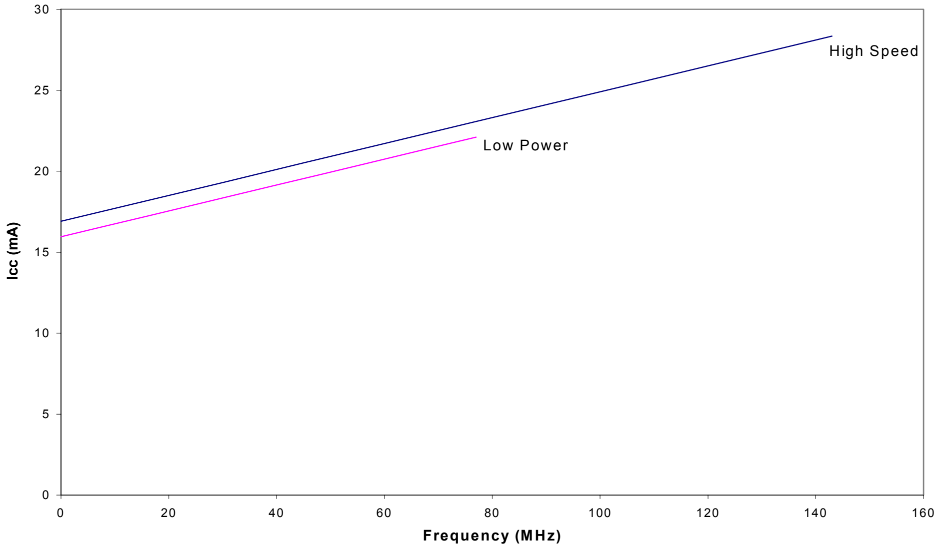
CY37512



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 3.3V Power Consumption

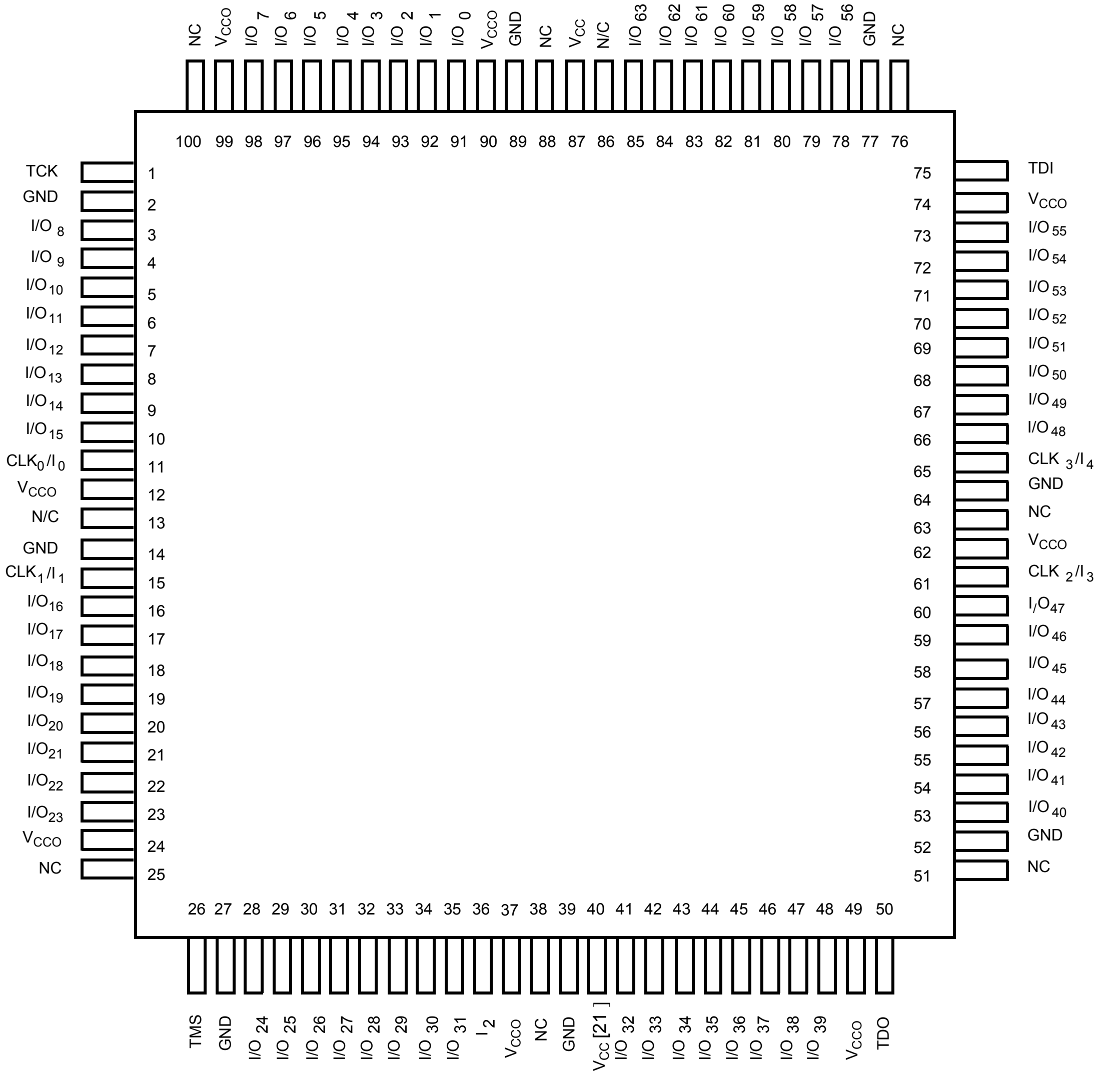
CY37032V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

Pin Configurations[20] (continued)

100-lead TQFP (A100)
Top View



Pin Configurations[20] (continued)

100-ball Fine-Pitch BGA (BB100) for CY37064V

Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	NC	I/O$_{7}$	I/O$_{5}$	I/O$_{2}$	I/O$_{62}$	I/O$_{60}$	I/O$_{58}$	I/O$_{57}$	I/O$_{56}$
B	I/O$_{9}$	I/O$_{8}$	I/O$_{6}$	I/O$_{4}$	I/O$_{1}$	I/O$_{63}$	V$_{CC}$	I/O$_{59}$	I/O$_{55}$	NC
C	I/O$_{10}$	TCK	V$_{CC}$	I/O$_{3}$	NC	NC	I/O$_{61}$	V$_{CC}$	TDI	I/O$_{54}$
D	I/O$_{11}$	NC	I/O$_{12}$	I/O$_{13}$	I/O$_{0}$	NC	I/O$_{51}$	I/O$_{52}$	CLK$_{3}$/I$_{4}$	I/O$_{53}$
E	I/O$_{14}$	CLK$_{0}$/I$_{0}$	I/O$_{15}$	NC	GND	GND	I/O$_{48}$	I/O$_{49}$	CLK$_{2}$/I$_{3}$	I/O$_{50}$
F	I/O$_{17}$	NC	NC	I/O$_{16}$	GND	GND	NC	NC	I$_{2}$	I/O$_{47}$
G	I/O$_{22}$	CLK$_{1}$/I$_{1}$	I/O$_{21}$	I/O$_{19}$	I/O$_{18}$	I/O$_{46}$	I/O$_{45}$	I/O$_{44}$	NC	I/O$_{43}$
H	I/O$_{23}$	TMS	V$_{CC}$	I/O$_{20}$	NC	I/O$_{32}$	I/O$_{42}$	V$_{CC}$	TDO	I/O$_{41}$
J	NC	I/O$_{26}$	I/O$_{28}$	NC	I/O$_{31}$	I/O$_{33}$	I/O$_{35}$	I/O$_{37}$	I/O$_{39}$	I/O$_{40}$
K	I/O$_{24}$	I/O$_{25}$	I/O$_{27}$	I/O$_{29}$	I/O$_{30}$	I/O$_{34}$	I/O$_{36}$	I/O$_{38}$	NC	NC

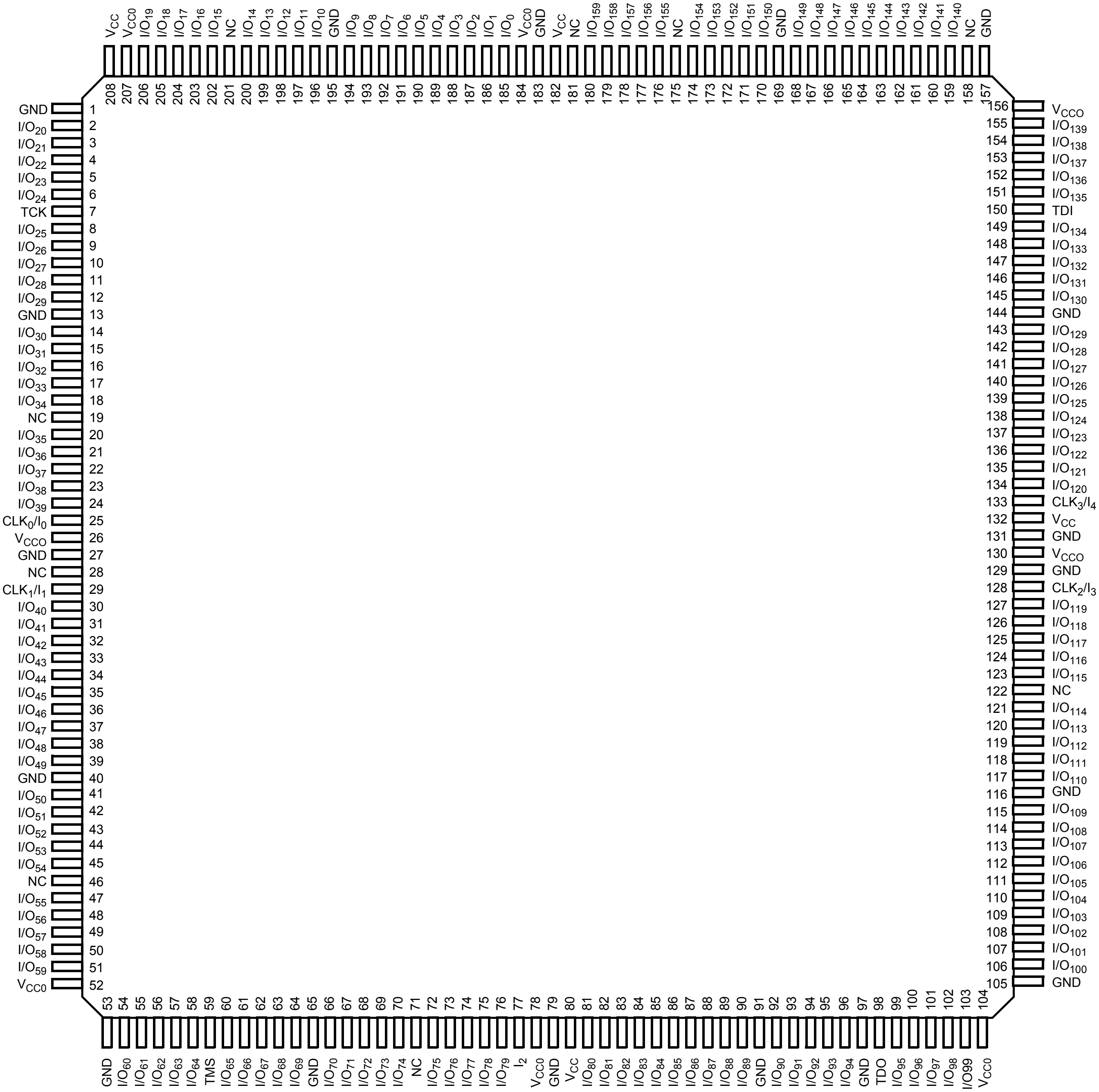
100-ball Fine-Pitch BGA (BB100) for CY37128V

Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	I/O$_{9}$	I/O$_{8}$	I/O$_{6}$	I/O$_{3}$	I/O$_{76}$	I/O$_{74}$	I/O$_{72}$	I/O$_{71}$	I/O$_{70}$
B	I/O$_{11}$	I/O$_{10}$	I/O$_{7}$	I/O$_{5}$	I/O$_{2}$	I/O$_{77}$	V$_{CC}$	I/O$_{73}$	I/O$_{68}$	I/O$_{69}$
C	I/O$_{12}$	I/O$_{13}$ TCK	V$_{CC}$	I/O$_{4}$	I/O$_{1}$	I/O$_{78}$	I/O$_{75}$	V$_{CC}$	I/O$_{67}$ TDI	I/O$_{66}$
D	I/O$_{14}$	NC	I/O$_{15}$	I/O$_{16}$	I/O$_{0}$	I/O$_{79}$	I/O$_{63}$	I/O$_{64}$	CLK$_{3}$/I$_{4}$	I/O$_{65}$
E	I/O$_{17}$	CLK$_{0}$/I$_{0}$	I/O$_{18}$	I/O$_{19}$	GND	GND	I/O$_{60}$	I/O$_{61}$	CLK$_{2}$/I$_{3}$	I/O$_{62}$
F	I/O$_{22}$	JTAG EN	I/O$_{21}$	I/O$_{20}$	GND	GND	I/O$_{59}$	I/O$_{58}$	I$_{2}$	I/O$_{57}$
G	I/O$_{27}$	CLK$_{1}$/I$_{1}$	I/O$_{26}$	I/O$_{24}$	I/O$_{23}$	I/O$_{56}$	I/O$_{55}$	I/O$_{54}$	NC	I/O$_{53}$
H	I/O$_{28}$	I/O$_{33}$ TMS	V$_{CC}$	I/O$_{25}$	I/O$_{39}$	I/O$_{40}$	I/O$_{52}$	V$_{CC}$	I/O$_{47}$ TDO	I/O$_{51}$
J	I/O$_{29}$	I/O$_{32}$	I/O$_{35}$	V$_{CC}$	I/O$_{38}$	I/O$_{41}$	I/O$_{43}$	I/O$_{45}$	I/O$_{48}$	I/O$_{50}$
K	I/O$_{30}$	I/O$_{31}$	I/O$_{34}$	I/O$_{36}$	I/O$_{37}$	I/O$_{42}$	I/O$_{44}$	I/O$_{46}$	I/O$_{49}$	NC

Pin Configurations[20] (continued)

208-Lead PQFP (N208) / CQFP (U208)
Top View



Pin Configurations[20] (continued)

292-Ball PBGA (BG292)
Top View

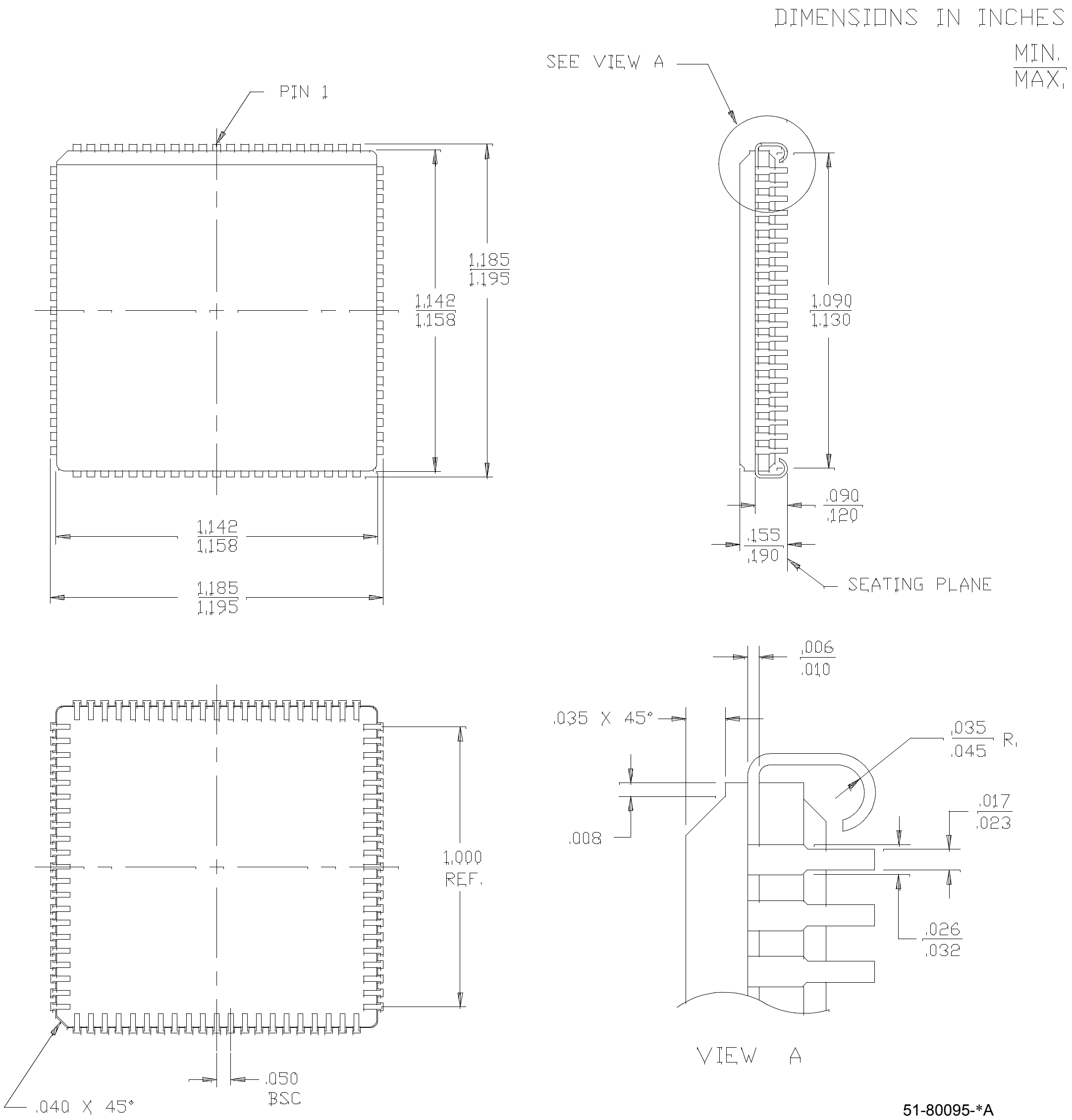
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O$_{21}$	NC	I/O$_{16}$	I/O$_{12}$	I/O$_{9}$	I/O$_{7}$	I/O$_{4}$	I/O$_{0}$	I/O$_{190}$	I/O$_{189}$	I/O$_{186}$	I/O$_{182}$	NC	I/O$_{178}$	I/O$_{175}$	NC	NC	I/O$_{169}$	I/O$_{168}$	A
B	I/O$_{23}$	I/O$_{20}$	I/O$_{19}$	I/O$_{18}$	I/O$_{15}$	I/O$_{11}$	I/O$_{8}$	I/O$_{5}$	I/O$_{1}$	I/O$_{191}$	I/O$_{187}$	I/O$_{185}$	I/O$_{181}$	NC	NC	I/O$_{174}$	I/O$_{171}$	I/O$_{170}$	NC	I/O$_{166}$	B
C	NC	NC	I/O$_{22}$	NC	I/O$_{17}$	I/O$_{14}$	I/O$_{10}$	I/O$_{6}$	I/O$_{2}$	NC	I/O$_{188}$	I/O$_{184}$	I/O$_{180}$	I/O$_{179}$	I/O$_{176}$	I/O$_{173}$	I/O$_{172}$	I/O$_{167}$	I/O$_{165}$	I/O$_{162}$	C
D	I/O$_{24}$	NC	NC	GND	NC	V$_{CCO}$	I/O$_{13}$	GND	I/O$_{3}$	NC	V$_{CC}$	I/O$_{183}$	GND	I/O$_{177}$	V$_{CCO}$	NC	GND	I/O$_{164}$	TDI	I/O$_{160}$	D
E	I/O$_{27}$	I/O$_{26}$	I/O$_{25}$	NC													I/O$_{163}$	I/O$_{161}$	I/O$_{159}$	I/O$_{156}$	E
F	I/O$_{30}$	TCK	I/O$_{28}$	V$_{CCO}$													V$_{CCO}$	I/O$_{158}$	NC	I/O$_{154}$	F
G	I/O$_{33}$	I/O$_{32}$	I/O$_{31}$	I/O$_{29}$													I/O$_{157}$	I/O$_{155}$	I/O$_{153}$	I/O$_{152}$	G
H	I/O$_{35}$	NC	I/O$_{34}$	GND				GND	GND	GND	GND	GND	GND				GND	I/O$_{151}$	I/O$_{150}$	I/O$_{149}$	H
J	I/O$_{39}$	I/O$_{38}$	I/O$_{37}$	I/O$_{36}$				GND	GND	GND	GND	GND	GND				I/O$_{148}$	I/O$_{147}$	I/O$_{146}$	I/O$_{145}$	J
K	I/O$_{42}$	I/O$_{40}$	I/O$_{41}$	V$_{CC}$				GND	GND	GND	GND	GND	GND				I/O$_{144}$	CLK$_{3}$/I$_{4}$	NC	NC	K
L	I/O$_{43}$	I/O$_{44}$	I/O$_{45}$	I/O$_{46}$				GND	GND	GND	GND	GND	GND				V$_{CC}$	CLK$_{2}$/I$_{3}$	I/O$_{143}$	NC	L
M	I/O$_{47}$	CLK$_{0}$/I$_{0}$	CLK$_{1}$/I$_{1}$	I/O$_{48}$				GND	GND	GND	GND	GND	GND				I/O$_{139}$	I/O$_{140}$	I/O$_{141}$	I/O$_{142}$	M
N	I/O$_{49}$	I/O$_{50}$	I/O$_{51}$	GND				GND	GND	GND	GND	GND	GND				GND	I/O$_{136}$	I/O$_{137}$	I/O$_{138}$	N
P	I/O$_{52}$	I/O$_{53}$	I/O$_{55}$	I/O$_{58}$													I/O$_{131}$	I/O$_{133}$	I/O$_{134}$	I/O$_{135}$	P
R	I/O$_{54}$	I/O$_{56}$	I/O$_{59}$	V$_{CCO}$													V$_{CCO}$	I/O$_{130}$	NC	I/O$_{132}$	R
T	I/O$_{57}$	I/O$_{60}$	I/O$_{62}$	I/O$_{65}$													I/O$_{124}$	I/O$_{127}$	I/O$_{128}$	I/O$_{129}$	T
U	I/O$_{61}$	I/O$_{63}$	I/O$_{66}$	GND	I/O$_{76}$	V$_{CCO}$	I/O$_{82}$	GND	I/O$_{91}$	V$_{CC}$	I/O$_{98}$	I/O$_{102}$	GND	I/O$_{112}$	V$_{CCO}$	NC	GND	I/O$_{123}$	I/O$_{122}$	I/O$_{126}$	U
V	I/O$_{64}$	I/O$_{67}$	I/O$_{69}$	I/O$_{75}$	I/O$_{78}$	I/O$_{81}$	I/O$_{85}$	I/O$_{88}$	I/O$_{92}$	I$_{2}$	I/O$_{97}$	I/O$_{101}$	I/O$_{105}$	I/O$_{109}$	I/O$_{113}$	TDO	I/O$_{114}$	I/O$_{117}$	I/O$_{121}$	I/O$_{125}$	V
W	I/O$_{68}$	I/O$_{70}$	I/O$_{72}$	I/O$_{74}$	I/O$_{79}$	I/O$_{83}$	I/O$_{86}$	I/O$_{89}$	I/O$_{93}$	I/O$_{95}$	I/O$_{96}$	I/O$_{100}$	I/O$_{104}$	I/O$_{107}$	I/O$_{110}$	NC	NC	I/O$_{115}$	I/O$_{118}$	I/O$_{120}$	W
Y	I/O$_{71}$	I/O$_{73}$	I/O$_{77}$	TMS	I/O$_{80}$	I/O$_{84}$	I/O$_{87}$	I/O$_{90}$	I/O$_{94}$	NC	NC	I/O$_{99}$	I/O$_{103}$	I/O$_{106}$	I/O$_{108}$	I/O$_{111}$	NC	NC	I/O$_{116}$	I/O$_{119}$	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

3.3V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

Package Diagrams (continued)

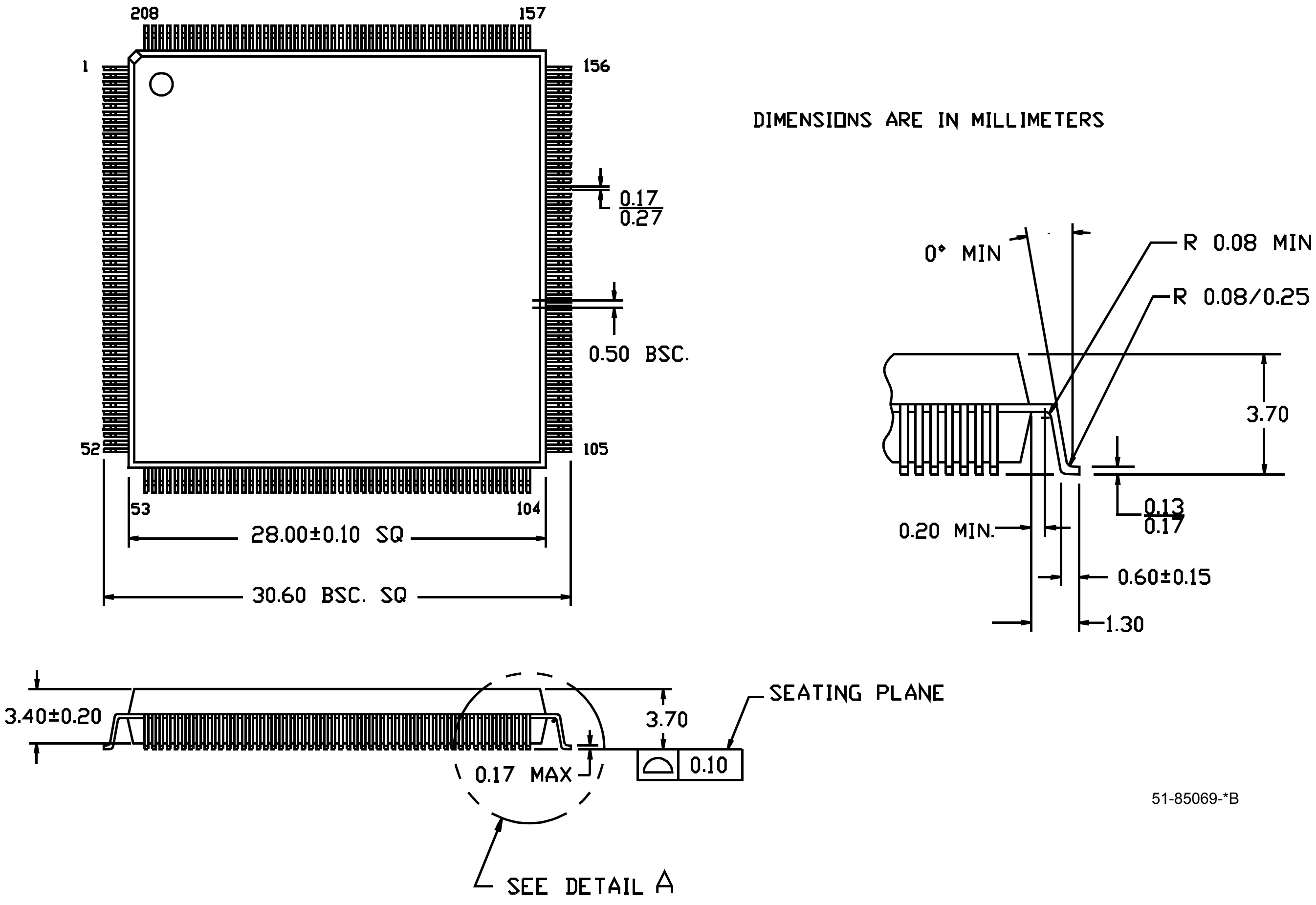
84-Lead Ceramic Leaded Chip Carrier Y84



51-80095-*A

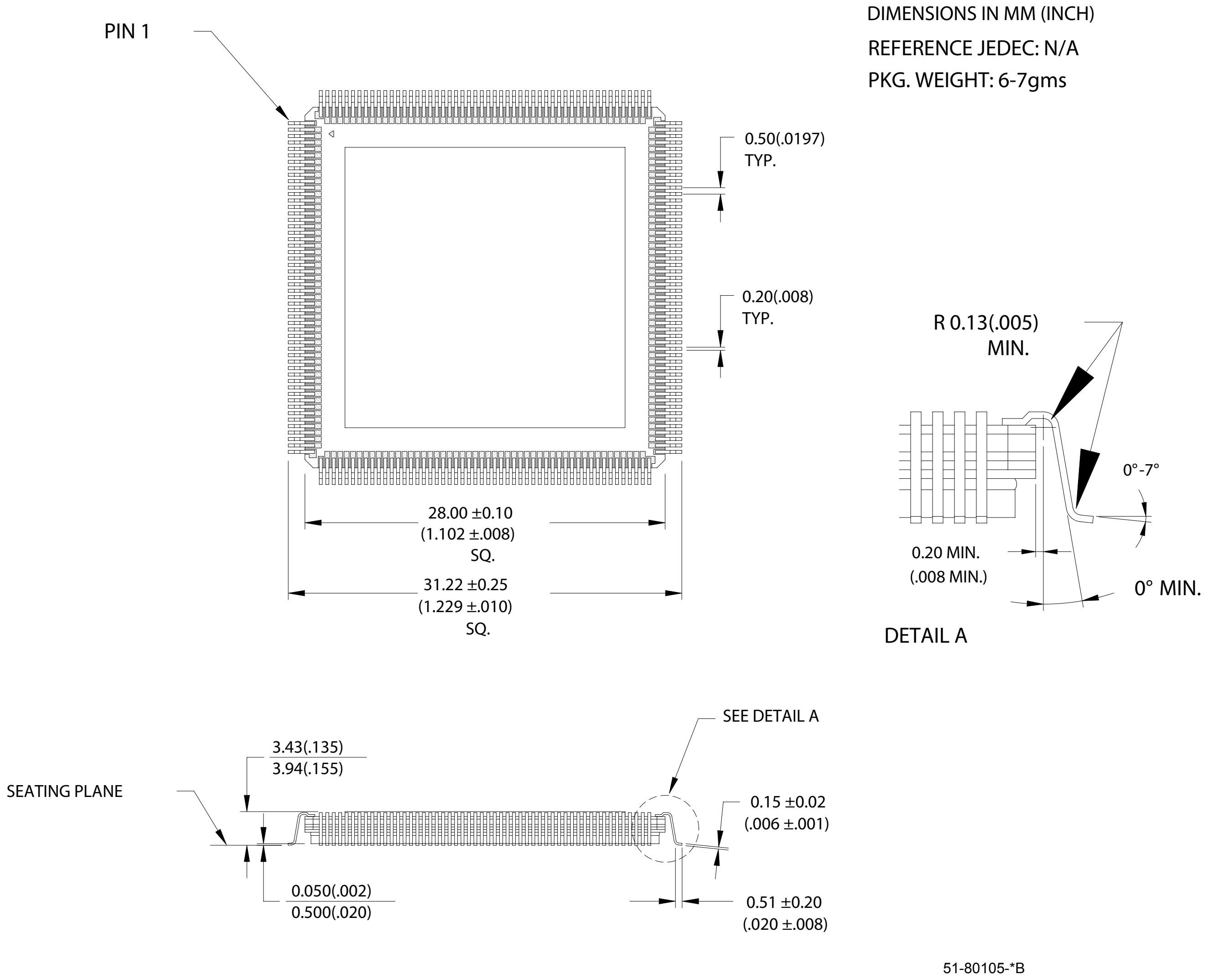
Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



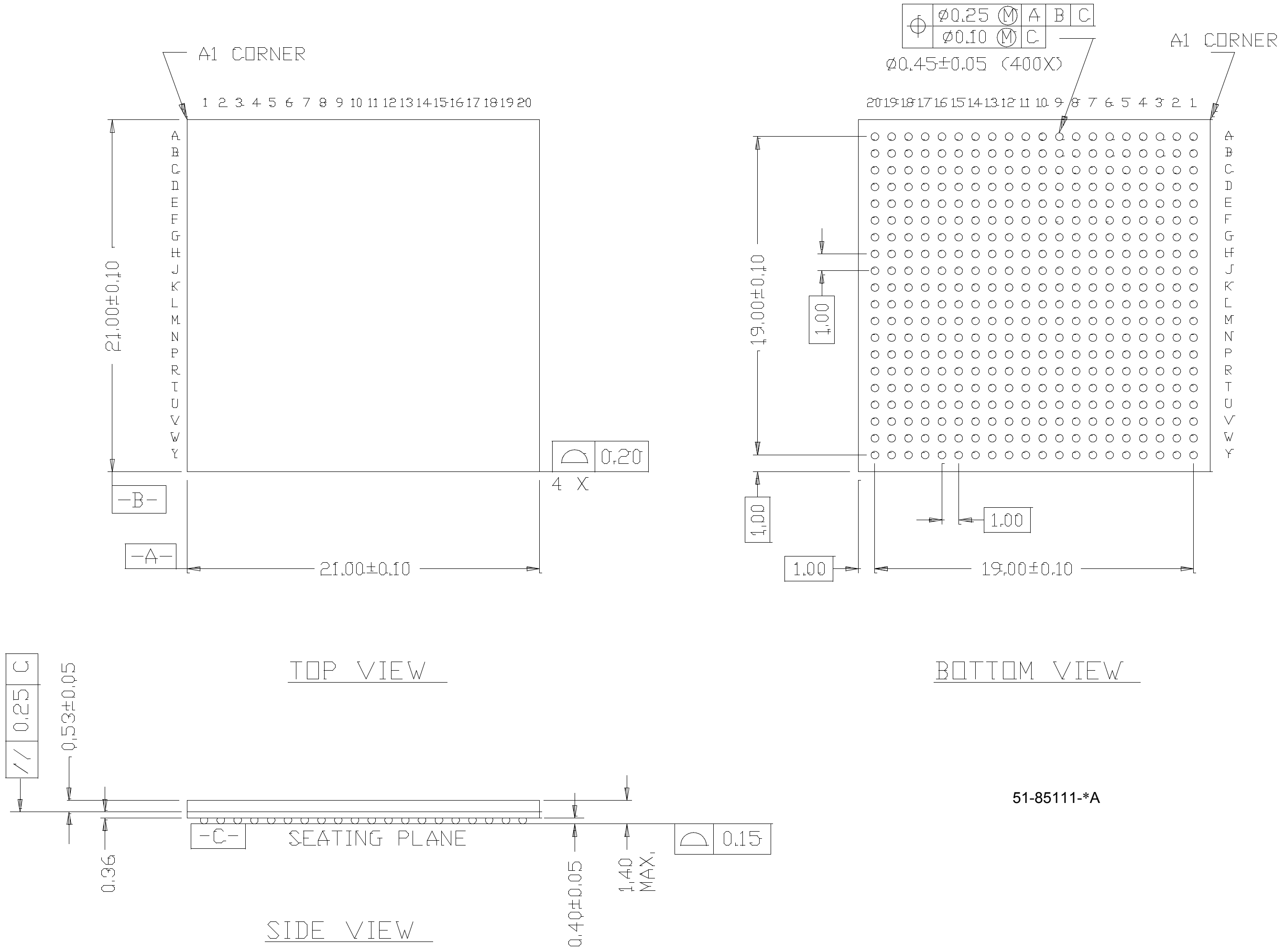
Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208



Package Diagrams (continued)

400-Ball FBGA (21 x 21 x 1.4 mm) BB400



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Document History Page

Document Title: Ultra37000 CPLD Family 5V, 3.3V, ISR™ High-Performance CPLDs
Document Number: 38-03007

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106272	04/18/01	SZV	Change from Spec number: 38-00475 to 38-03007
*A	124942	03/21/03	OOR	Updated 3.3V V_{CC} requirements for –144 speeds Added an Addendum
*B	126262	05/09/03	TEH	Changed pinout for CY37128V BB100 package
*C	128125	07/16/03	HOM	Obsoleted following 3.3V PLCC packaged devices: CY37032VP44-143JC CY37032VP44-100JC CY37032VP44-100JI CY37064VP44-143JC CY37064VP84-143JC CY37064VP44-100JC CY37064VP84-100JC CY37064VP44-100JI CY37064VP84-100JI CY37128VP84-125JC CY37128VP84-83JC CY37128VP84-83JI
*D	282709	See ECN	YDT	Changed package diagrams and labels for consistency Added Lead (Pb)-free logo on first page, as well as a note in Features Added Lead (Pb)-free package diagram labels Added Lead-free Parts to Ordering Information CY37032P44-200AXC, CY37032P44-200JXC, CY37032P44-154AXI, CY37032P44-154JXI, CY37032P44-125AXC, CY37032P44-125JXC, CY37064P44-200AXC, CY37064P44-200JXC, CY37064P100-200AXC, CY37064P44-154AXI, CY37064P44-154JXI, CY37064P44-125AXC, CY37064P44-125JXC, CY37064P100-125AXC, CY37064P44-125AXI, CY37064P100-125AXI, CY37128P84-167JXC, CY37128P100-167AXC, CY37128P160-167AXC, CY37128P84-125JXC, CY37128P100-125AXC, CY37128P160-125AXC, CY37128P84-125JXI, CY37128P100-125AXI, CY37128P160-125AXI, CY37128P84-100JXC, CY37128P100-100AXC, CY37128P160-100AXC, CY37128P100-100AXI, CY37192P160-154AXC, CY37192P160-125AXC, CY37192P160-125AXI, CY37192P160-83AXC, CY37192P160-83AXI, CY37256P160-154AXC, CY37256P160-125AXC, CY37256P160-125AXI, CY37256P160-83AXC, CY37256P160-83AXI, CY37032VP44-143AXC, CY37032VP44-100AXC, CY37032VP44-100AXI, CY37032VP44-100JXI, CY37064VP44-143AXC, CY37064VP100-143AXC, CY37064VP44-100AXC, CY37064VP100-100AXC, CY37064VP44-100AXI, CY37064VP100-100AXI, CY37128VP100-125AXC, CY37128VP160-125AXC, CY37128VP160-125AXI, CY37128VP100-83AXC, CY37128VP160-83AXC, CY37128VP100-83AXI, CY37128VP160-83AXI, CY37192VP160-100AXC, CY37192VP160-66AXC, CY37256VP160-100AXC, CY37256VP160-100AXI, CY37256VP160-66AXC
*E	321635	See ECN	PCX	Added Package Diagram BG292 Updated all PBGA package type information (BG292 & BG388)