Infineon Technologies - CY37192VP160-100AXC Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	192
Number of Gates	-
Number of I/O	125
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37192vp160-100axc

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V					X		X	
CY37192V						X		X
CY37256V						X		X
CY37384V							X	X
CY37512V							X	X

Device-Package Offering and I/O Count

Device	44-Lead TQFP	44-Lead CLCC	48-Lead FBGA	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	292-Lead PBGA	256-Lead FBGA	388-Lead PBGA	400-Lead FBGA
CY37032V	37		37											
CY37064V	37	37	37		69	69								
CY37128V				69	69	85	133							
CY37192V							125							
CY37256V							133	133	165		197	197		
CY37384V									165		197			
CY37512V									165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The PIM consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*® and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note *Understanding Bus-Hold—A Feature of Cypress CPLDs*.

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

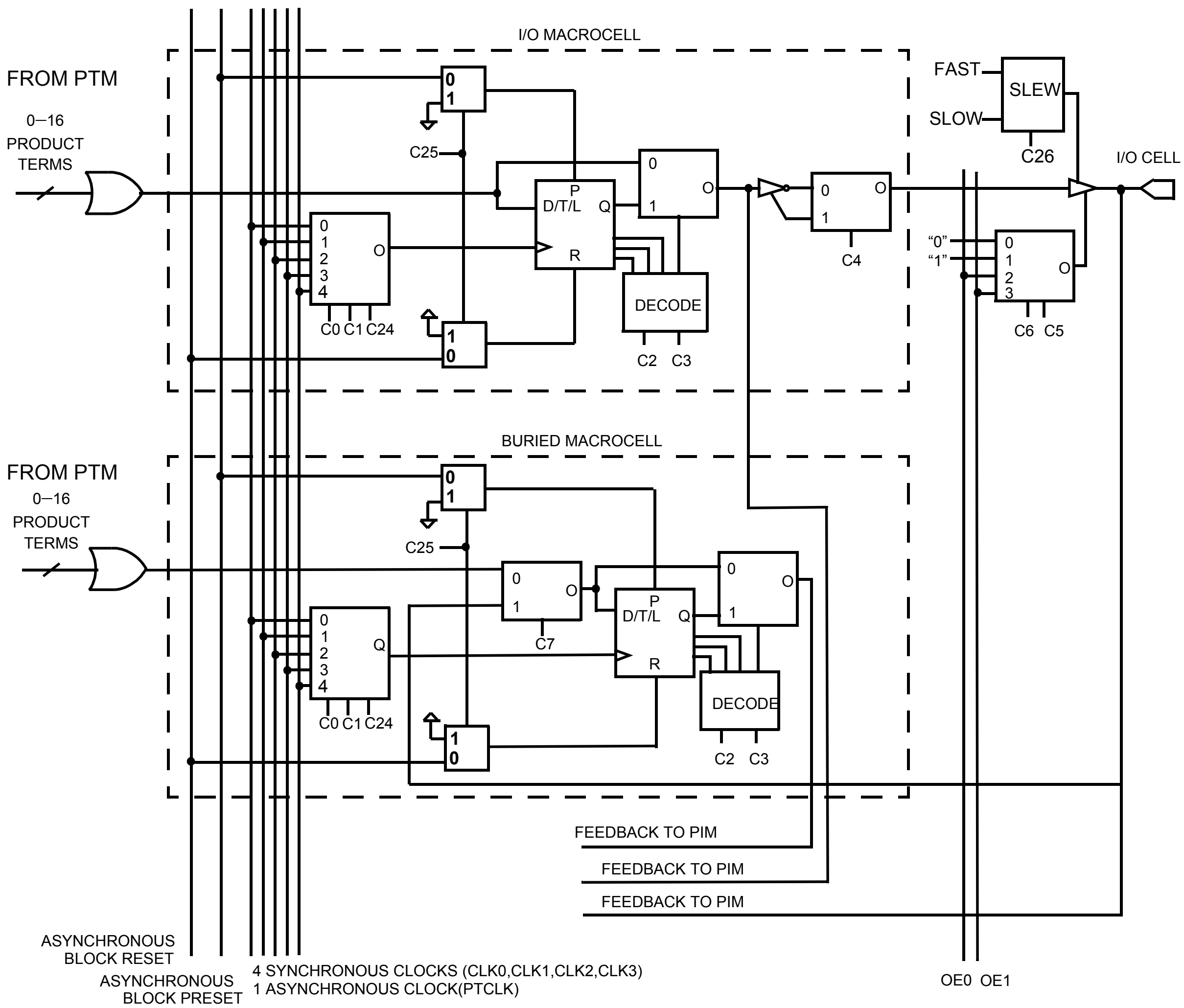
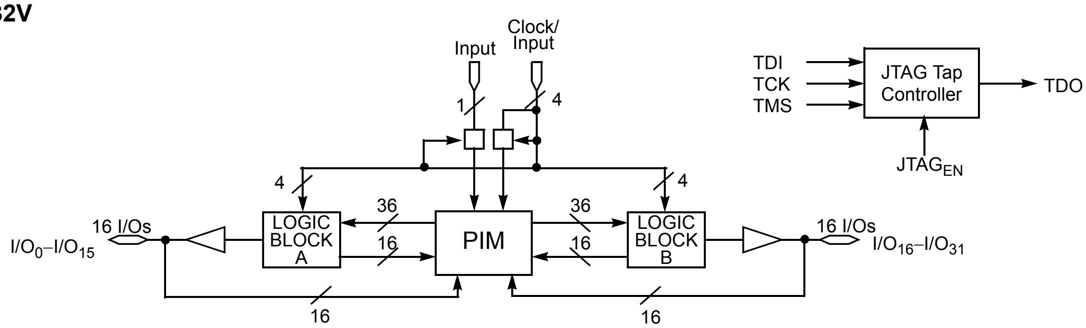


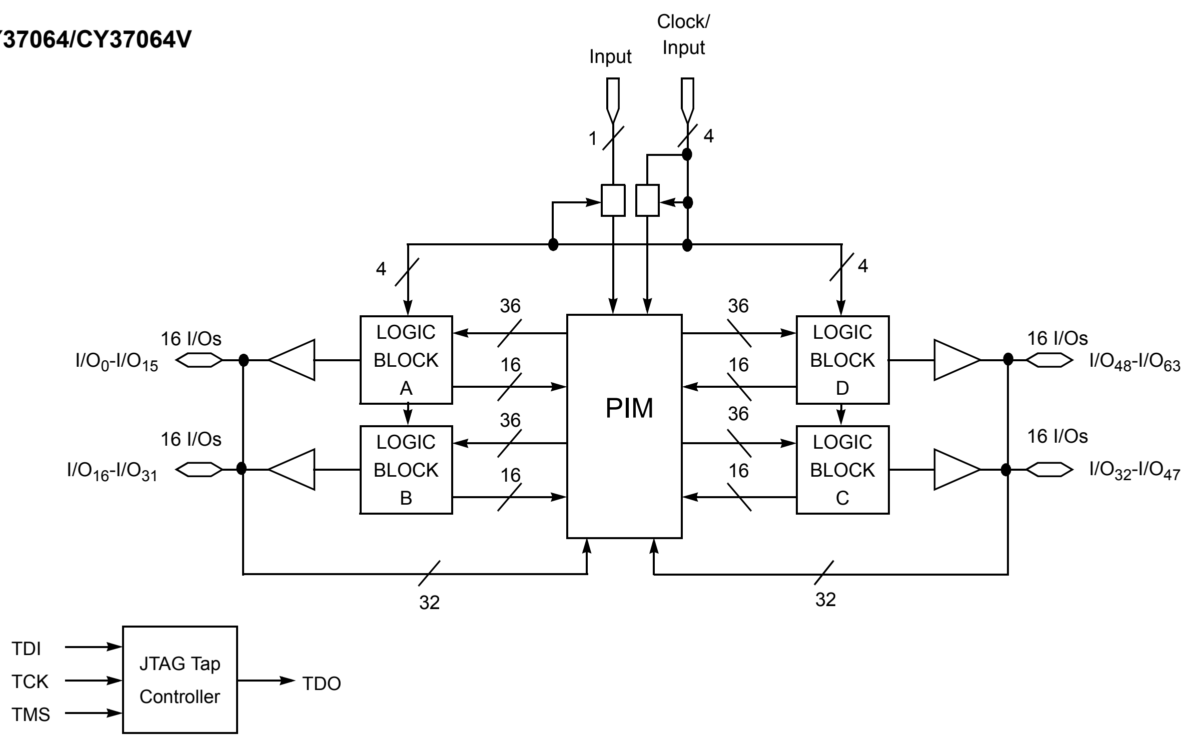
Figure 2. I/O and Buried Macrocells

Logic Block Diagrams

CY37032/CY37032V

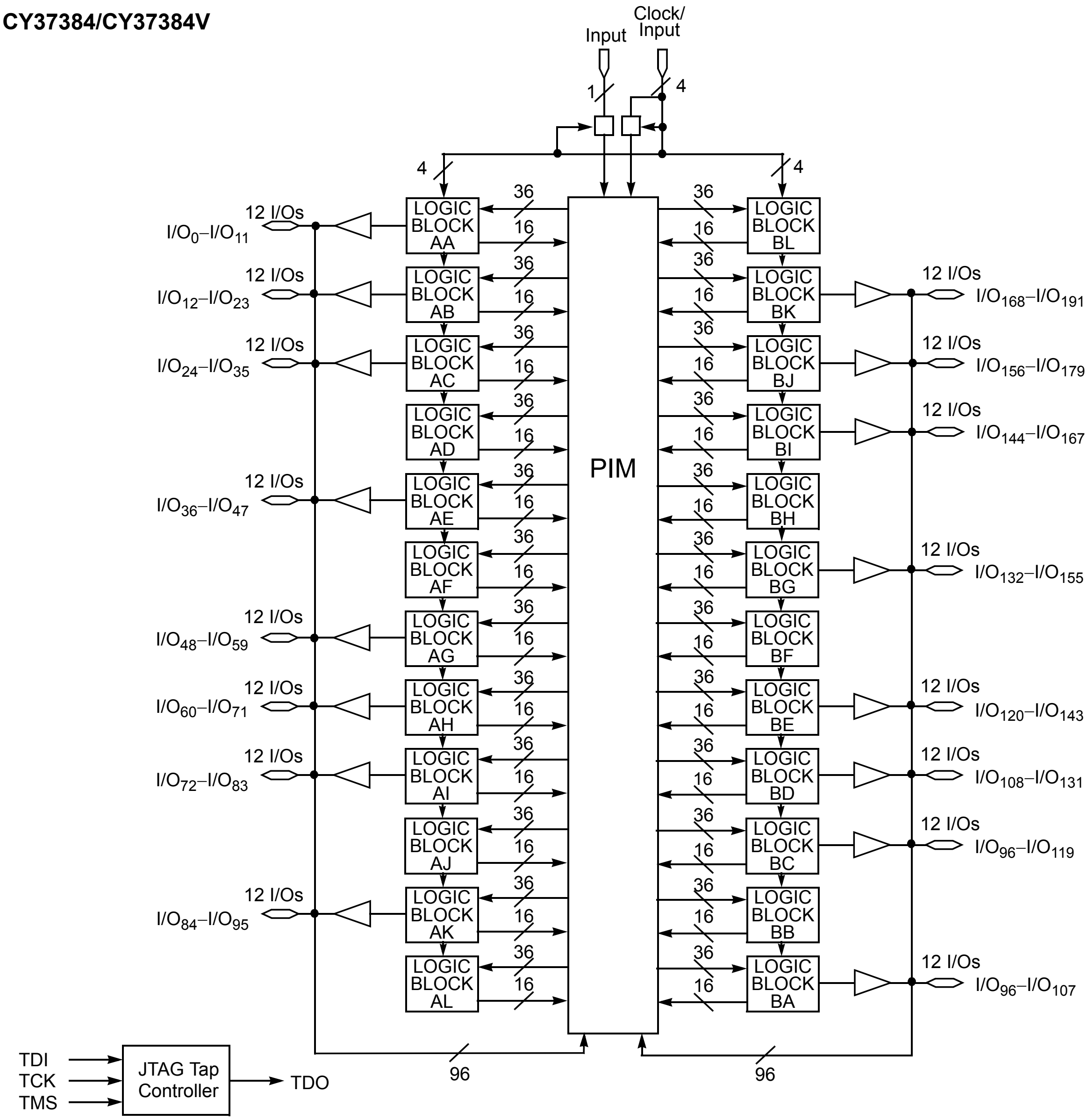


CY37064/CY37064V



Logic Block Diagrams (continued)

CY37384/CY37384V



Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

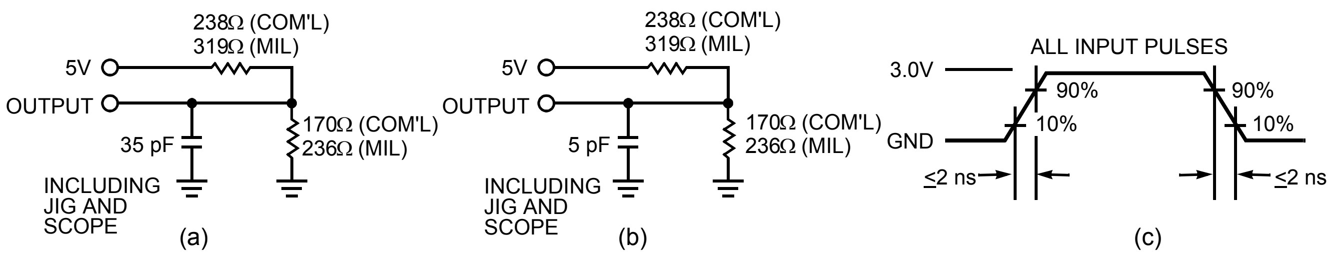
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

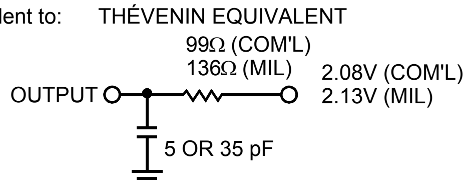
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Characteristics

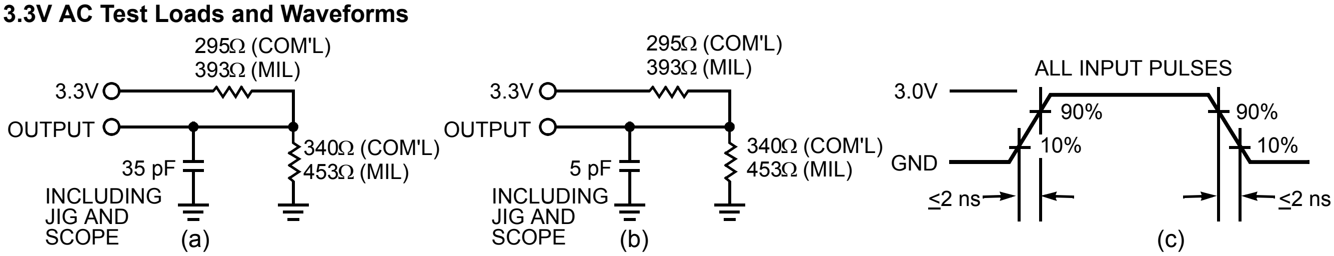
5.0V AC Test Loads and Waveforms



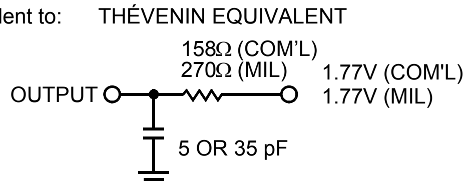
Equivalent to: THÉVENIN EQUIVALENT

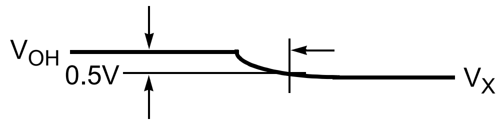
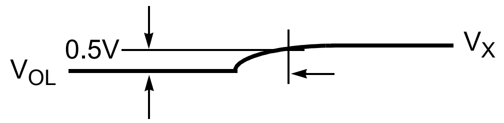
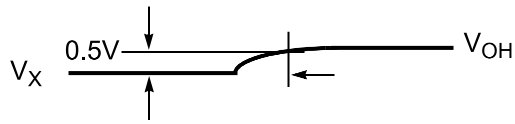
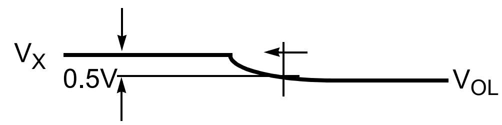


3.3V AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter[11]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

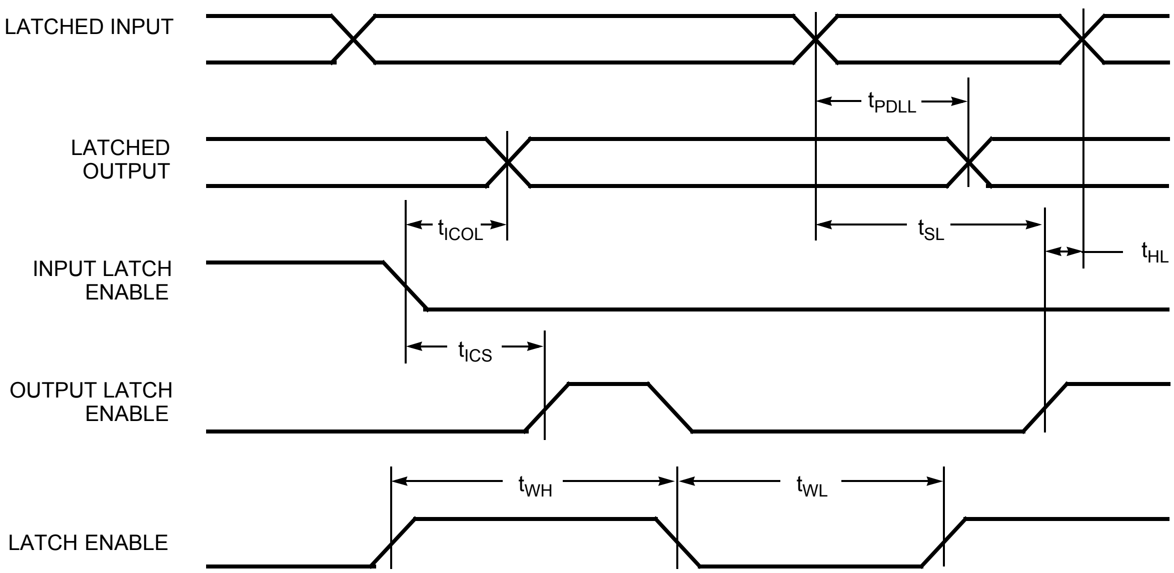
Switching Characteristics Over the Operating Range [12]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t_{PD}[13, 14, 15]	Input to Combinatorial Output	ns
t_{PDL}[13, 14, 15]	Input to Output Through Transparent Input or Output Latch	ns
t_{PDLL}[13, 14, 15]	Input to Output Through Transparent Input and Output Latches	ns
t_{EA}[13, 14, 15]	Input to Output Enable	ns
t_{ER}[11, 13]	Input to Output Disable	ns
Input Register Parameters		
t_{WL}	Clock or Latch Enable Input LOW Time[8]	ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	ns
t_{IS}	Input Register or Latch Set-up Time	ns
t_{IH}	Input Register or Latch Hold Time	ns
t_{ICO}[13, 14, 15]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t_{ICOL}[13, 14, 15]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t_{CO}[14, 15]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output	ns
t_S[13]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_H	Register or Latch Data Hold Time	ns
t_{CO2}[13, 14, 15]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t_{SCS}[13]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	ns
t_{SL}[13]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns

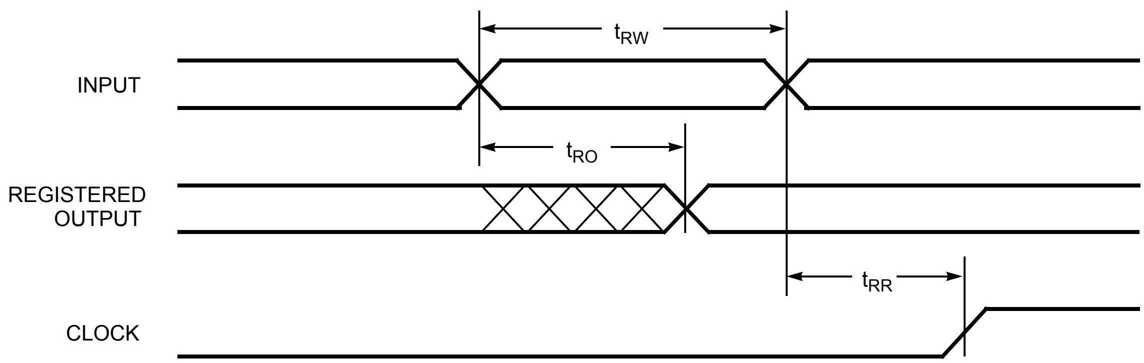
Notes:
11. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.
12. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
13. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
14. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
15. When V_{CCO} = 3.3V, add $t_{3.3IO}$ to this spec.

Switching Waveforms (continued)

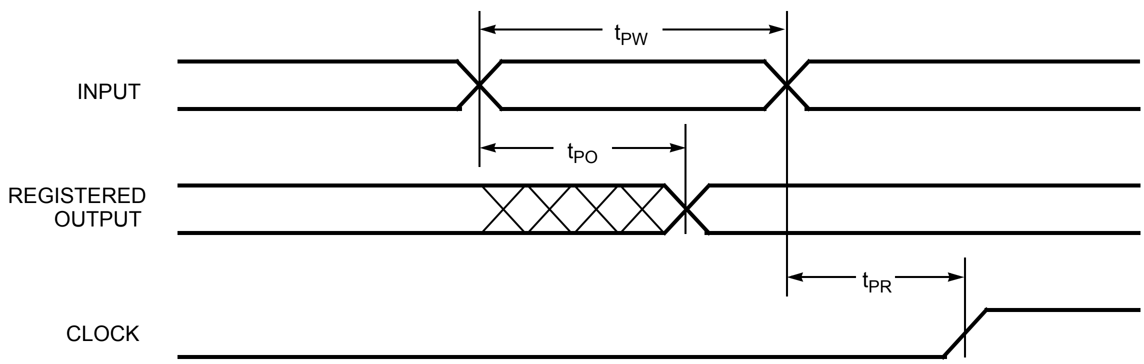
Latched Input and Output



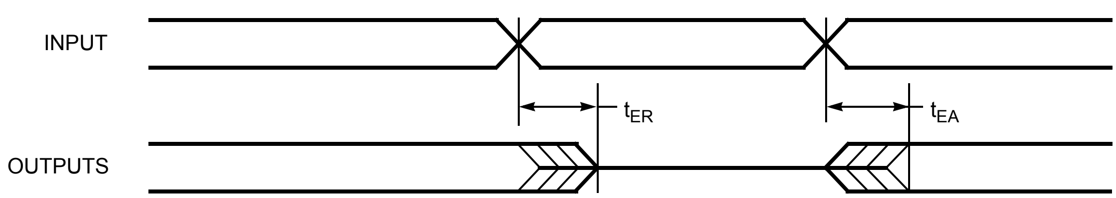
Asynchronous Reset



Asynchronous Preset



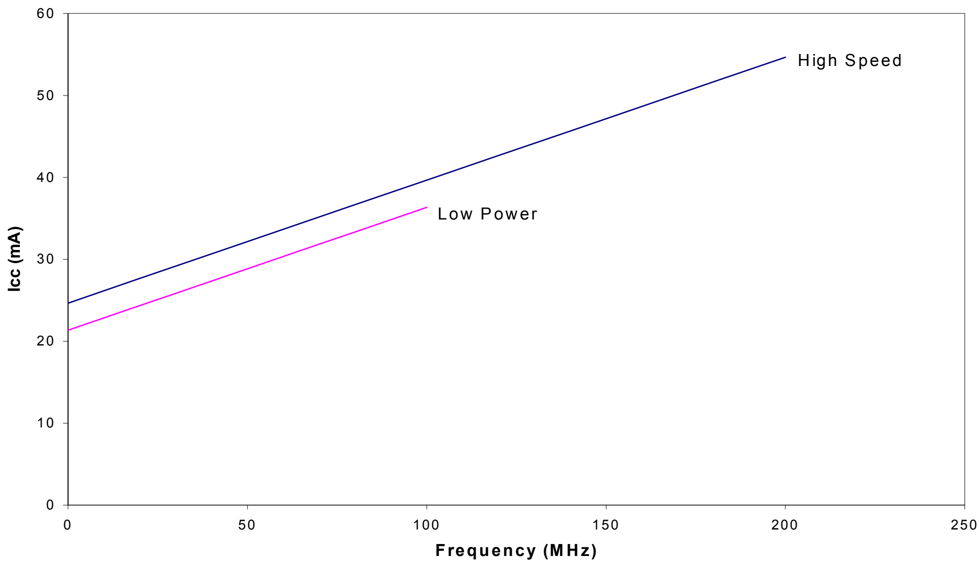
Output Enable/Disable



Power Consumption

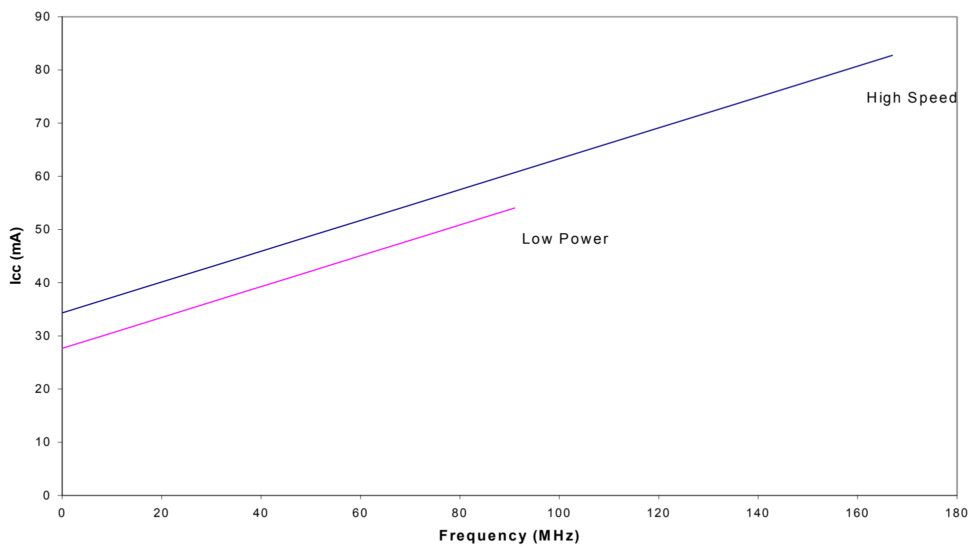
Typical 5.0V Power Consumption

CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

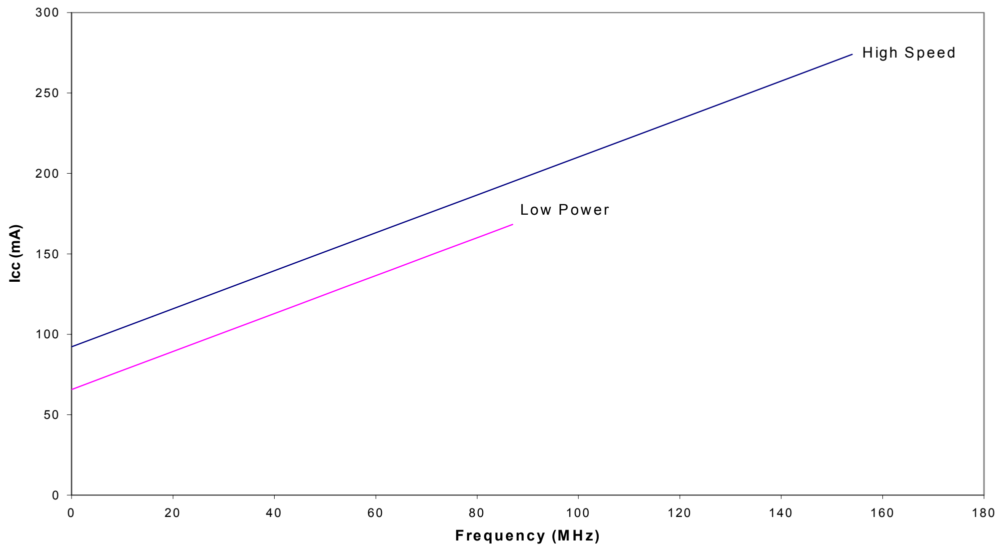
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

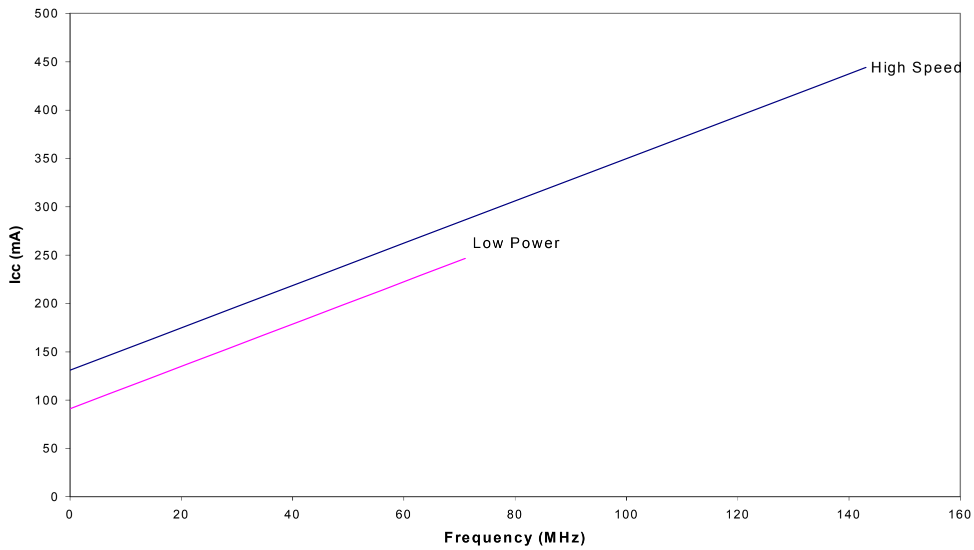
Typical 5.0V Power Consumption (continued)

CY37256



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

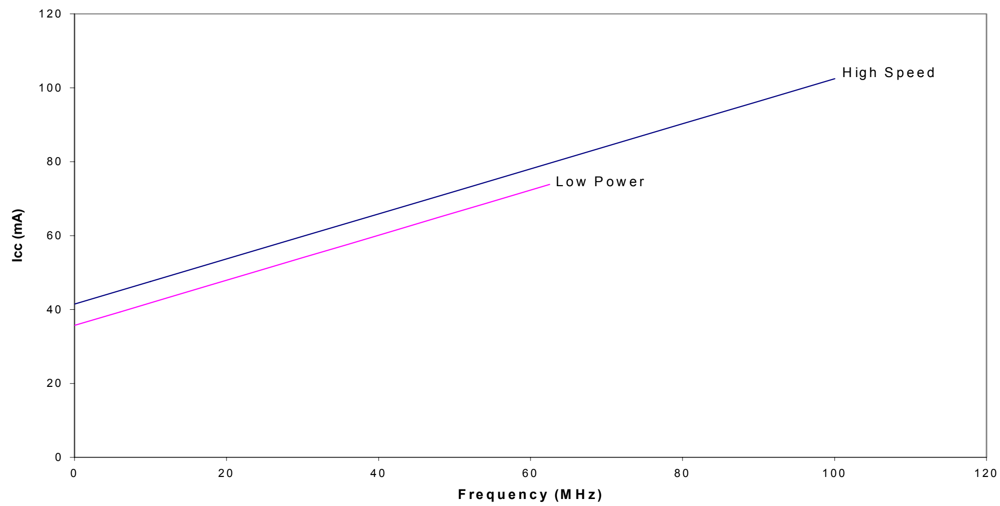
CY37384



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

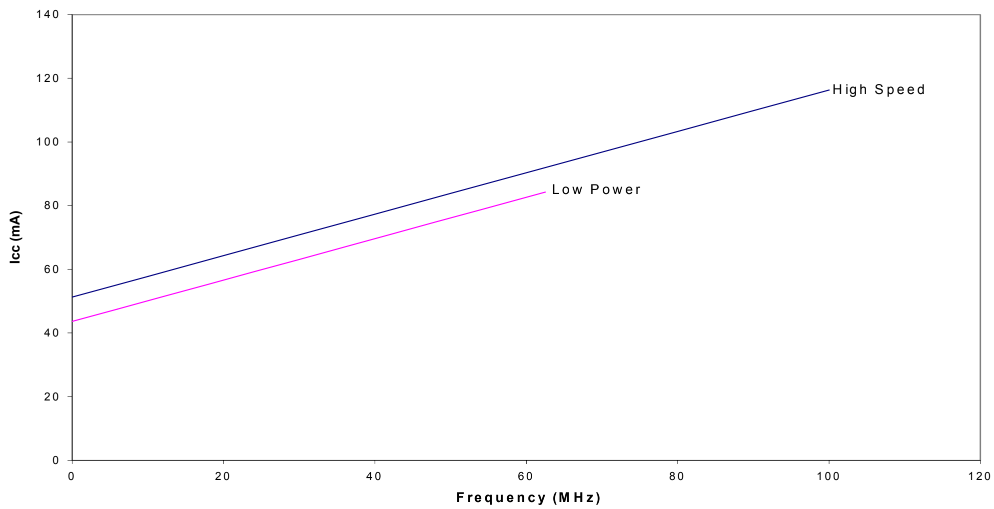
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

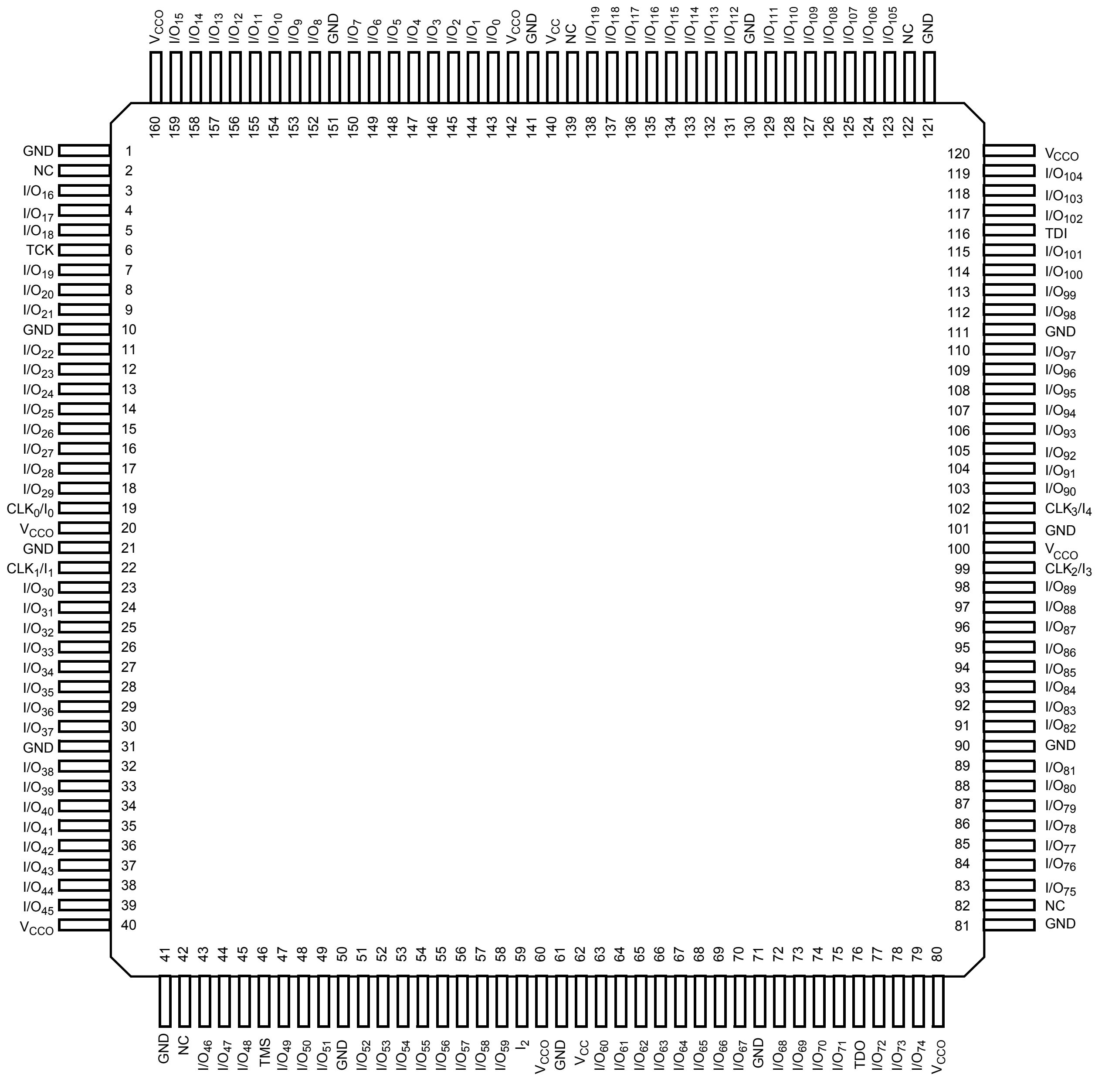
CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

Pin Configurations[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[20] (continued)

256-Ball Fine-Pitch BGA (BB256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	I/O$_{26}$	I/O$_{24}$	I/O$_{20}$	V$_{CC}$	I/O$_{11}$	GND	GND	I/O$_{186}$	V$_{CC}$	I/O$_{177}$	I/O$_{172}$	I/O$_{167}$	GND	GND
B	GND	I/O$_{27}$	I/O$_{25}$	I/O$_{23}$	I/O$_{19}$	I/O$_{15}$	I/O$_{10}$	GND	GND	I/O$_{185}$	I/O$_{181}$	I/O$_{176}$	I/O$_{171}$	I/O$_{166}$	I/O$_{165}$	GND
C	I/O$_{29}$	I/O$_{28}$	NC	I/O$_{22}$	I/O$_{18}$	I/O$_{14}$	I/O$_{9}$	I/O$_{4}$	I/O$_{191}$	I/O$_{184}$	I/O$_{180}$	I/O$_{175}$	I/O$_{170}$	NC	I/O$_{163}$	I/O$_{164}$
D	I/O$_{32}$	I/O$_{31}$	I/O$_{30}$	NC	I/O$_{17}$	I/O$_{13}$	I/O$_{8}$	I/O$_{3}$	I/O$_{190}$	I/O$_{183}$	I/O$_{179}$	I/O$_{174}$	I/O$_{169}$	I/O$_{160}$	I/O$_{161}$	I/O$_{162}$
E	I/O$_{35}$	I/O$_{34}$	I/O$_{33}$	I/O$_{21}$	I/O$_{16}$	I/O$_{12}$	I/O$_{7}$	I/O$_{2}$	I/O$_{189}$	V$_{CC}$	I/O$_{178}$	I/O$_{173}$	I/O$_{168}$	I/O$_{157}$	I/O$_{158}$	I/O$_{159}$
F	V$_{CC}$	I/O$_{38}$	I/O$_{37}$	I/O$_{36}$	TCK	V$_{CC}$	I/O$_{6}$	I/O$_{1}$	I/O$_{188}$	I/O$_{182}$	V$_{CC}$	TDI	I/O$_{154}$	I/O$_{155}$	I/O$_{156}$	V$_{CC}$
G	I/O$_{43}$	I/O$_{42}$	I/O$_{41}$	I/O$_{40}$	V$_{CC}$	I/O$_{39}$	I/O$_{5}$	I/O$_{0}$	I/O$_{187}$	I/O$_{148}$	I/O$_{149}$	CLK$_{3}$ /I$_{4}$	I/O$_{150}$	I/O$_{151}$	I/O$_{152}$	I/O$_{153}$
H	GND	GND	I/O$_{47}$	I/O$_{46}$	CLK$_{0}$ /I$_{0}$	I/O$_{45}$	I/O$_{44}$	GND	GND	I/O$_{144}$	I/O$_{145}$	CLK$_{2}$ /I$_{3}$	I/O$_{146}$	I/O$_{147}$	GND	GND
J	GND	GND	I/O$_{51}$	I/O$_{50}$	NC	I/O$_{49}$	I/O$_{48}$	GND	GND	I/O$_{140}$	I/O$_{141}$	I$_{2}$	I/O$_{142}$	I/O$_{143}$	GND	GND
K	I/O$_{57}$	I/O$_{56}$	I/O$_{55}$	I/O$_{54}$	CLK$_{1}$ /I$_{1}$	I/O$_{53}$	I/O$_{52}$	I/O$_{91}$	I/O$_{96}$	I/O$_{101}$	I/O$_{135}$	V$_{CC}$	I/O$_{136}$	I/O$_{137}$	I/O$_{138}$	I/O$_{139}$
L	V$_{CC}$	I/O$_{60}$	I/O$_{59}$	I/O$_{58}$	TMS	V$_{CC}$	I/O$_{86}$	I/O$_{92}$	I/O$_{97}$	I/O$_{102}$	V$_{CC}$	TDO	I/O$_{132}$	I/O$_{133}$	I/O$_{134}$	V$_{CC}$
M	I/O$_{63}$	I/O$_{62}$	I/O$_{61}$	I/O$_{72}$	I/O$_{77}$	I/O$_{82}$	V$_{CC}$	I/O$_{93}$	I/O$_{98}$	I/O$_{103}$	I/O$_{108}$	I/O$_{112}$	I/O$_{117}$	I/O$_{129}$	I/O$_{130}$	I/O$_{131}$
N	I/O$_{66}$	I/O$_{65}$	I/O$_{64}$	I/O$_{73}$	I/O$_{78}$	I/O$_{83}$	I/O$_{87}$	I/O$_{94}$	I/O$_{99}$	I/O$_{104}$	I/O$_{109}$	I/O$_{113}$	NC	I/O$_{126}$	I/O$_{127}$	I/O$_{128}$
P	I/O$_{68}$	I/O$_{67}$	NC	I/O$_{74}$	I/O79	I/O$_{84}$	I/O$_{88}$	I/O$_{95}$	I/O$_{100}$	I/O$_{105}$	I/O$_{110}$	I/O$_{114}$	I/O$_{118}$	NC	I/O$_{124}$	I/O$_{125}$
R	GND	I/O$_{69}$	I/O$_{70}$	I/O$_{75}$	I/O$_{80}$	I/O$_{85}$	I/O$_{89}$	GND	GND	I/O$_{106}$	I/O$_{111}$	I/O$_{115}$	I/O$_{119}$	I/O$_{121}$	I/O$_{123}$	GND
T	GND	GND	I/O$_{71}$	I/O$_{76}$	I/O$_{81}$	V$_{CC}$	I/O$_{90}$	GND	GND	I/O$_{107}$	V$_{CC}$	I/O$_{116}$	I/O$_{120}$	I/O$_{122}$	GND	GND

5.0V Ordering Information (continued)

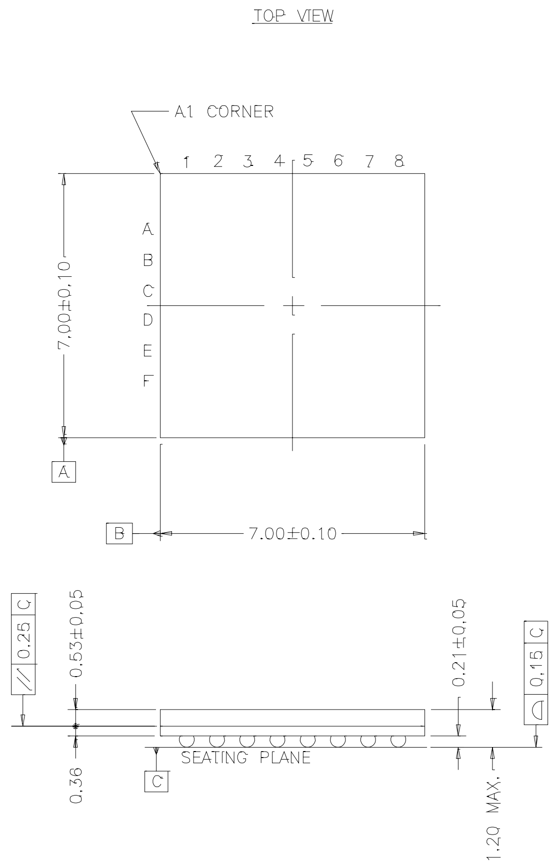
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	154	CY37256P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-154AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-154NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-154BGC	BG292	292-Ball Plastic Ball Grid Array	
	125	CY37256P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952302QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
	83	CY37256P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952301QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	125	CY37384P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
	83	CY37384P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	

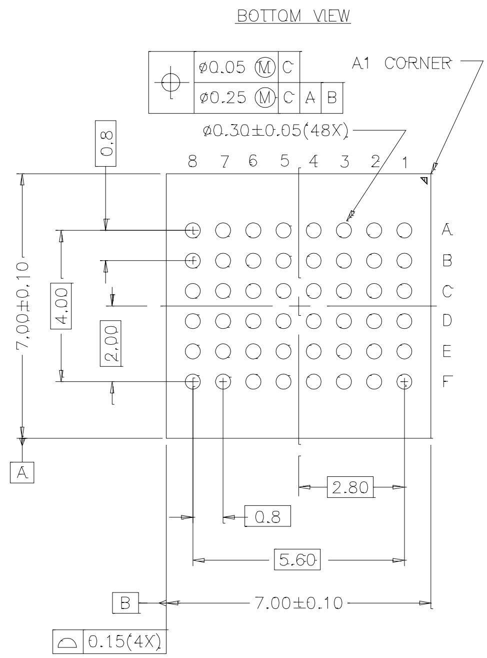
3.3V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

Package Diagrams (continued)

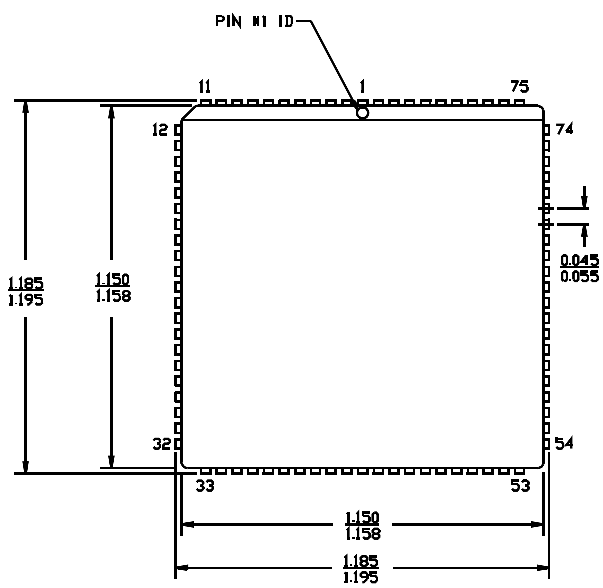
48-Ball (7.0 mm x 7.0 mm x 1.2 mm, 0.80 pitch) Thin BGA BA48D

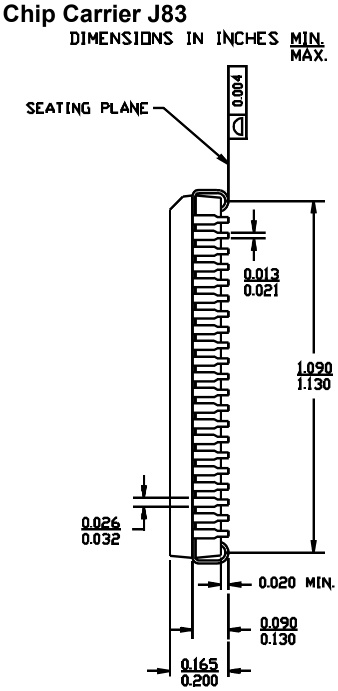




51-85109-*C

84-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J83

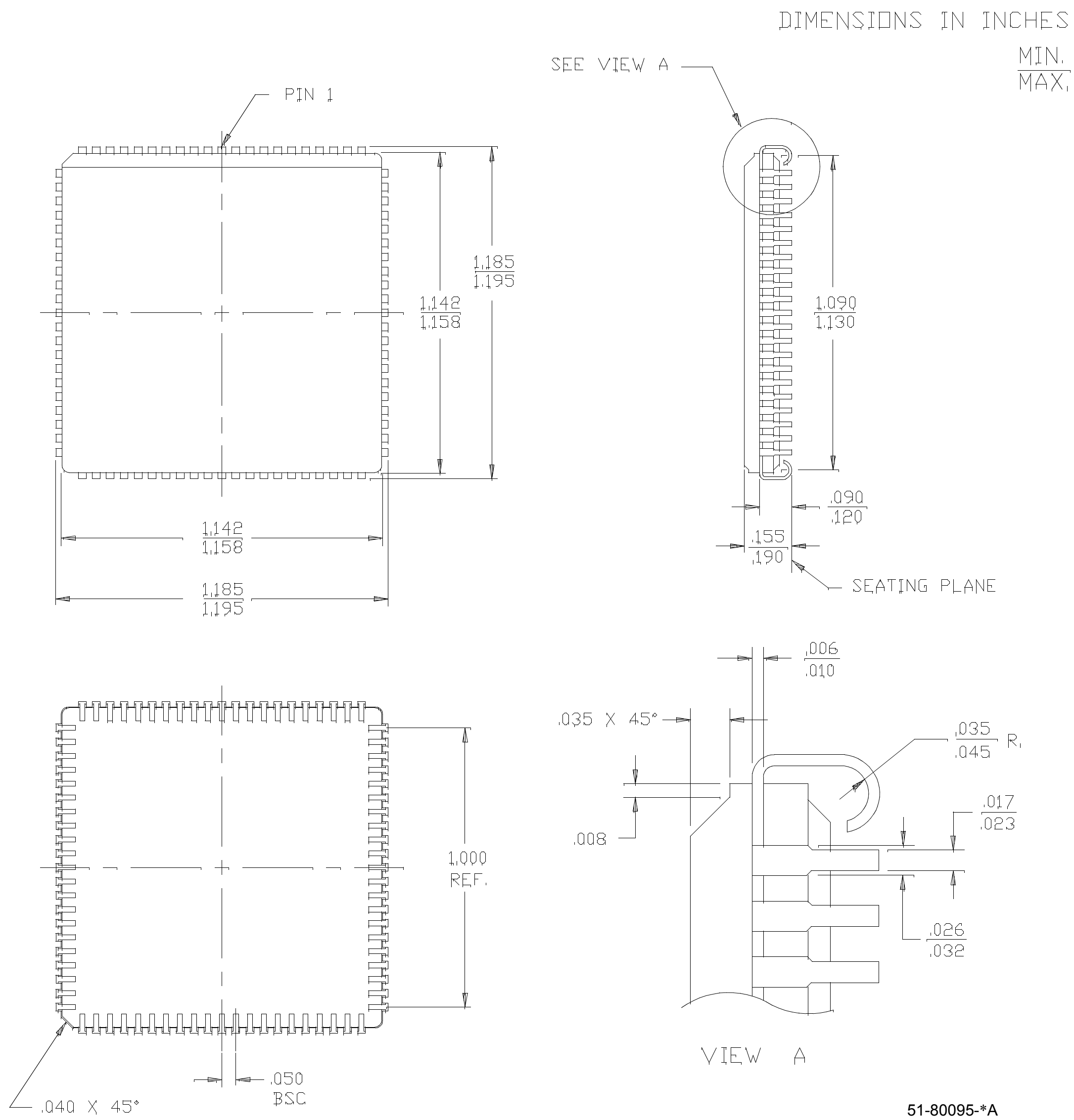




51-85006-*A

Package Diagrams (continued)

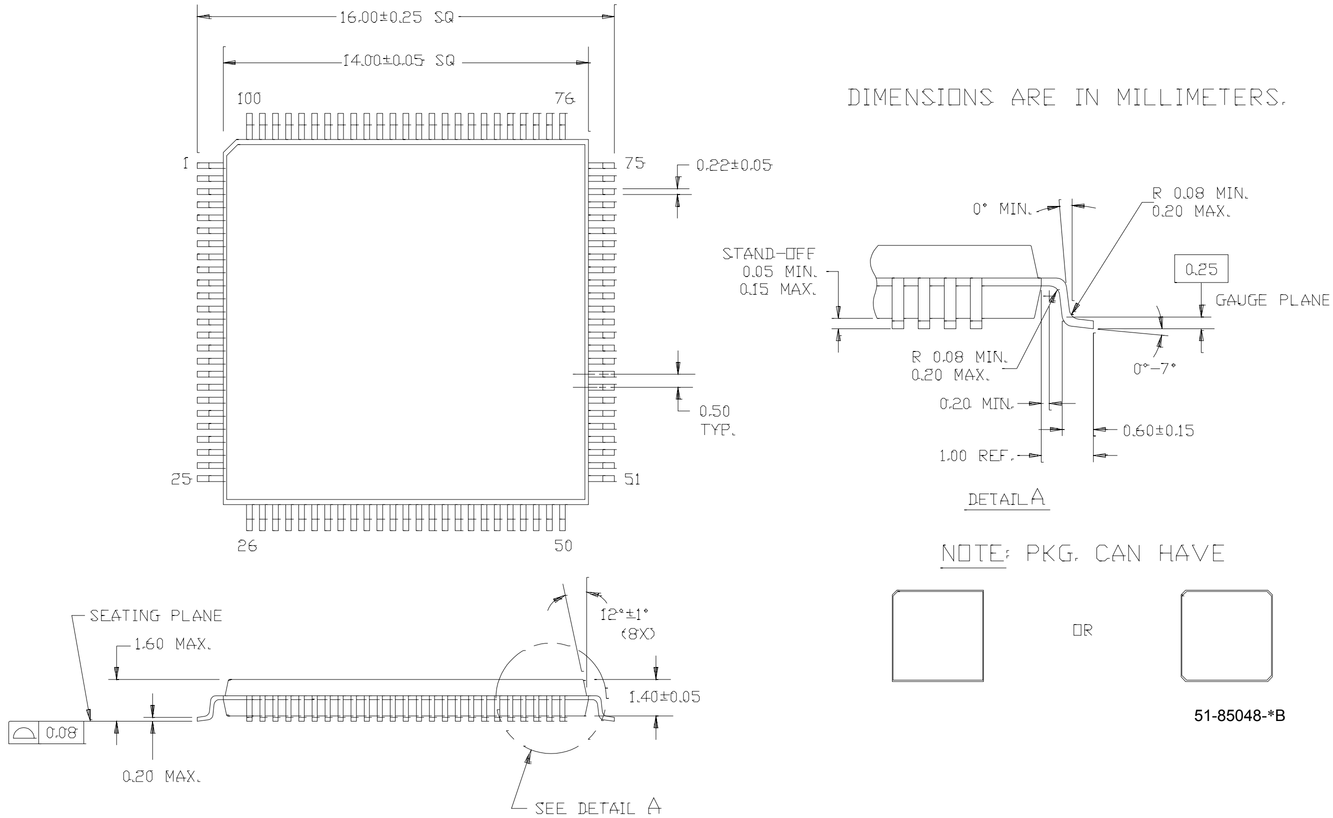
84-Lead Ceramic Leaded Chip Carrier Y84



51-80095-*A

Package Diagrams (continued)

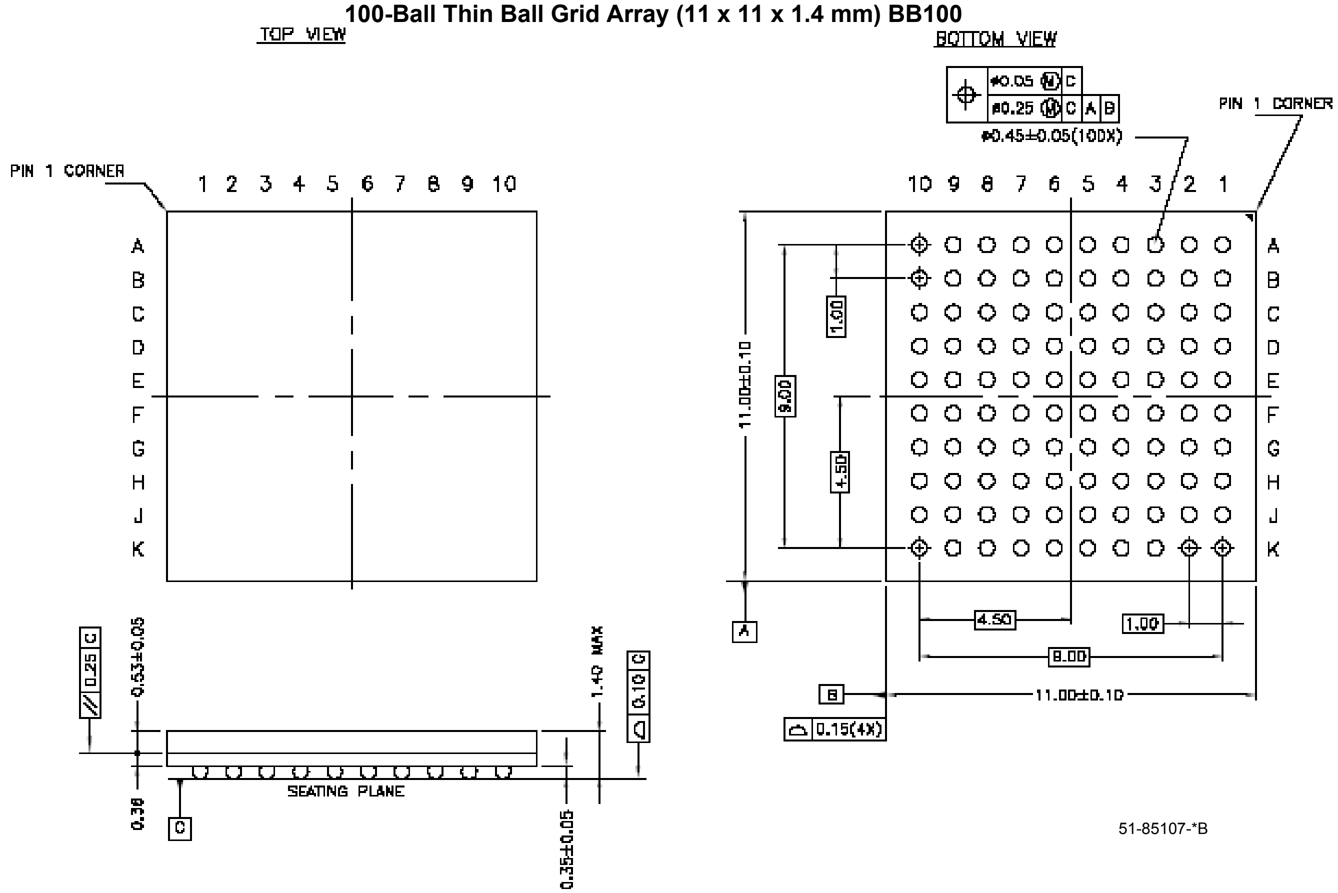
100-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (TQFP) A100



51-85048-*B

Package Diagrams (continued)

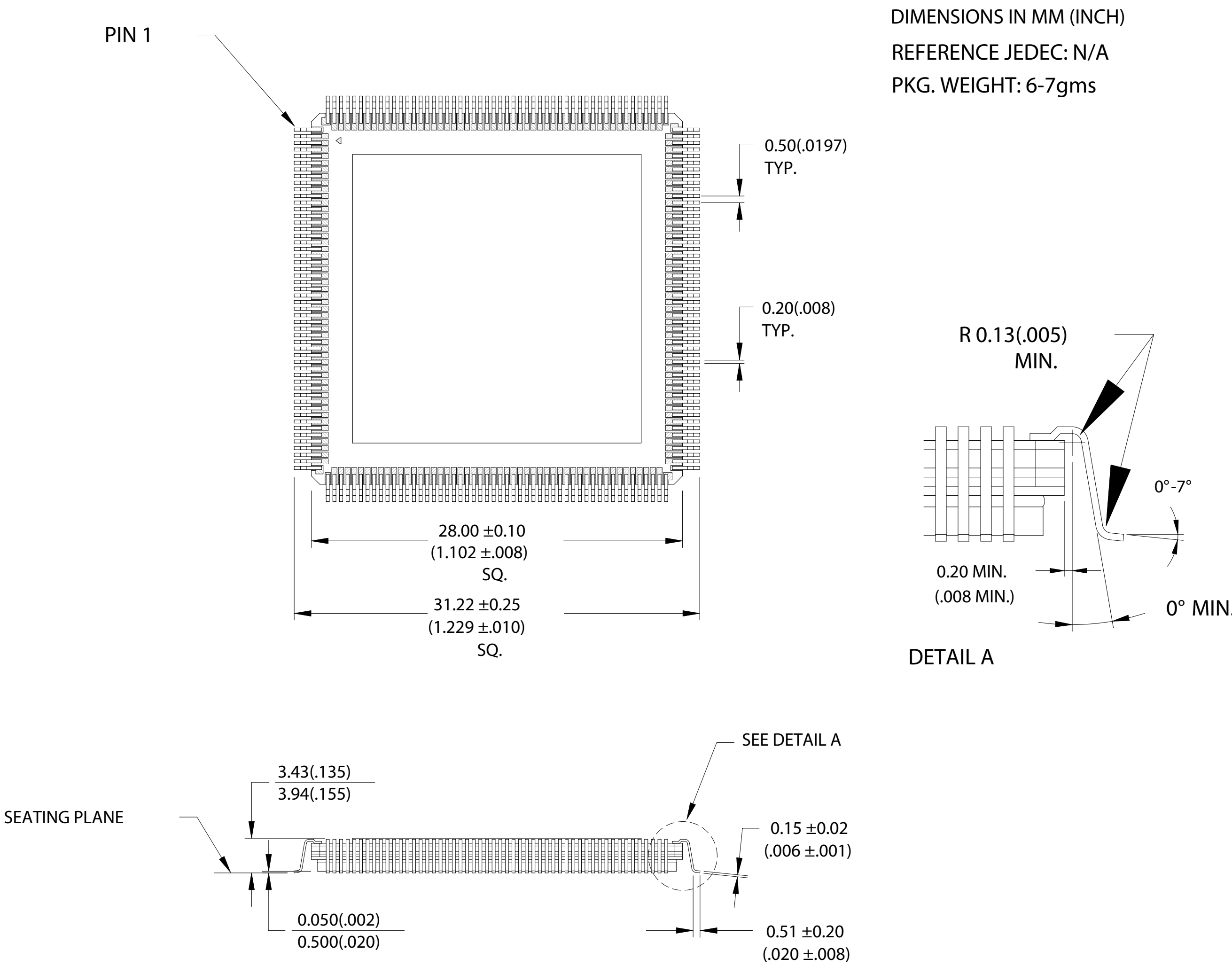
100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



51-85107-*B

Package Diagrams (continued)

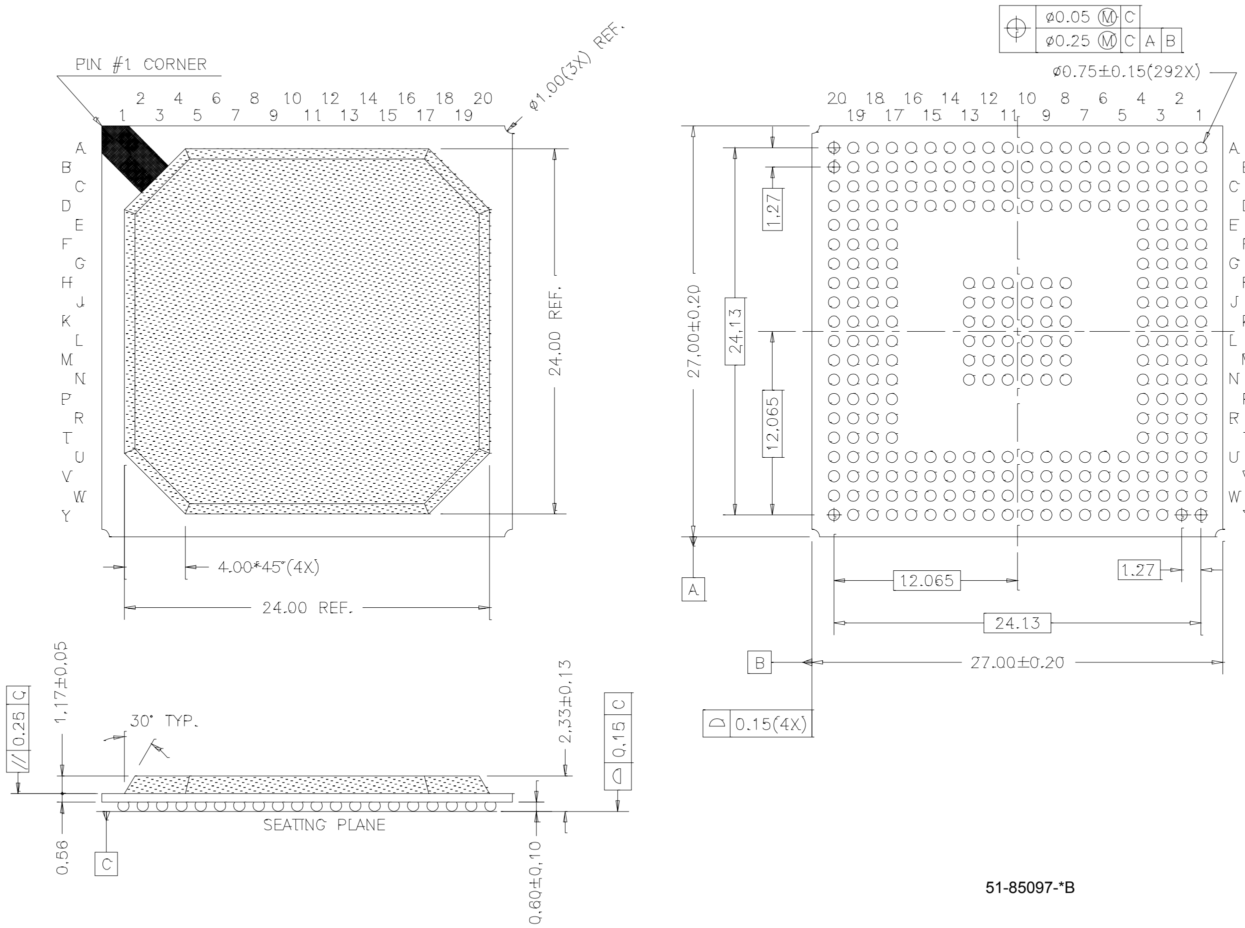
208-Lead Ceramic Quad Flatpack (Cavity Up) U208



51-80105-*B

Package Diagrams (continued)

292-Ball Plastic Ball Grid Array PBGA (27 x 27 x 2.33 mm) BG292



51-85097-*B