



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	192
Number of Gates	-
Number of I/O	125
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37192vp160-66axc

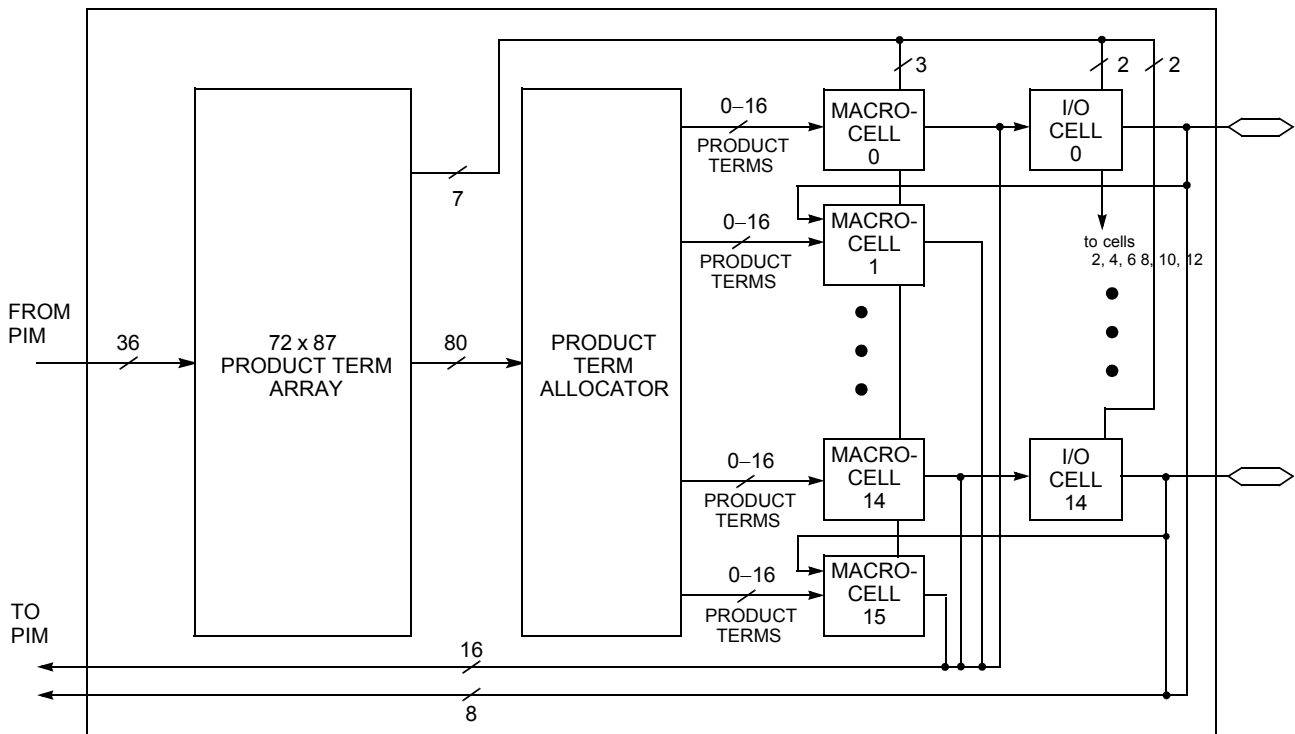


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a

variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.



Ultra37000 CPLD Family

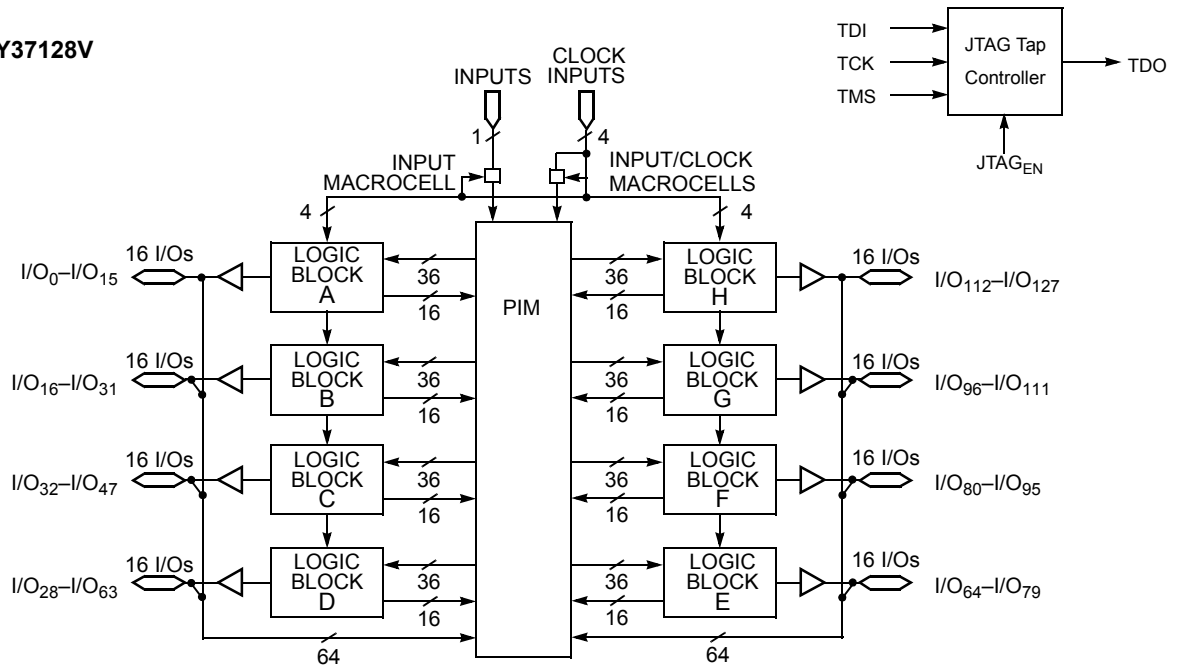
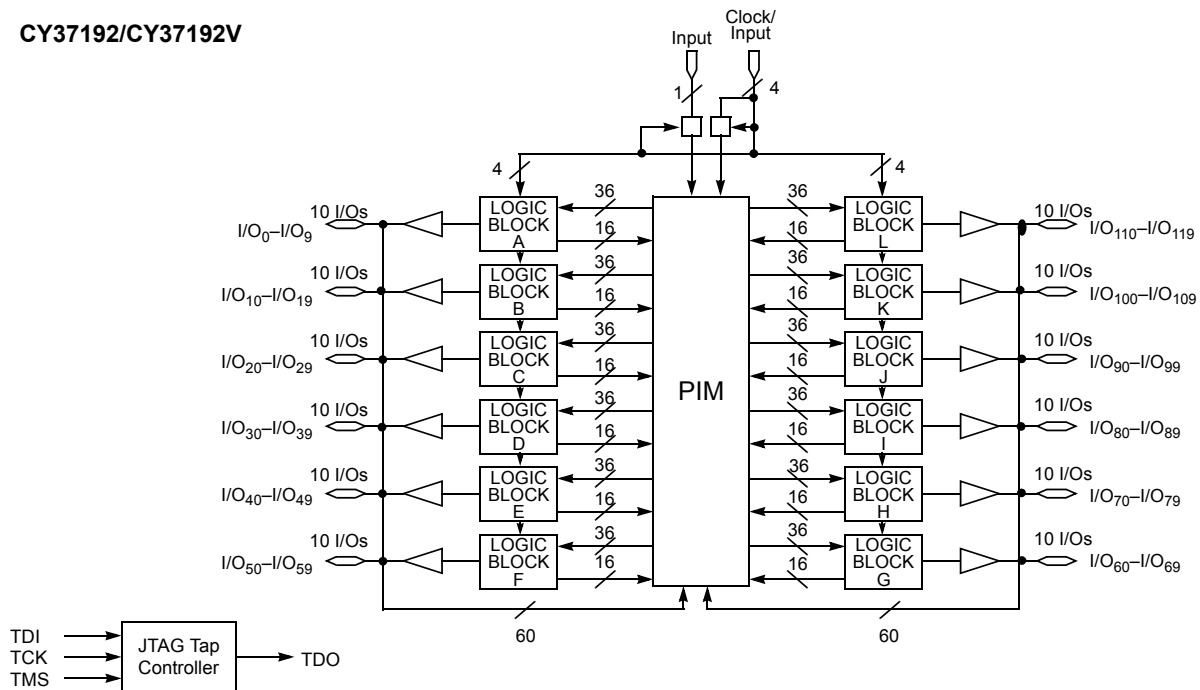
The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

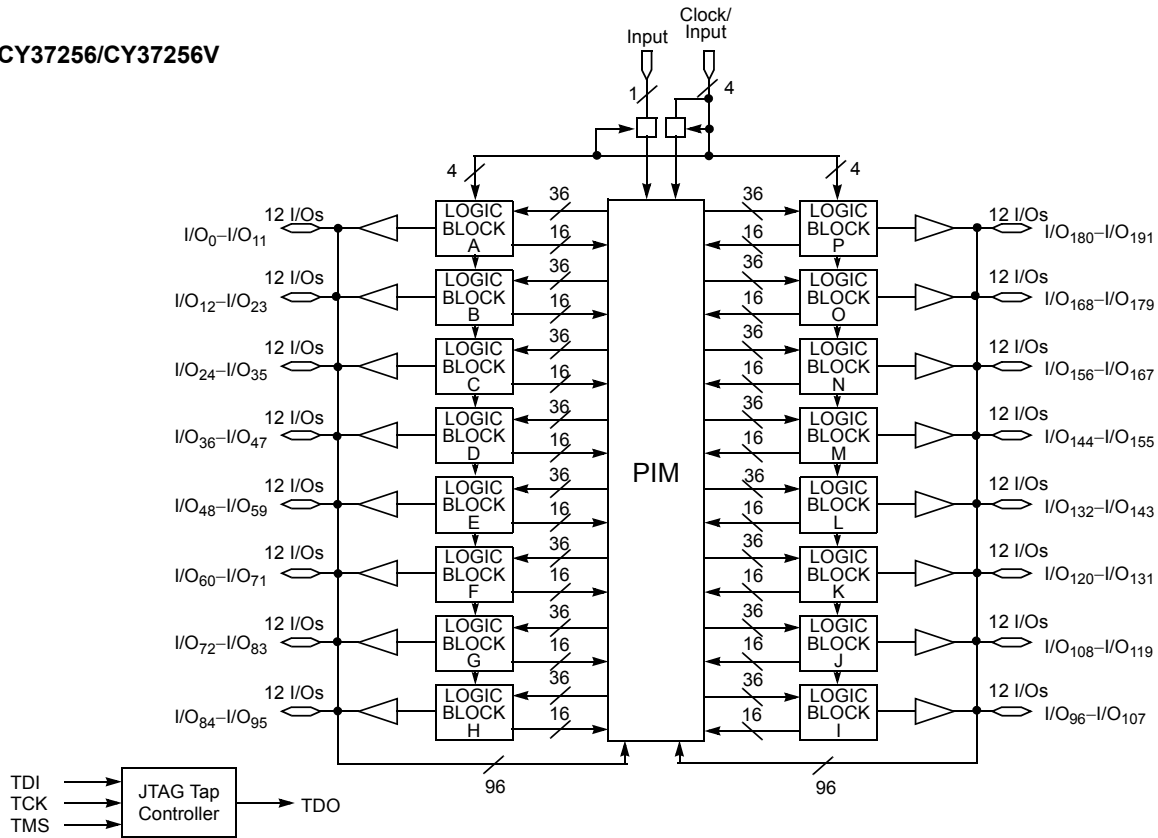
Third-Party Programmers

As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams (continued)
CY37128/CY37128V

CY37192/CY37192V


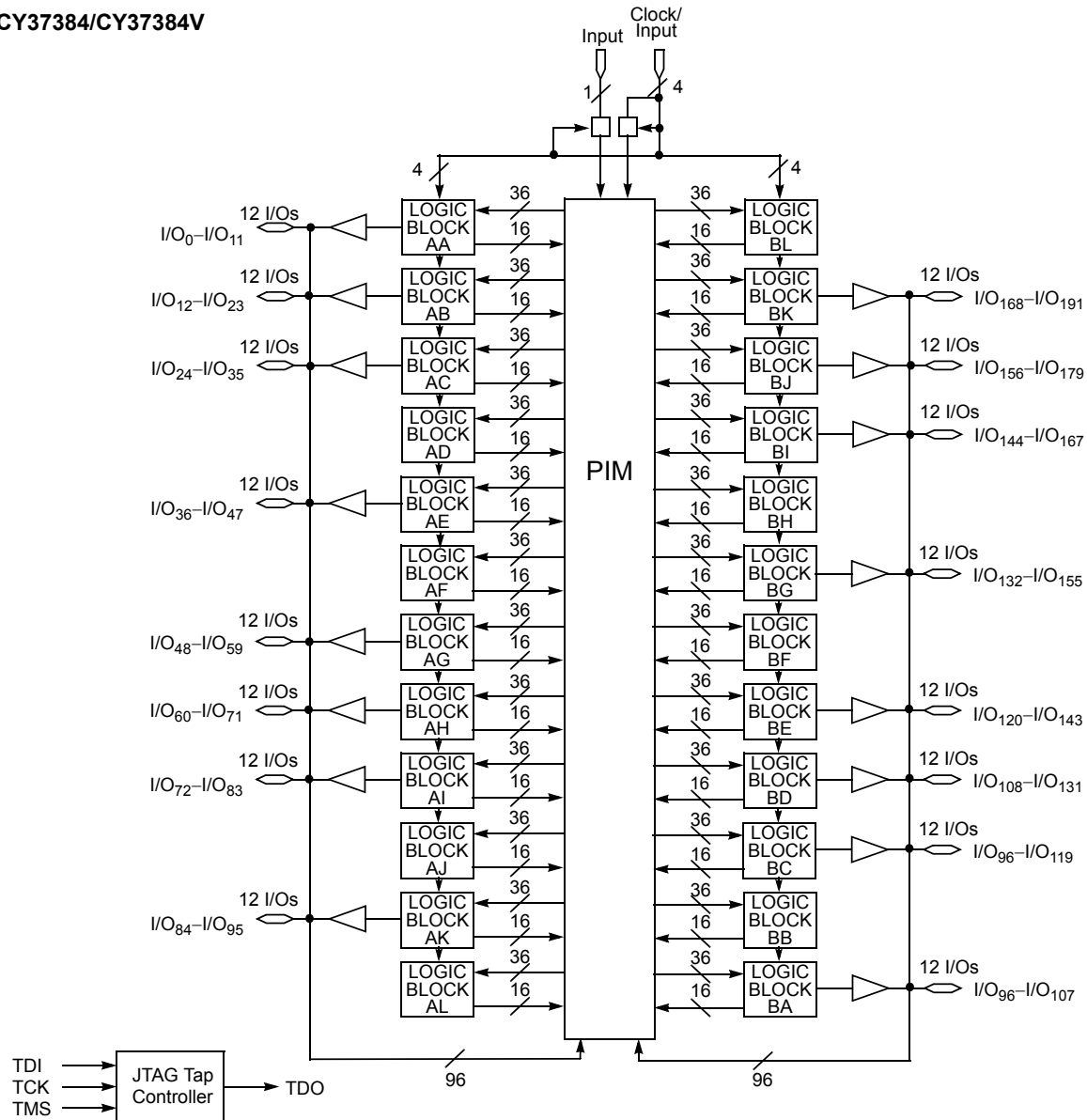
Logic Block Diagrams (continued)

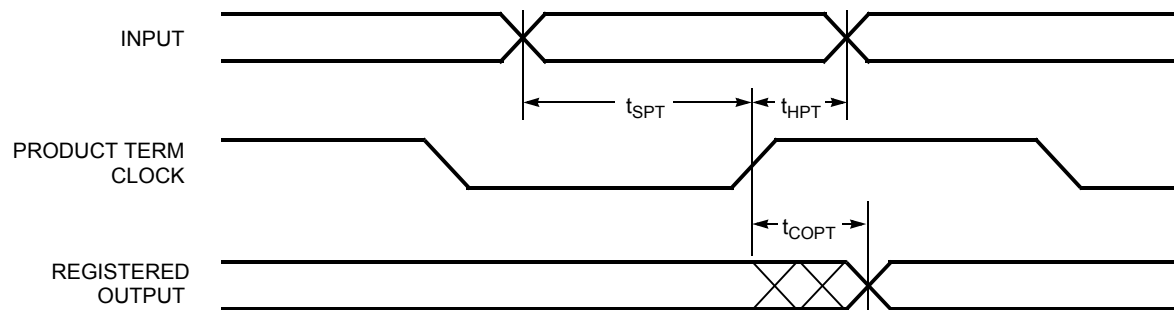
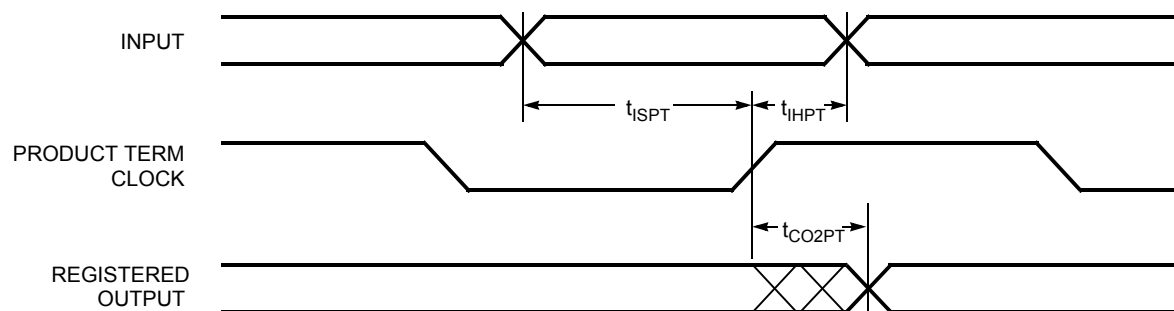
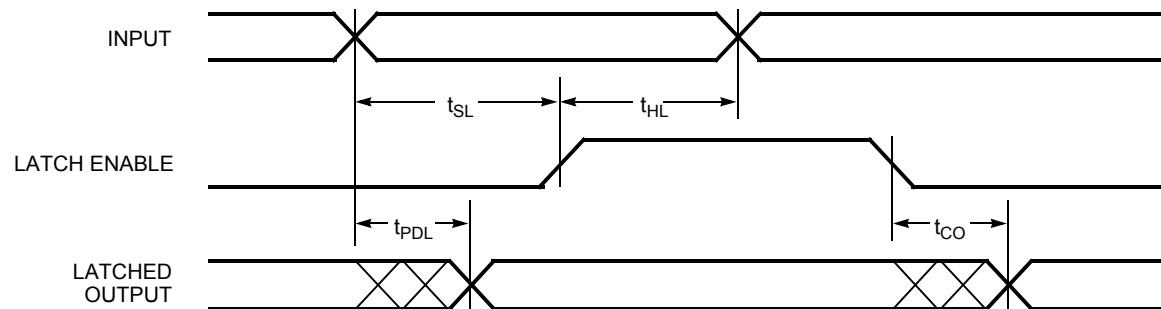
CY37256/CY37256V

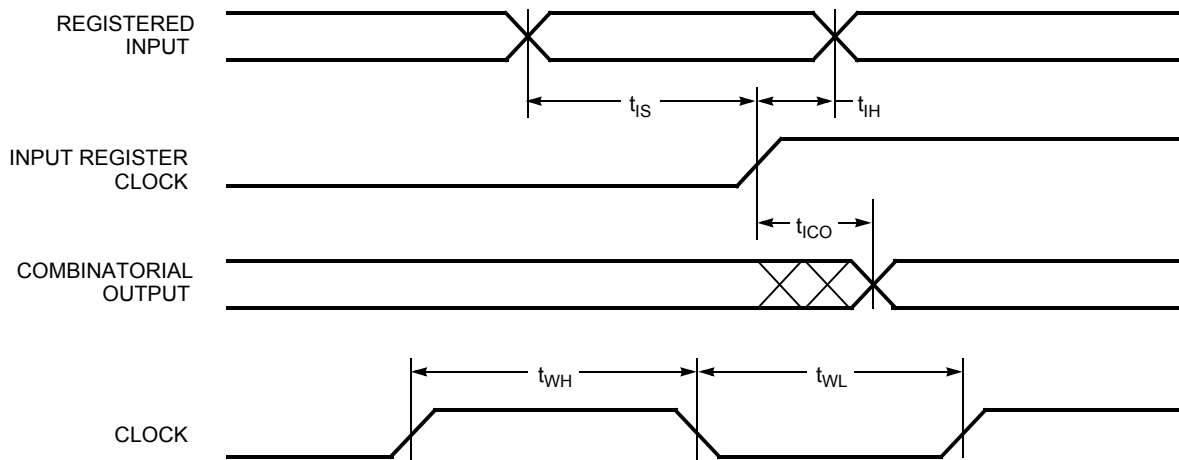
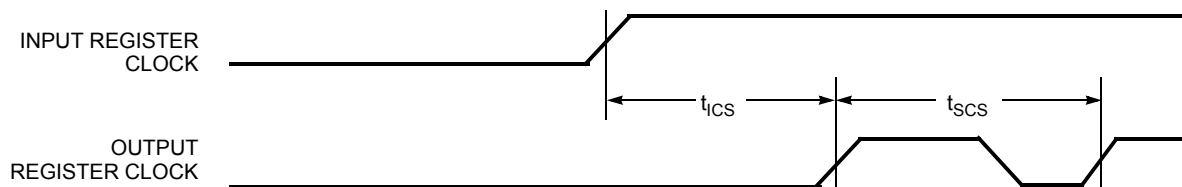
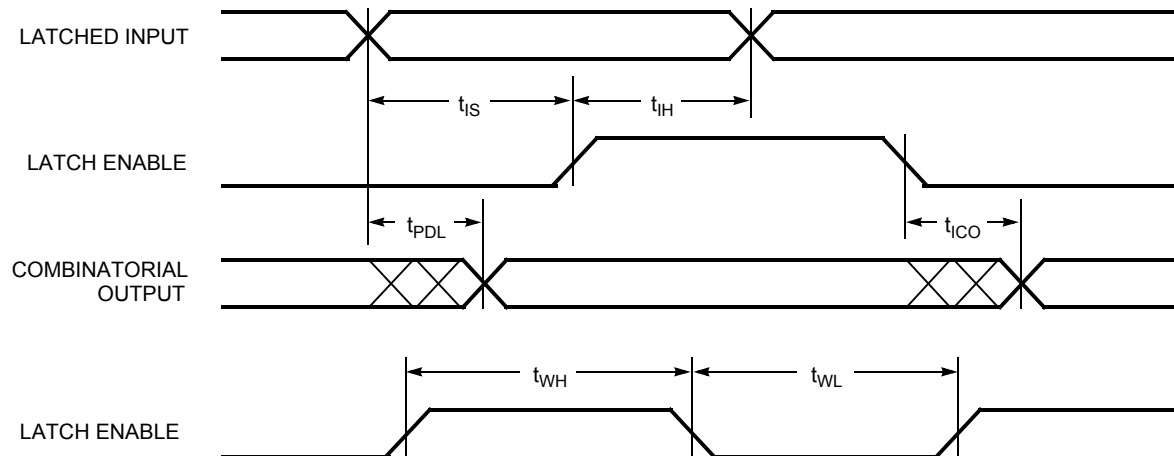


Logic Block Diagrams (continued)

CY37384/CY37384V

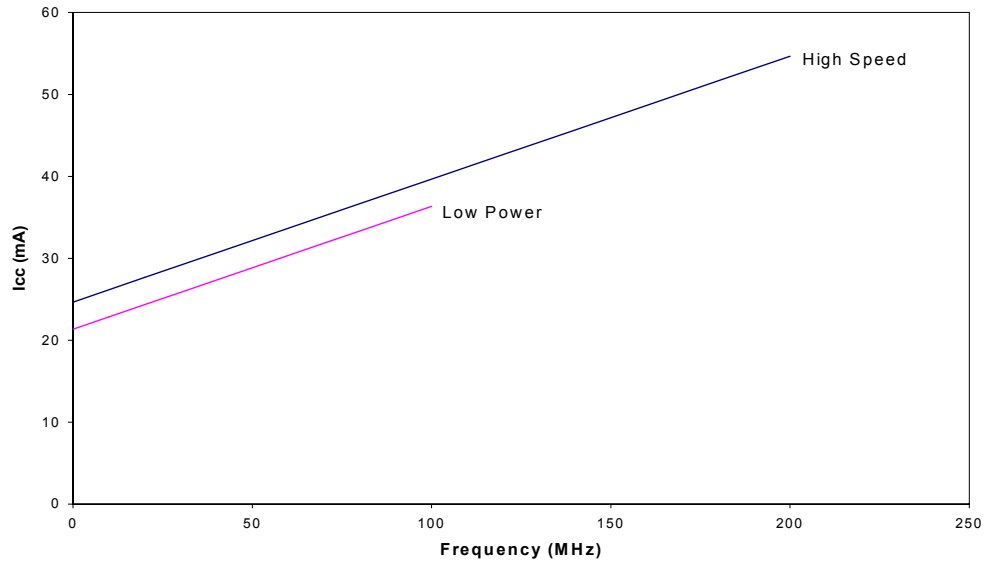


Switching Waveforms (continued)
Registered Output with Product Term Clocking Input Going Through the Array

Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register

Latched Output


Switching Waveforms (continued)
Registered Input

Clock to Clock

Latched Input


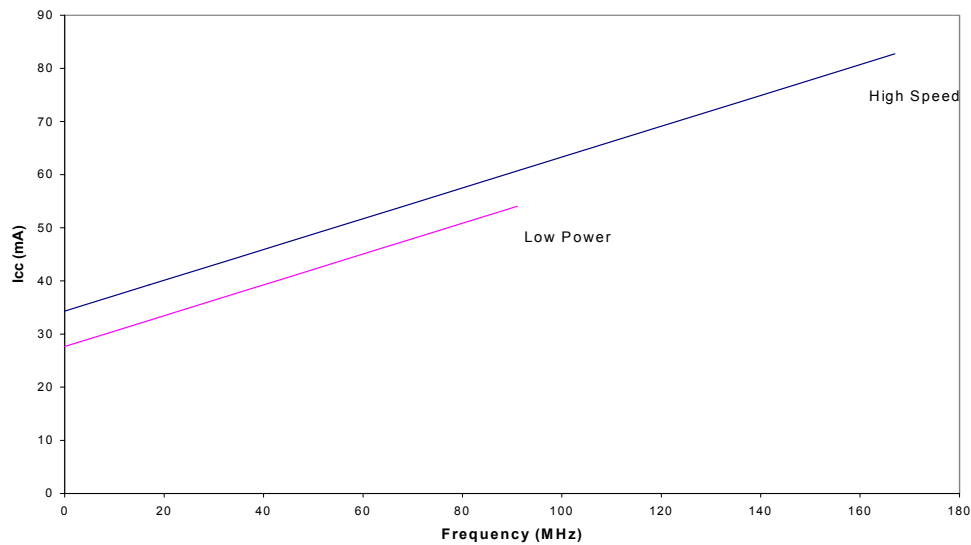
Power Consumption

Typical 5.0V Power Consumption CY37032

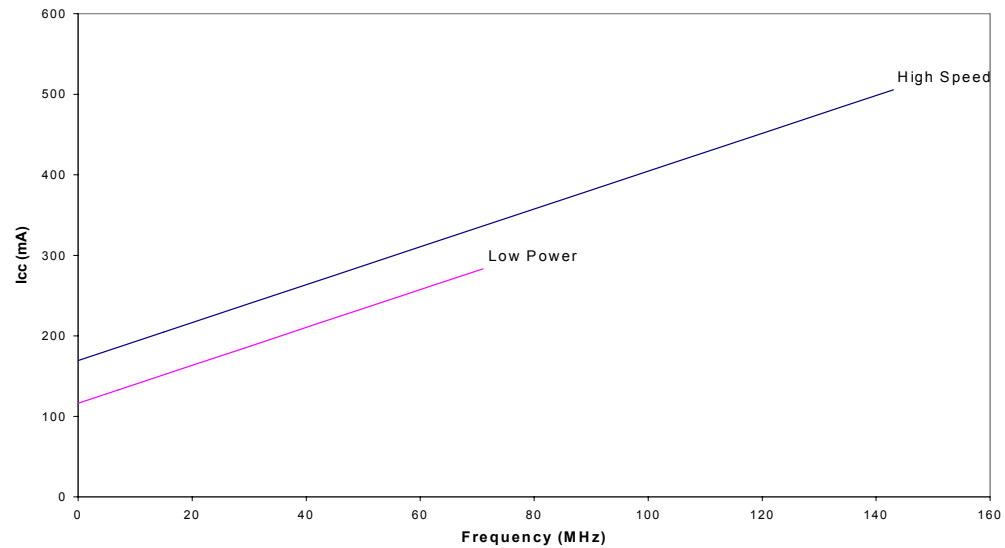


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

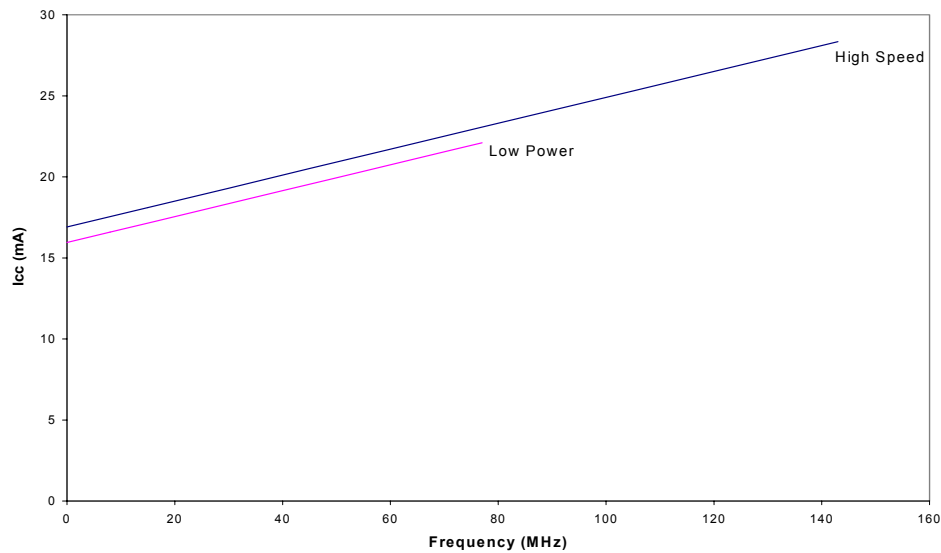
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 5.0V Power Consumption (continued)
CY37512


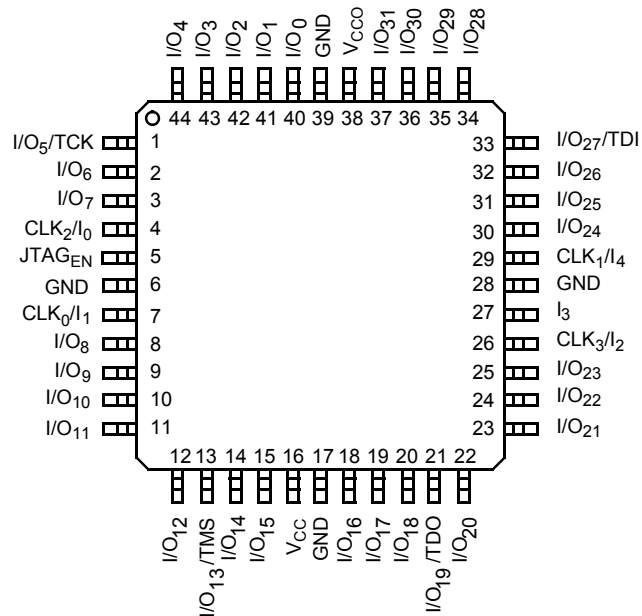
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 5.0V$, $T_A = \text{Room Temperature}$

Typical 3.3V Power Consumption
CY37032V


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
 $V_{CC} = 3.3V$, $T_A = \text{Room Temperature}$

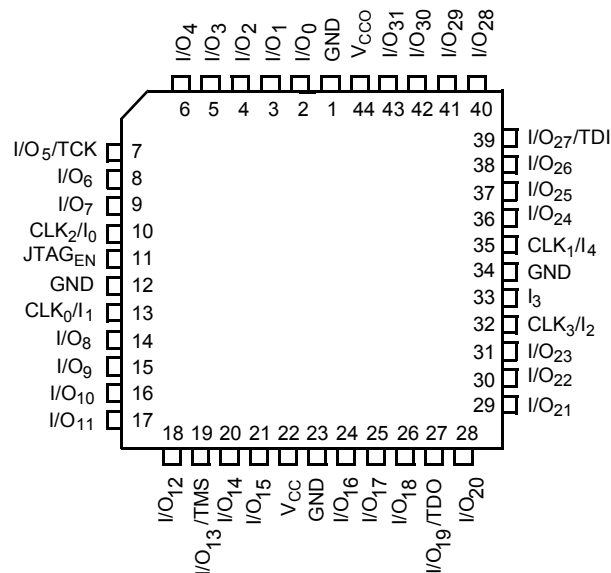
44-pin TQFP (A44)

Top View



44-pin PLCC (J67) / CLCC (Y67)

Top View

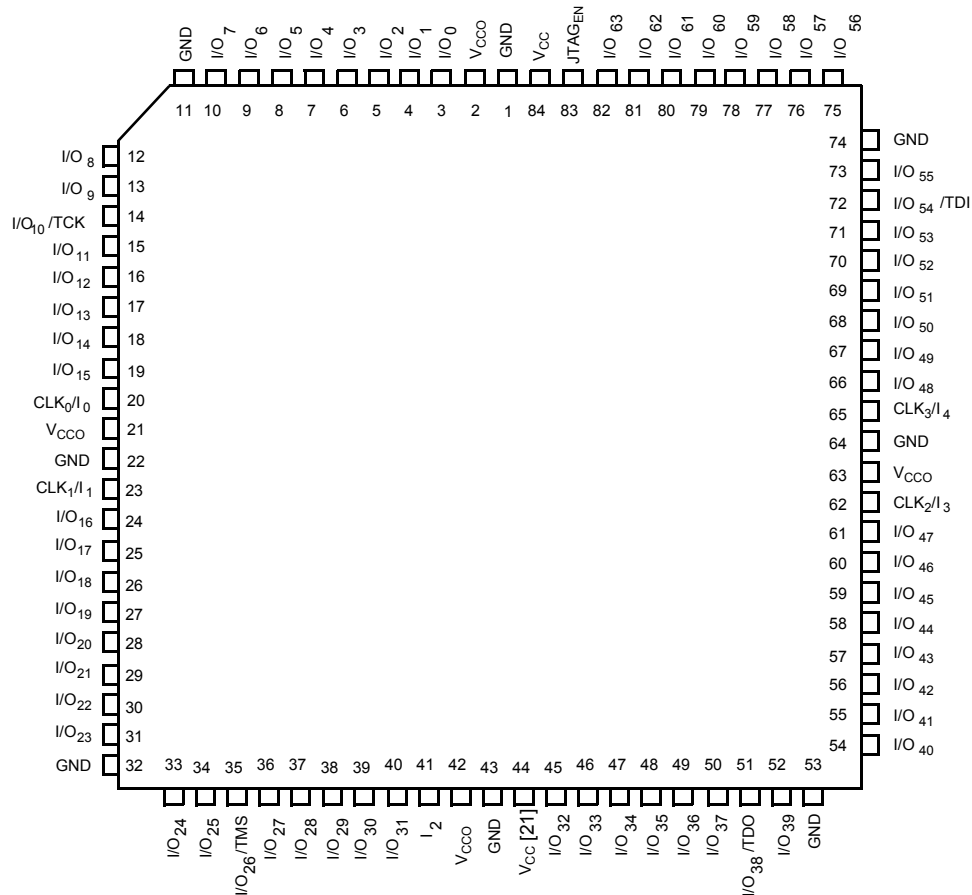


Pin Configurations^[20] (continued)
48-ball Fine-Pitch BGA (BA50)
Top View

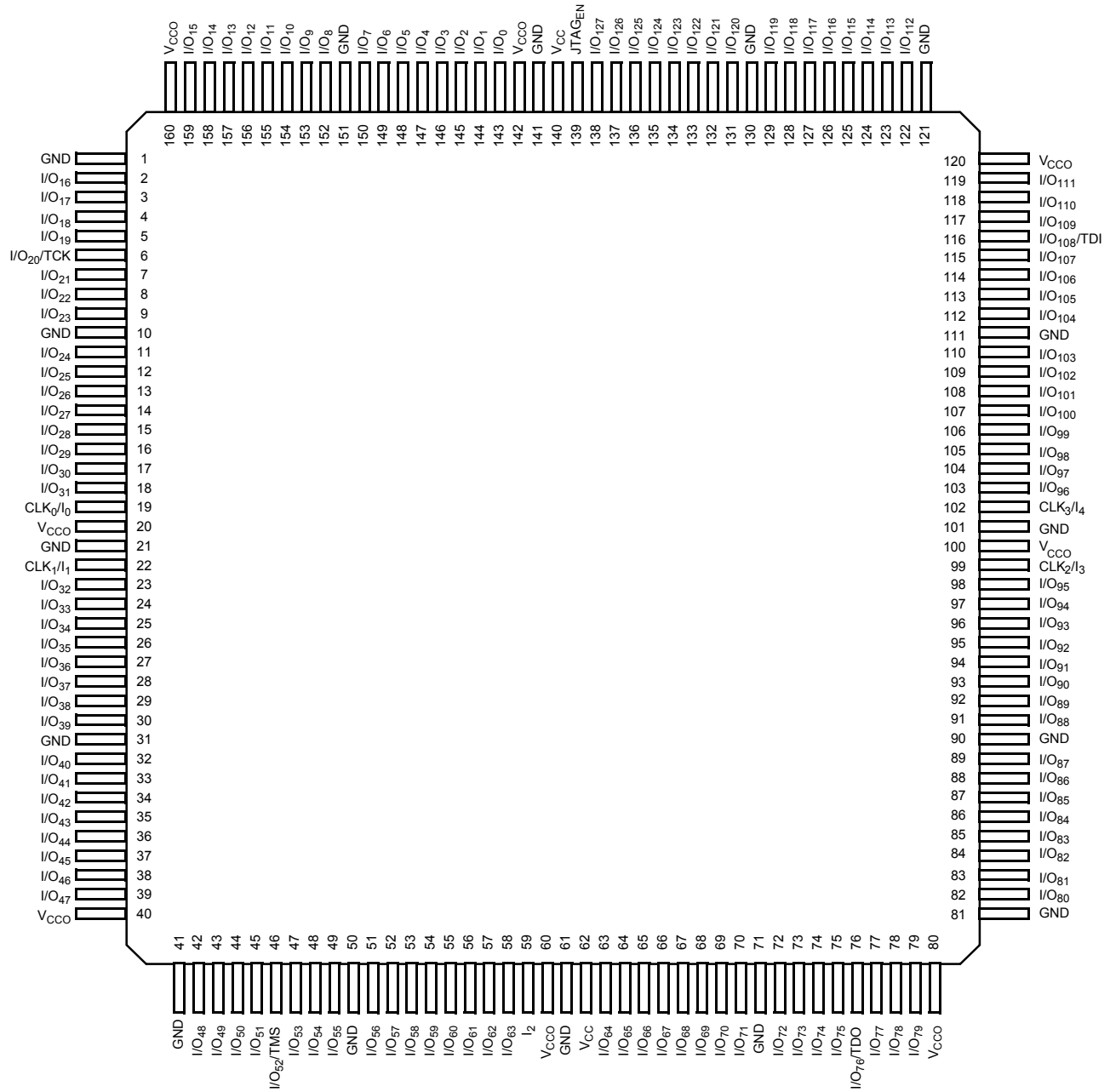
	1	2	3	4	5	6	7	8
A	I/O ₅ TCK	V _{CC}	I/O ₃	I/O ₁	I/O ₃₁	I/O ₃₀	V _{CC}	I/O ₂₇ TDI
B	V _{CC}	I/O ₄	I/O ₂	I/O ₀	I/O ₂₉	I/O ₂₈	I/O ₂₆	CLK ₁ /I ₄
C	CLK ₂ /I ₀	I/O ₇	I/O ₆	GND	GND	I/O ₂₅	I/O ₂₄	I ₃
D	JTAG _{EN}	I/O ₈	I/O ₉	GND	GND	I/O ₂₂	I/O ₂₃	CLK ₃ /I ₂
E	CLK ₀ /I ₁	I/O ₁₂	I/O ₁₁	I/O ₁₀	I/O ₁₆	I/O ₂₀	I/O ₂₁	V _{CC}
F	I/O ₁₃ TMS	V _{CC}	I/O ₁₄	I/O ₁₅	I/O ₁₇	I/O ₁₈	V _{CC}	I/O ₁₉ TDO

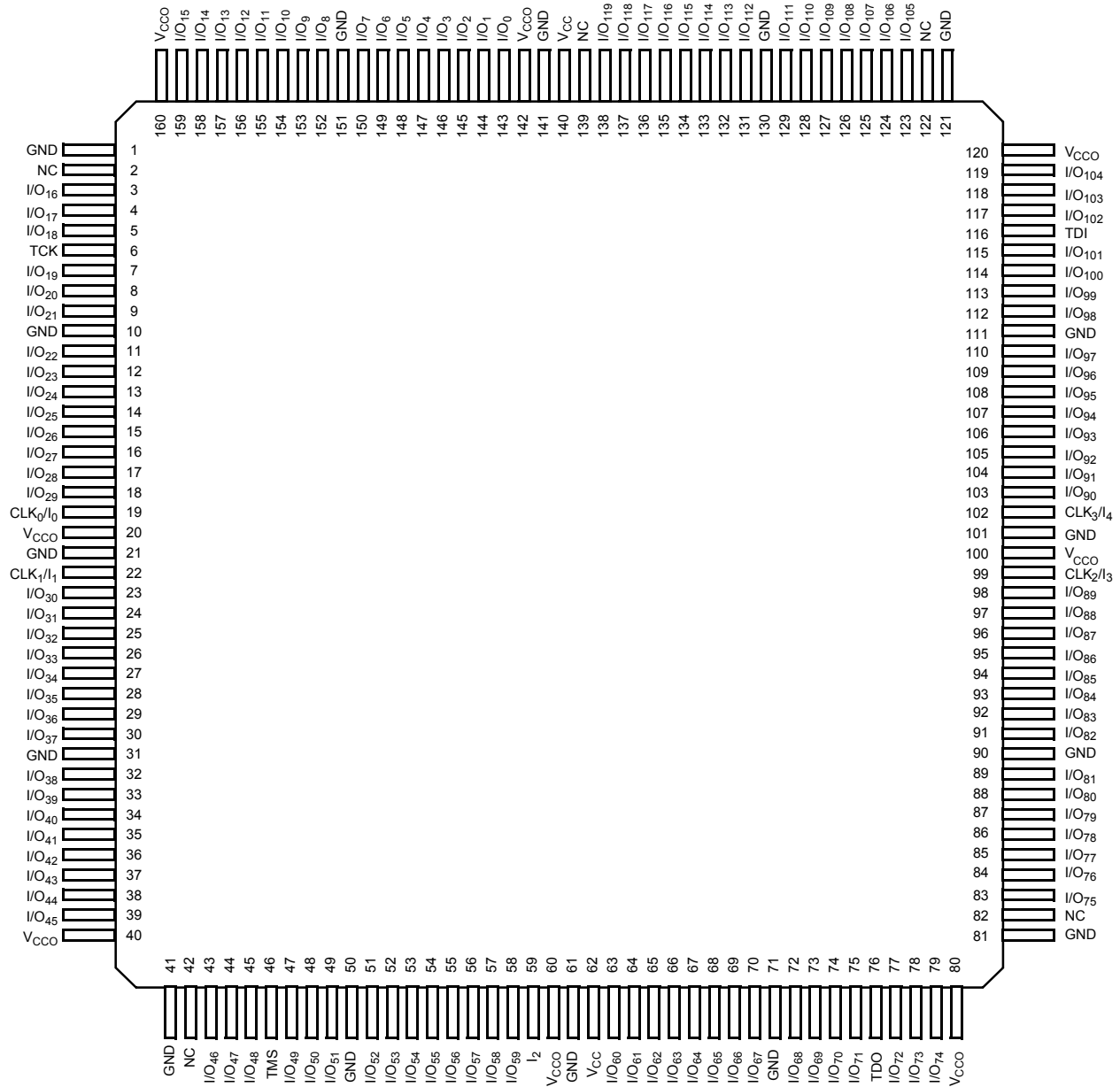
Note:

20. For 3.3V versions (Ultra37000V), V_{CCO} = V_{CC}.

84-lead PLCC (J83) / CLCC (Y84)
Top View

Note:

21. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations^[20] (continued)
**160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View**


Pin Configurations^[20] (continued)
**160-Lead TQFP (A160) for CY37192(V)
Top View**




Pin Configurations^[20] (continued)

400-Ball Fine-Pitch BGA (BB400)

Top View

A	GND	GND	NC	I/O ₁₇	I/O ₁₆	I/O ₁₄	I/O ₂₉	V _{CC}	I/O ₁₁	GND	GND	I/O ₂₅₇	V _{CC}	I/O ₂₃₉	I/O ₂₃₃	I/O ₂₃₂	I/O ₂₃₀	NC	GND	GND
B	GND	GND	GND	NC	I/O ₁₅	I/O ₁₃	I/O ₂₈	V _{CC}	I/O ₁₀	GND	GND	I/O ₂₅₆	V _{CC}	I/O ₂₃₈	I/O ₂₃₁	I/O ₂₂₉	NC	GND	GND	GND
C	NC	GND	GND	GND	I/O ₂₀	I/O ₁₂	I/O ₂₇	V _{CC}	I/O ₉	GND	GND	I/O ₂₅₅	V _{CC}	I/O ₂₃₇	I/O ₂₂₈	I/O ₂₄₅	GND	GND	GND	NC
D	I/O ₄₄	NC	GND	I/O ₂₁	I/O ₁₉	I/O ₁₈	I/O ₂₆	I/O ₂₅	I/O ₈	GND	GND	I/O ₂₅₄	I/O ₂₃₅	I/O ₂₃₆	I/O ₂₅₁	I/O ₂₄₄	I/O ₂₄₃	GND	NC	I/O ₂₂₇
E	I/O ₄₆	I/O ₄₃	I/O ₂₃	I/O ₂₂	NC	I/O ₃₅	I/O ₃₄	I/O ₂₄	I/O ₇	I/O ₄	I/O ₂₆₃	I/O ₂₅₃	I/O ₂₃₄	I/O ₂₅₀	I/O ₂₄₈	NC	I/O ₂₄₁	I/O ₂₄₂	I/O ₂₂₅	I/O ₂₂₆
F	I/O ₄₇	I/O ₄₅	I/O ₄₂	I/O ₄₁	I/O ₄₀	NC	I/O ₃₃	I/O ₃₂	I/O ₆	I/O ₃	I/O ₂₆₂	I/O ₂₅₂	I/O ₂₄₉	I/O ₂₄₇	I/O ₂₂₀	I/O ₂₂₁	I/O ₂₄₀	I/O ₂₂₂	I/O ₂₂₃	I/O ₂₂₄
G	I/O ₅₃	I/O ₅₂	I/O ₅₁	I/O ₅₀	I/O ₃₉	I/O ₃₈	I/O ₃₇	I/O ₃₁	I/O ₅	I/O ₂	I/O ₂₆₁	V _{CC}	I/O ₂₄₆	I/O ₂₁₇	I/O ₂₁₈	I/O ₂₁₉	I/O ₂₁₂	I/O ₂₁₃	I/O ₂₁₄	I/O ₂₁₅
H	V _{CC}	V _{CC}	V _{CC}	I/O ₄₉	I/O ₄₈	I/O ₃₆	TCK	V _{CC}	I/O ₃₀	I/O ₁	I/O ₂₅₉	I/O ₂₆₀	V _{CC}	TDI	I/O ₂₁₆	I/O ₂₁₀	I/O ₂₁₁	V _{CC}	V _{CC}	V _{CC}
J	I/O ₅₉	I/O ₅₈	I/O ₅₇	I/O ₅₆	I/O ₅₅	I/O ₅₄	V _{CC}	I/O ₆₂	I/O ₆₀	I/O ₀	I/O ₂₅₈	I/O ₂₀₂	I/O ₂₀₃	CLK ₃ /I ₄	I/O ₂₀₄	I/O ₂₀₅	I/O ₂₀₆	I/O ₂₀₇	I/O ₂₀₈	I/O ₂₀₉
K	GND	GND	GND	GND	I/O ₆₅	I/O ₆₄	CLK ₀ /I ₀	I/O ₆₃	I/O ₆₁	GND	GND	I/O ₁₉₈	I/O ₁₉₉	CLK ₂ /I ₃	I/O ₂₀₀	I/O ₂₀₁	GND	GND	GND	GND
L	GND	GND	GND	GND	I/O ₆₉	I/O ₆₈	NC	I/O ₆₇	I/O ₆₆	GND	GND	I/O ₁₉₃	I/O ₁₉₅	I ₂	I/O ₁₉₆	I/O ₁₉₇	GND	GND	GND	GND
M	I/O ₈₉	I/O ₈₈	I/O ₈₇	I/O ₈₆	I/O ₈₅	I/O ₈₄	CLK ₁ /I ₁	I/O ₇₁	I/O ₇₀	I/O ₁₂₆	I/O ₁₃₂	I/O ₁₉₂	I/O ₁₉₄	V _{CC}	I/O ₁₇₄	I/O ₁₇₅	I/O ₁₇₆	I/O ₁₇₇	I/O ₁₇₈	I/O ₁₇₉
N	V _{CC}	V _{CC}	V _{CC}	I/O ₉₁	I/O ₉₀	I/O ₇₂	TMS	V _{CC}	I/O ₁₂₈	I/O ₁₂₇	I/O ₁₃₃	I/O ₁₆₂	V _{CC}	TDO	I/O ₁₈₀	I/O ₁₆₈	I/O ₁₆₉	V _{CC}	V _{CC}	V _{CC}
P	I/O ₉₅	I/O ₉₄	I/O ₉₃	I/O ₉₂	I/O ₇₅	I/O ₇₄	I/O ₇₃	I/O ₁₁₄	V _{CC}	I/O ₁₂₉	I/O ₁₃₄	I/O ₁₃₇	I/O ₁₆₃	I/O ₁₈₁	I/O ₁₈₂	I/O ₁₈₃	I/O ₁₇₀	I/O ₁₇₁	I/O ₁₇₂	I/O ₁₇₃
R	I/O ₉₀	I/O ₇₉	I/O ₇₈	I/O ₁₀₈	I/O ₇₇	I/O ₇₆	I/O ₁₁₅	I/O ₁₁₇	I/O ₁₂₀	I/O ₁₃₀	I/O ₁₃₅	I/O ₁₃₈	I/O ₁₆₄	I/O ₁₆₅	NC	I/O ₁₈₄	I/O ₁₈₅	I/O ₁₈₆	I/O ₁₈₉	I/O ₁₉₁
T	I/O ₈₂	I/O ₈₁	I/O ₁₁₀	I/O ₁₀₉	NC	I/O ₁₁₆	I/O ₁₁₈	I/O ₁₀₂	I/O ₁₂₁	I/O ₁₃₁	I/O ₁₃₆	I/O ₁₃₉	I/O ₁₅₆	I/O ₁₆₆	I/O ₁₆₇	NC	I/O ₁₅₄	I/O ₁₅₅	I/O ₁₈₇	I/O ₁₉₀
U	I/O ₈₃	NC	GND	I/O ₁₁₁	I/O ₁₁₂	I/O ₁₁₉	I/O ₁₀₄	I/O ₁₀₃	I/O ₁₂₂	GND	GND	I/O ₁₄₀	I/O ₁₅₇	I/O ₁₅₈	I/O ₁₅₀	I/O ₁₅₁	I/O ₁₅₃	GND	NC	I/O ₁₈₈
V	NC	GND	GND	GND	I/O ₁₁₃	I/O ₉₆	I/O ₁₀₅	V _{CC}	I/O ₁₂₃	GND	GND	I/O ₁₄₁	V _{CC}	I/O ₁₅₉	I/O ₁₄ 4	I/O ₁₅₂	GND	GND	GND	NC
W	GND	GND	GND	NC	I/O ₉₇	I/O ₉₉	I/O ₁₀₆	V _{CC}	I/O ₁₂₄	GND	GND	I/O ₁₄₂	V _{CC}	I/O ₁₆₀	I/O ₁₄₅	I/O ₁₄₇	NC	GND	GND	GND
Y	GND	GND	NC	I/O ₉₈	I/O ₁₀₀	I/O ₁₀₁	I/O ₁₀₇	V _{CC}	I/O ₁₂₅	GND	GND	I/O ₁₄₃	V _{CC}	I/O ₁₆₁	I/O ₁₄₆	I/O ₁₄₈	I/O ₁₄₉	NC	GND	GND

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	154	CY37256P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-154AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-154NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-154BGC	BG292	292-Ball Plastic Ball Grid Array	
	125	CY37256P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952302QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
	83	CY37256P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952301QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	125	CY37384P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
	83	CY37384P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	

5.0V Ordering Information (continued)

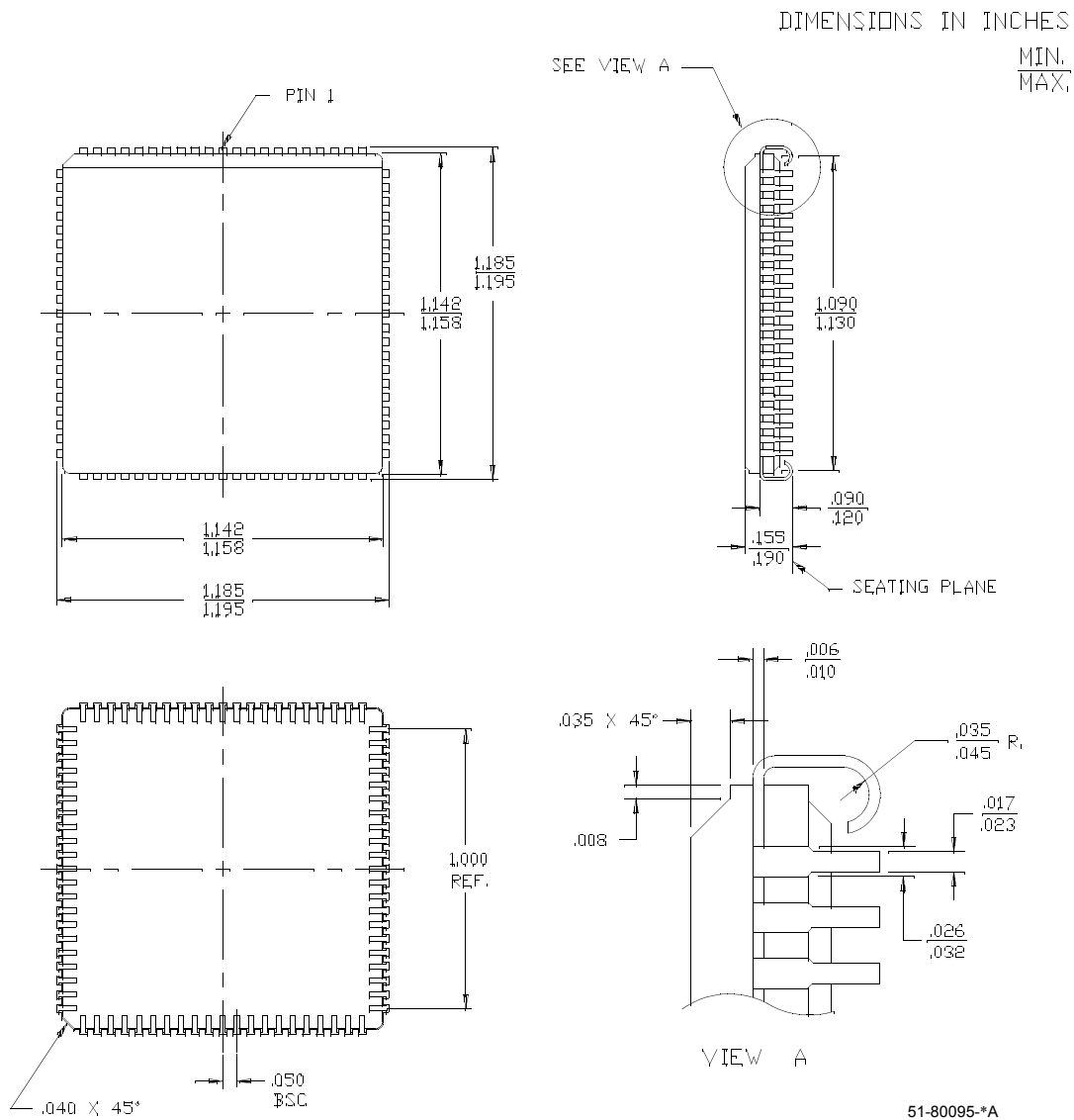
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-125BGC	BG388	388-Ball Plastic Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

3.3V Ordering Information

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-143BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAI	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP44-100JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	

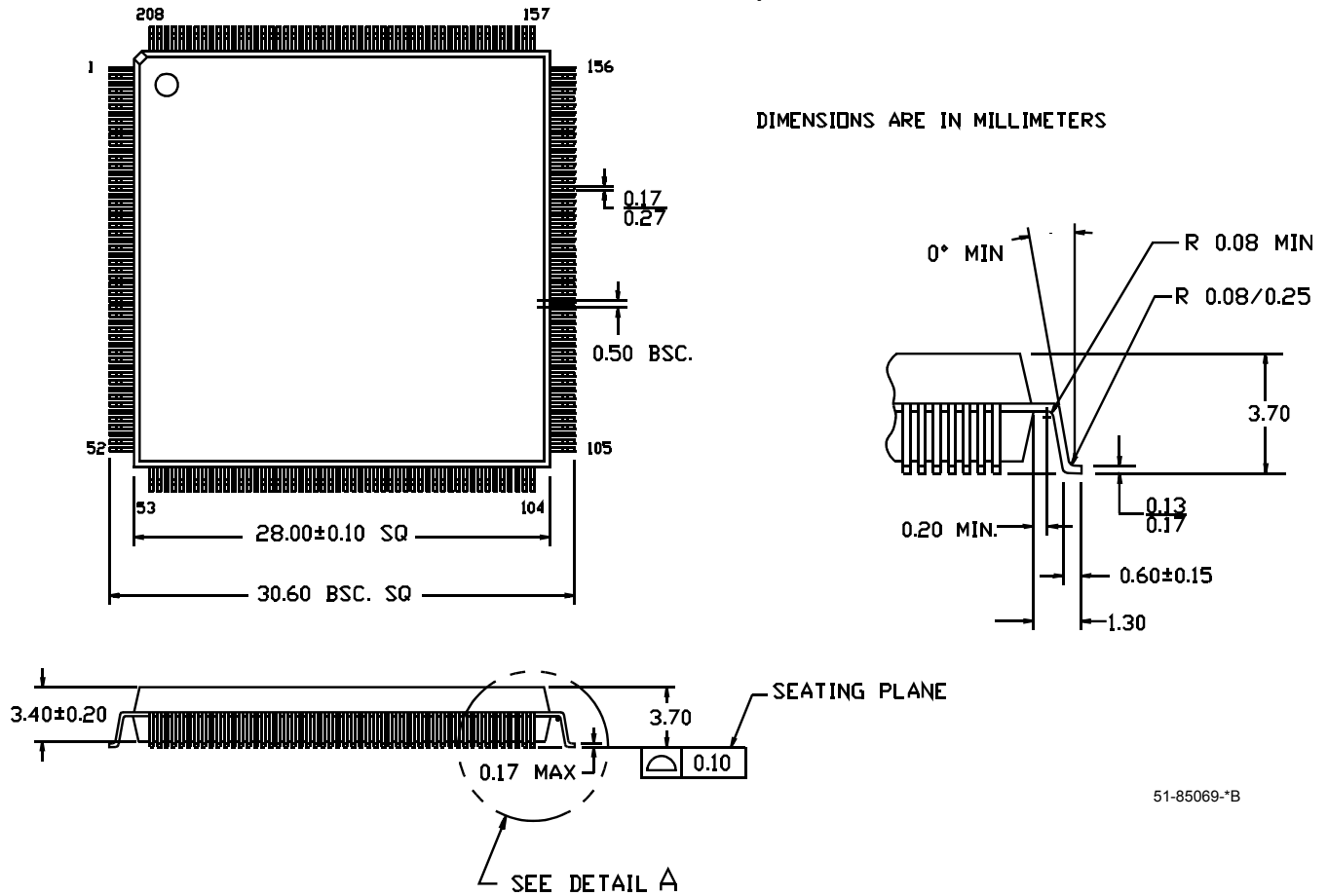
Package Diagrams (continued)

84-Lead Ceramic Leaded Chip Carrier Y84

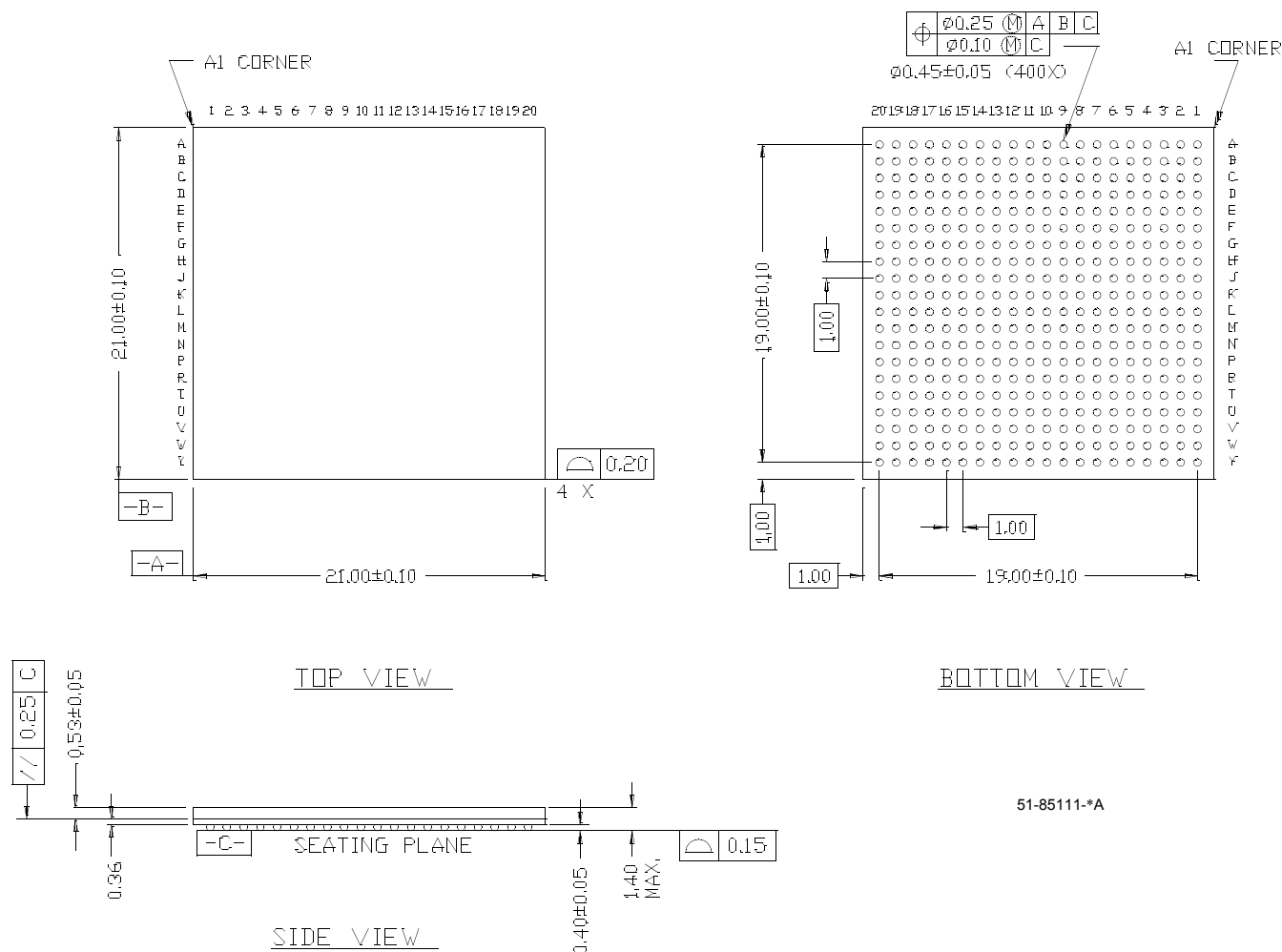


Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



51-85069-*B

Package Diagrams (continued)
400-Ball FBGA (21 x 21 x 1.4 mm) BB400


ViewDraw and SpeedWave are trademarks of ViewLogic. Windows is a registered trademark of Microsoft Corporation. *Warp* is a registered trademark, and In-System Reprogrammable, ISR, *Warp* Professional, *Warp* Enterprise, and Ultra37000 are trademarks, of Cypress Semiconductor Corporation. All product and company names mentioned in this document are the trademarks of their respective holders.