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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	133
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37256p160-125axi

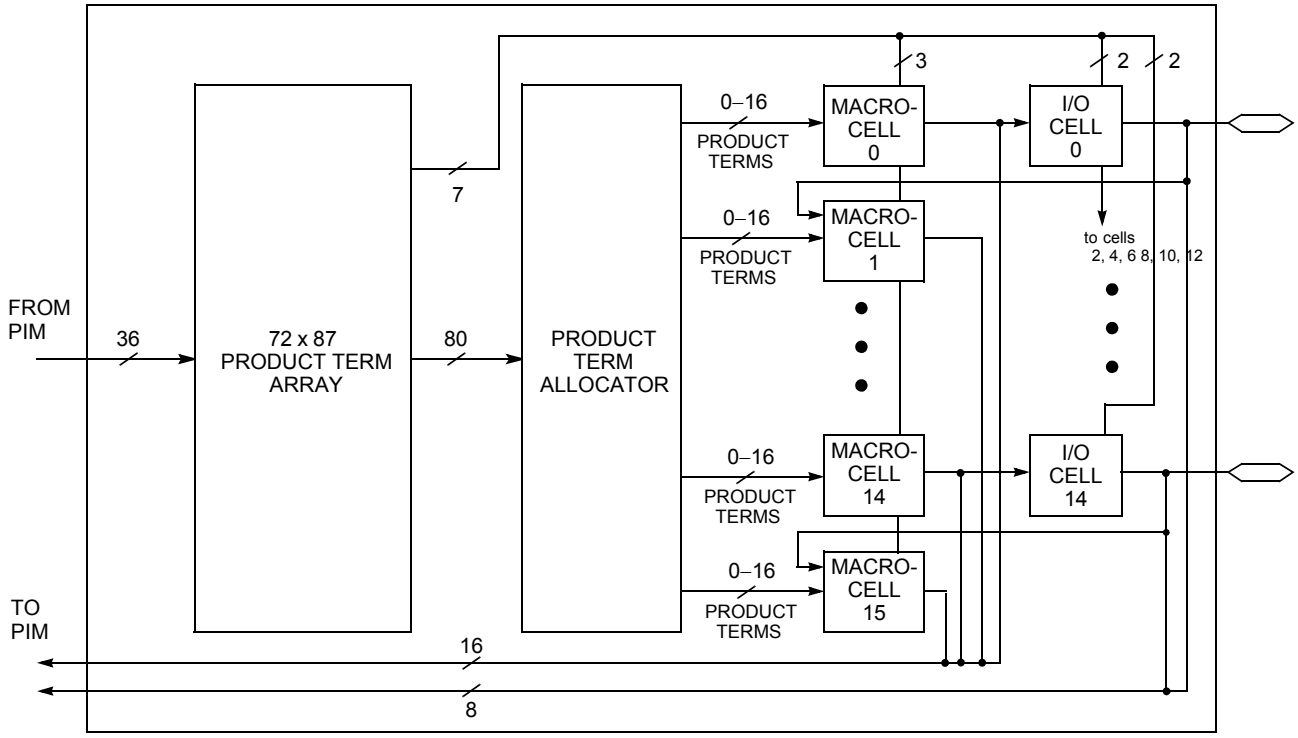


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

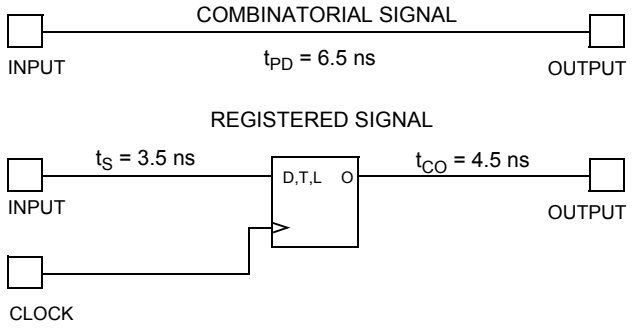


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

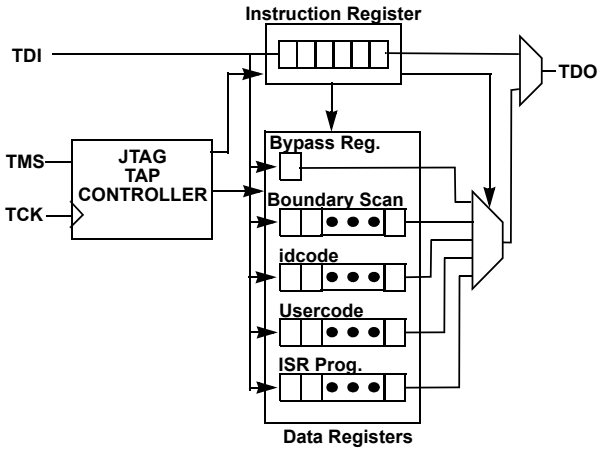


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC*, Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

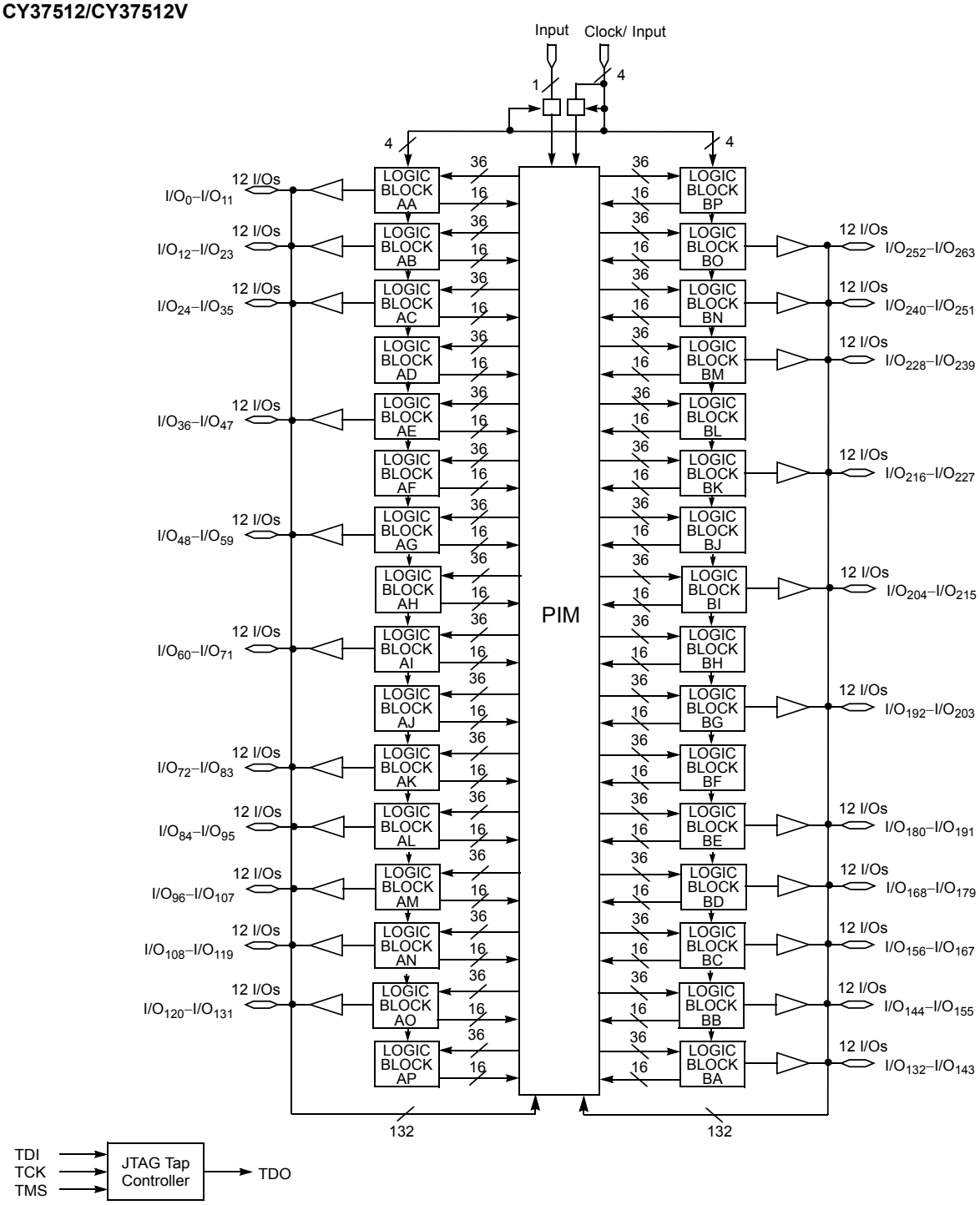
Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

Logic Block Diagrams (continued)

CY37512/CY37512V



Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual-Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

3.3V Device Characteristics Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 3.0 to 3.6V

Current into Outputs ..... 8 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}[10]
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Notes:
9. Dual pins are I/O with JTAG pins.
10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V± 0.16V.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

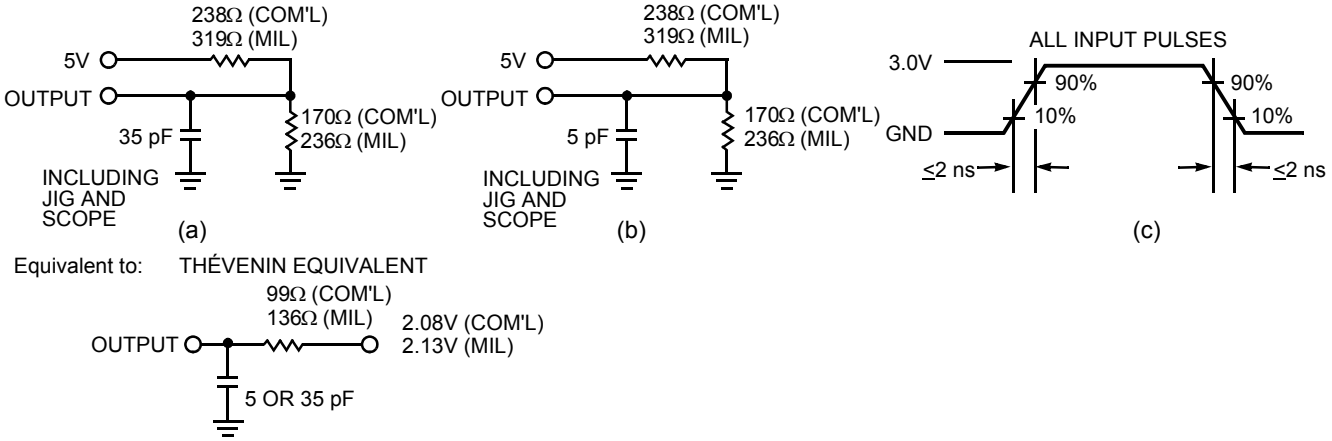
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

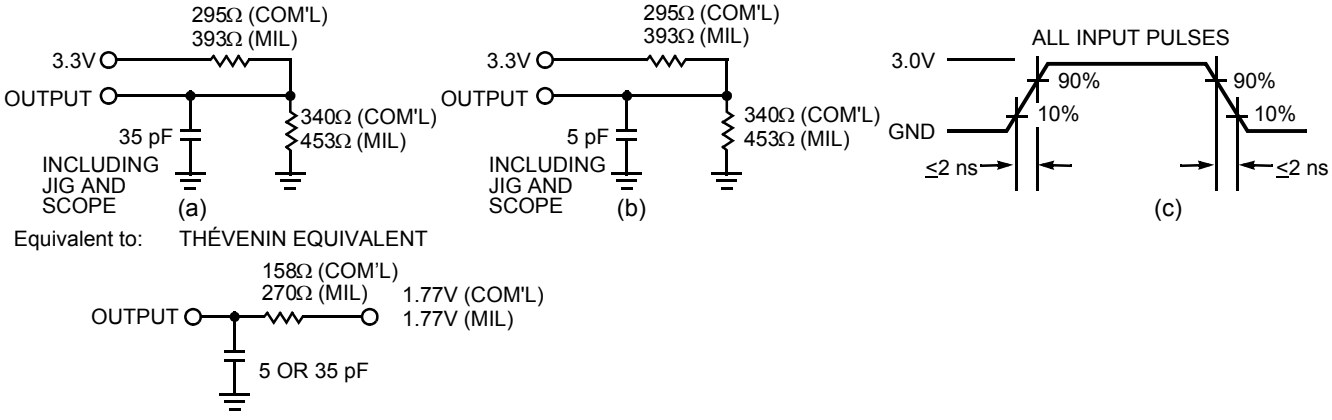
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Characteristics

5.0V AC Test Loads and Waveforms



3.3V AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range [12]

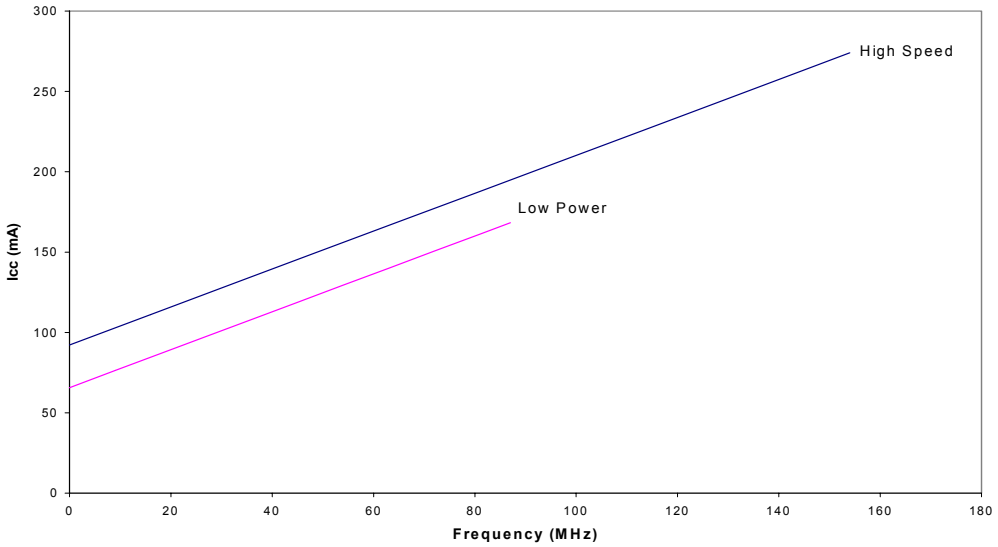
Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t_{PD}[13, 14, 15]		6		6.5		7.5		8.5		10		12		15		20	ns
t_{PDL}[13, 14, 15]		11		12.5		14.5		16		16.5		17		19		22	ns
t_{PDLL}[13, 14, 15]		12		13.5		15.5		17		17.5		18		20		24	ns
t_{EA}[13, 14, 15]		8		8.5		11		13		14		16		19		24	ns
t_{ER}[11, 13]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t_{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{IS}	2		2		2		2		2		2.5		3		4		ns
t_{IH}	2		2		2		2		2		2.5		3		4		ns
t_{ICO}[13, 14, 15]		11		11		11		12.5		12.5		16		19		24	ns
t_{ICOL}[13, 14, 15]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t_{CO}[14, 15]		4		4		4.5		6		6.5[16]		6.5[17]		8[18]		10	ns
t_{S}[13]	4		4		5		5		5.5[16]		6[17]		8[18]		10		ns
t_{H}	0		0		0		0		0		0		0		0		ns
t_{CO2}[13, 14, 15]		9.5		10		11		12		14		16		19		24	ns
t_{SCS}[13]	5		6		6.5		7		8[16]		10		12		15		ns
t_{SL}[13]	7.5		7.5		8.5		9		10		12		15		15		ns
t_{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t_{COPT}[13, 14, 15]		7		10		10		13		13		13		15		20	ns
t_{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{ISPT}[13]	0		0		0		0		0		0		0		0		ns
t_{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t_{CO2PT}[13, 14, 15]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t_{ICS}[13]	5		6		6		7		8[16]		10		12		15		ns
Operating Frequency Parameters																	
f_{MAX1}	200		167		154		143		125[16]		100		83		66		MHz
f_{MAX2}	200		200		200		167		154		153[17]		125[18]		100		MHz
f_{MAX3}	125		125		105		91		83		80[17]		62.5		50		MHz
f_{MAX4}	167		167		154		125		118		100		83		66		MHz
Reset/Preset Parameters																	
t_{RW}	8		8		8		8		10		12		15		20		ns
t_{RR}[13]	10		10		10		10		12		14		17		22		ns

Notes:

16. The following values correspond to the CY37512 and CY37384 devices: t_{CO} = 5 ns, t_S = 6.5 ns, t_{SCS} = 8.5 ns, t_{ICS} = 8.5 ns, f_{MAX1} = 118 MHz.
17. The following values correspond to the CY37192V and CY37256V devices: t_{CO} = 6 ns, t_S = 7 ns, f_{MAX2} = 143 MHz, f_{MAX3} = 77 MHz, and f_{MAX4} = 100 MHz; and for the CY37512 devices: t_S = 7 ns.
18. The following values correspond to the CY37512V and CY37384V devices: t_{CO} = 6.5 ns, t_S = 9.5 ns, and f_{MAX2} = 105 MHz.

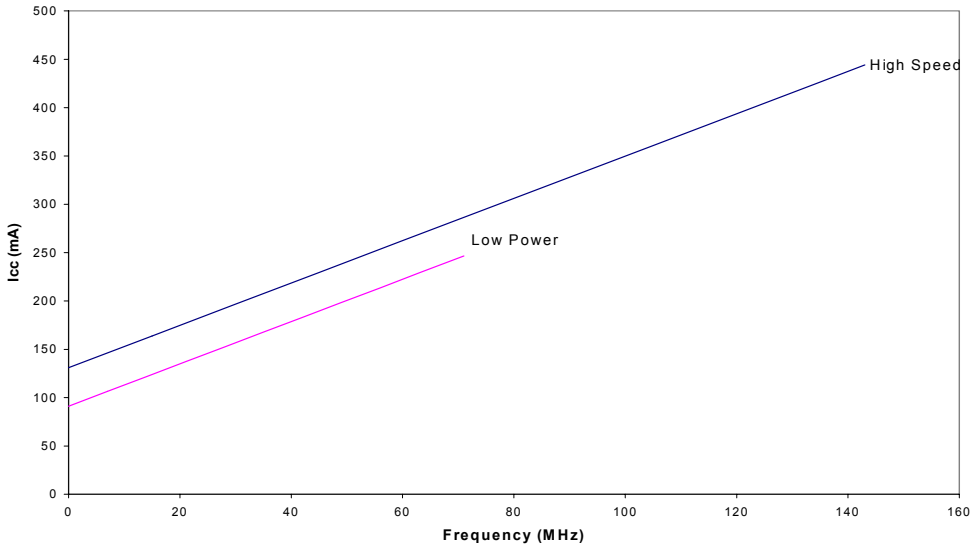
Typical 5.0V Power Consumption (continued)

CY37256



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

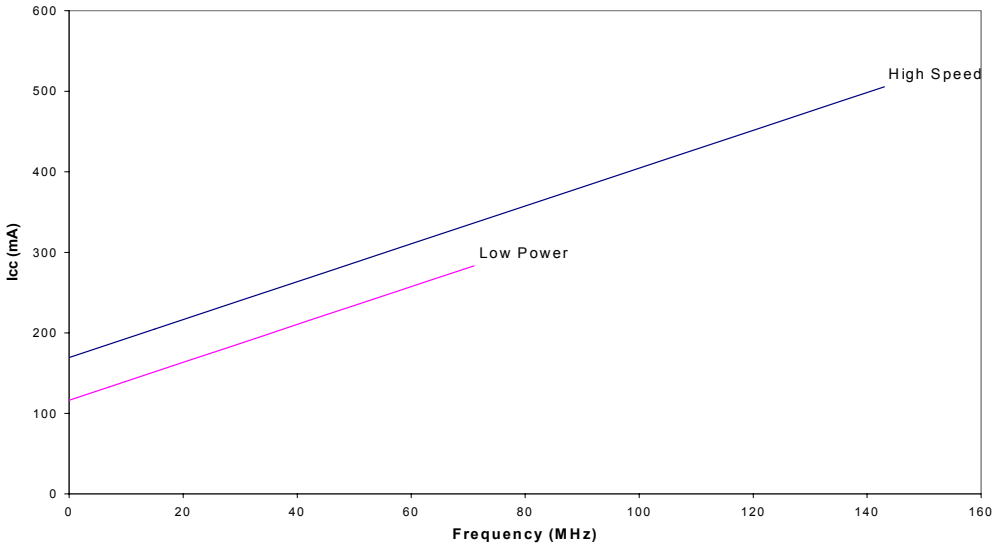
CY37384



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 5.0V Power Consumption (continued)

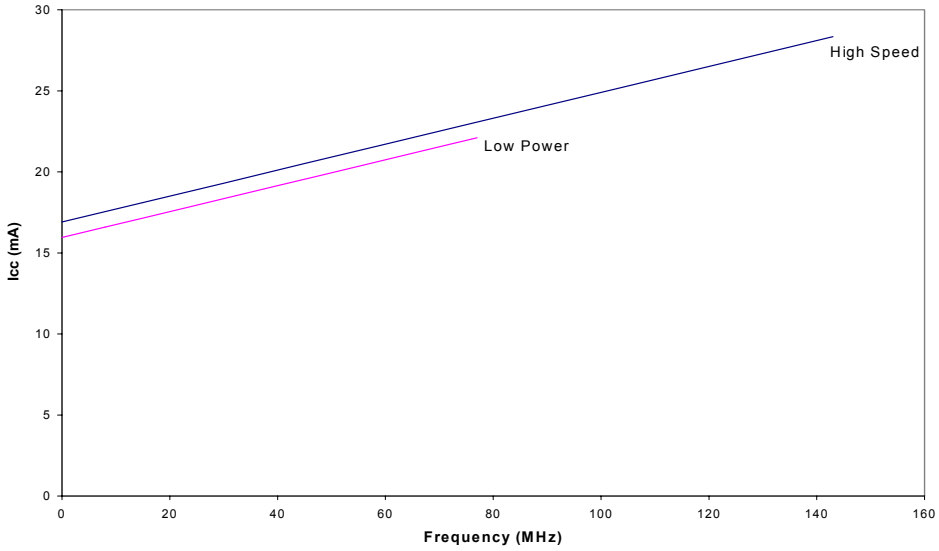
CY37512



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 3.3V Power Consumption

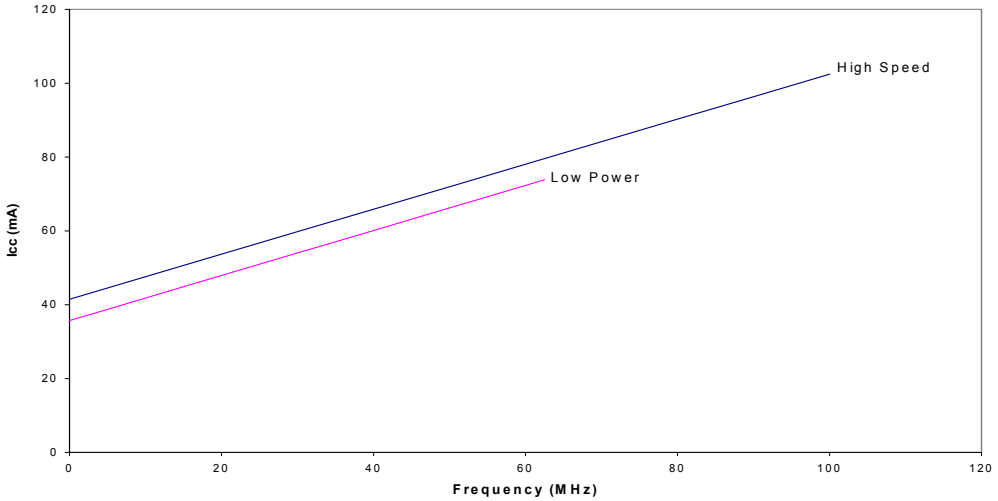
CY37032V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

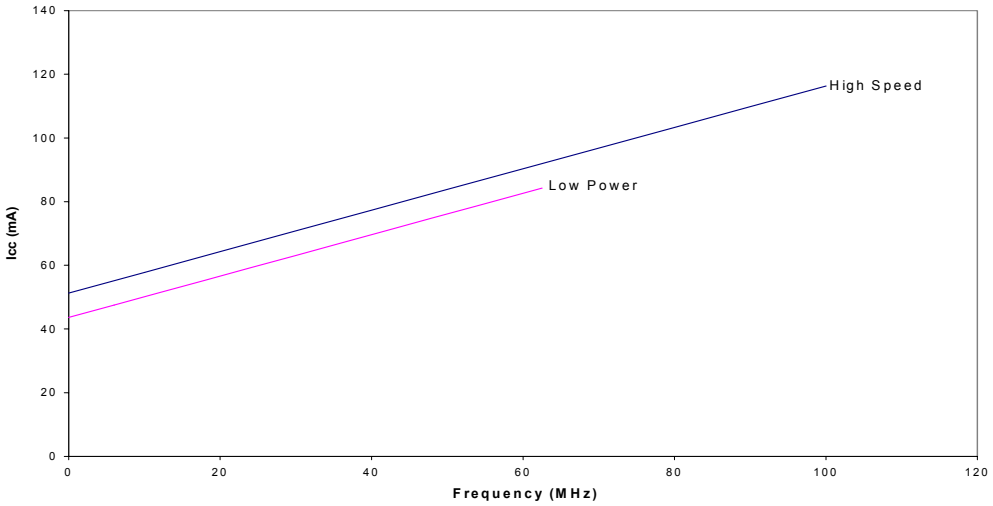
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

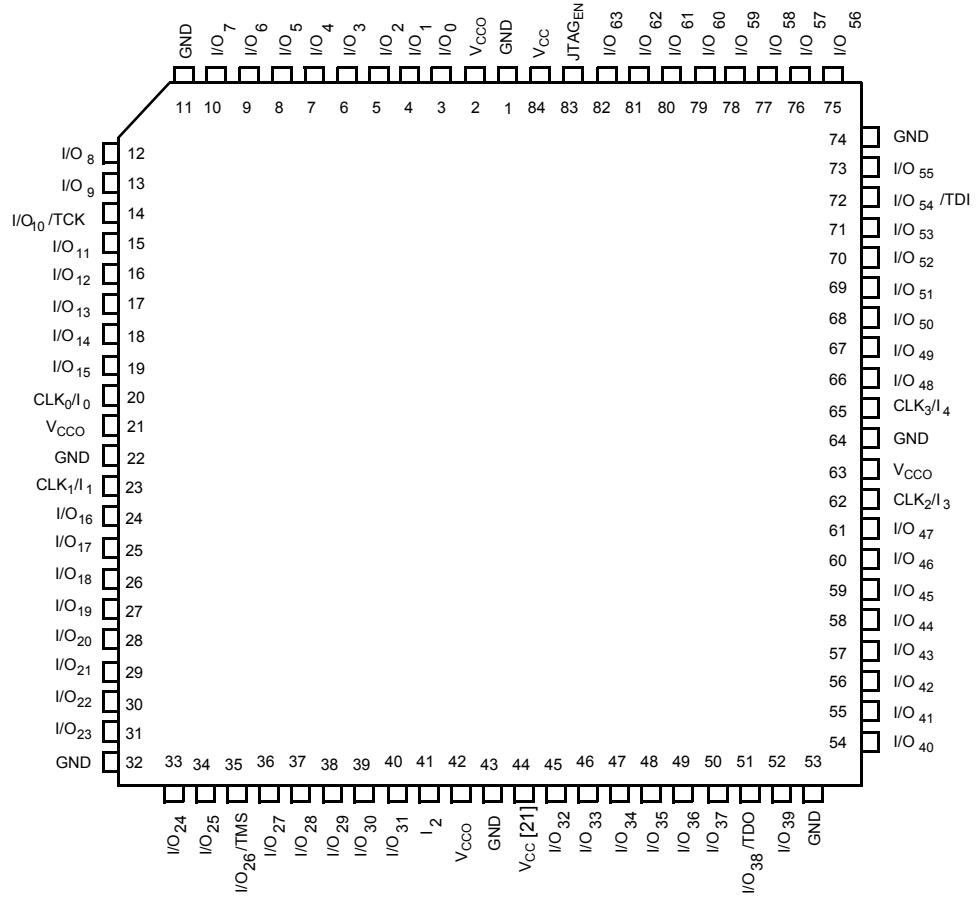
Pin Configurations[20] (continued)

48-ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O_5 TCK	V_{CC}	I/O_3	I/O_1	I/O_{31}	I/O_{30}	V_{CC}	I/O_{27} TDI
B	V_{CC}	I/O_4	I/O_2	I/O_0	I/O_{29}	I/O_{28}	I/O_{26}	CLK_1/ I_4
C	CLK_2/ I_0	I/O_7	I/O_6	GND	GND	I/O_{25}	I/O_{24}	I_3
D	$JTAG_{EN}$	I/O_8	I/O_9	GND	GND	I/O_{22}	I/O_{23}	CLK_3/ I_2
E	CLK_0/ I_1	I/O_{12}	I/O_{11}	I/O_{10}	I/O_{16}	I/O_{20}	I/O_{21}	V_{CC}
F	I/O_{13} TMS	V_{CC}	I/O_{14}	I/O_{15}	I/O_{17}	I/O_{18}	V_{CC}	I/O_{19} TDO

Note:
20. For 3.3V versions (Ultra37000V), $V_{CCO} = V_{CC}$.

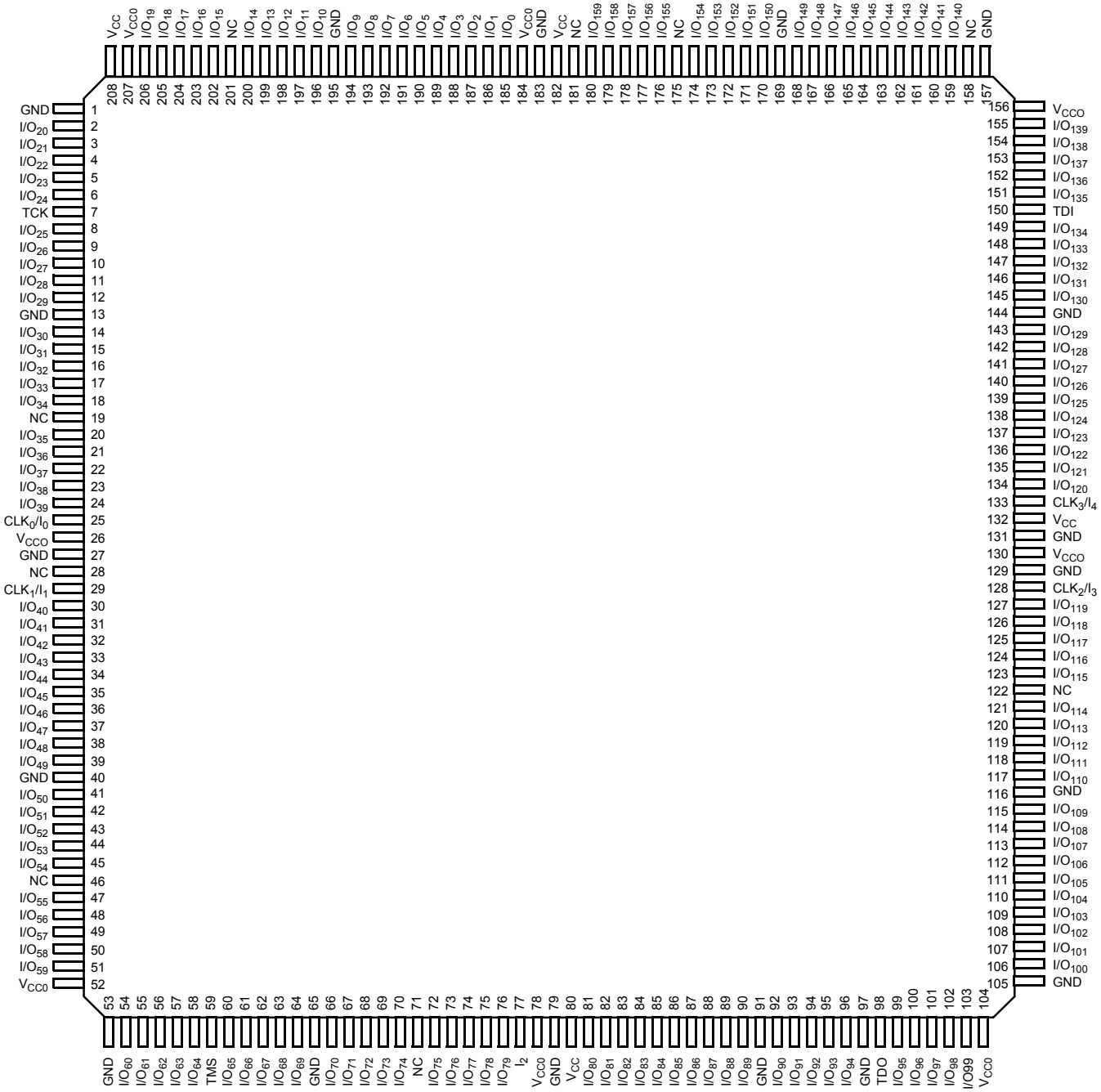
84-lead PLCC (J83) / CLCC (Y84)
Top View



Note:
21. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations[20] (continued)

208-Lead PQFP (N208) / CQFP (U208)
Top View



Pin Configurations[20] (continued)

292-Ball PBGA (BG292)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O_{21}	NC	I/O_{16}	I/O_{12}	I/O_{9}	I/O_{7}	I/O_{4}	I/O_{0}	I/O_{190}	I/O_{189}	I/O_{186}	I/O_{182}	NC	I/O_{178}	I/O_{175}	NC	NC	I/O_{169}	I/O_{168}	A
B	I/O_{23}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{15}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{1}	I/O_{191}	I/O_{187}	I/O_{185}	I/O_{181}	NC	NC	I/O_{174}	I/O_{171}	I/O_{170}	NC	I/O_{166}	B
C	NC	NC	I/O_{22}	NC	I/O_{17}	I/O_{14}	I/O_{10}	I/O_{6}	I/O_{2}	NC	I/O_{188}	I/O_{184}	I/O_{180}	I/O_{179}	I/O_{176}	I/O_{173}	I/O_{172}	I/O_{167}	I/O_{165}	I/O_{162}	C
D	I/O_{24}	NC	NC	GND	NC	V_{CCO}	I/O_{13}	GND	I/O_{3}	NC	V_{CC}	I/O_{183}	GND	I/O_{177}	V_{CCO}	NC	GND	I/O_{164}	TDI	I/O_{160}	D
E	I/O_{27}	I/O_{26}	I/O_{25}	NC													I/O_{163}	I/O_{161}	I/O_{159}	I/O_{156}	E
F	I/O_{30}	TCK	I/O_{28}	V_{CCO}													V_{CCO}	I/O_{158}	NC	I/O_{154}	F
G	I/O_{33}	I/O_{32}	I/O_{31}	I/O_{29}													I/O_{157}	I/O_{155}	I/O_{153}	I/O_{152}	G
H	I/O_{35}	NC	I/O_{34}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{151}	I/O_{150}	I/O_{149}	H
J	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{36}				GND	GND	GND	GND	GND	GND				I/O_{148}	I/O_{147}	I/O_{146}	I/O_{145}	J
K	I/O_{42}	I/O_{40}	I/O_{41}	V_{CC}				GND	GND	GND	GND	GND	GND				I/O_{144}	CLK_3/I_4	NC	NC	K
L	I/O_{43}	I/O_{44}	I/O_{45}	I/O_{46}				GND	GND	GND	GND	GND	GND				V_{CC}	CLK_2/I_3	I/O_{143}	NC	L
M	I/O_{47}	CLK_0/I_0	CLK_1/I_1	I/O_{48}				GND	GND	GND	GND	GND	GND				I/O_{139}	I/O_{140}	I/O_{141}	I/O_{142}	M
N	I/O_{49}	I/O_{50}	I/O_{51}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{136}	I/O_{137}	I/O_{138}	N
P	I/O_{52}	I/O_{53}	I/O_{55}	I/O_{58}													I/O_{131}	I/O_{133}	I/O_{134}	I/O_{135}	P
R	I/O_{54}	I/O_{56}	I/O_{59}	V_{CCO}													V_{CCO}	I/O_{130}	NC	I/O_{132}	R
T	I/O_{57}	I/O_{60}	I/O_{62}	I/O_{65}													I/O_{124}	I/O_{127}	I/O_{128}	I/O_{129}	T
U	I/O_{61}	I/O_{63}	I/O_{66}	GND	I/O_{76}	V_{CCO}	I/O_{82}	GND	I/O_{91}	V_{CC}	I/O_{98}	I/O_{102}	GND	I/O_{112}	V_{CCO}	NC	GND	I/O_{123}	I/O_{122}	I/O_{126}	U
V	I/O_{64}	I/O_{67}	I/O_{69}	I/O_{75}	I/O_{78}	I/O_{81}	I/O_{85}	I/O_{88}	I/O_{92}	I_2	I/O_{97}	I/O_{101}	I/O_{105}	I/O_{109}	I/O_{113}	TDO	I/O_{114}	I/O_{117}	I/O_{121}	I/O_{125}	V
W	I/O_{68}	I/O_{70}	I/O_{72}	I/O_{74}	I/O_{79}	I/O_{83}	I/O_{86}	I/O_{89}	I/O_{93}	I/O_{95}	I/O_{96}	I/O_{100}	I/O_{104}	I/O_{107}	I/O_{110}	NC	NC	I/O_{115}	I/O_{118}	I/O_{120}	W
Y	I/O_{71}	I/O_{73}	I/O_{77}	TMS	I/O_{80}	I/O_{84}	I/O_{87}	I/O_{90}	I/O_{94}	NC	NC	I/O_{99}	I/O_{103}	I/O_{106}	I/O_{108}	I/O_{111}	NC	NC	I/O_{116}	I/O_{119}	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Pin Configurations[20] (continued)

388-Lead PBGA (BG388)

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	GND	I/O_{19}	I/O_{15}	I/O_{13}	I/O_{34}	I/O_{31}	I/O_{28}	I/O_{25}	I/O_{10}	I/O_{7}	I/O_{4}	I/O_{1}	I/O_{263}	I/O_{260}	I/O_{257}	I/O_{254}	I/O_{239}	I/O_{237}	I/O_{232}	I/O_{229}	I/O_{250}	I/O_{248}	I/O_{244}	GND	GND
B	GND	NC	I/O_{18}	I/O_{17}	I/O_{14}	I/O_{35}	I/O_{32}	I/O_{29}	I/O_{26}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{2}	V_{CC}	I/O_{261}	I/O_{258}	I/O_{255}	I/O_{252}	I/O_{234}	I/O_{231}	I/O_{228}	I/O_{249}	I/O_{246}	I/O_{245}	I/O_{240}	GND
C	I/O_{23}	I/O_{38}	I/O_{37}	I/O_{16}	I/O_{12}	I/O_{33}	I/O_{30}	I/O_{27}	I/O_{24}	I/O_{9}	I/O_{6}	I/O_{3}	I/O_{0}	I/O_{262}	I/O_{259}	I/O_{256}	I/O_{253}	I/O_{238}	I/O_{235}	I/O_{233}	I/O_{230}	I/O_{251}	I/O_{247}	I/O_{225}	I/O_{224}	I/O_{227}
D	I/O_{39}	I/O_{40}	I/O_{36}	NC	NC	I/O_{21}	I/O_{20}	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O_{236}	I/O_{243}	NC	NC	I/O_{226}	I/O_{222}	I/O_{223}
E	I/O_{42}	TCK	I/O_{41}	NC																			NC	TDI	I/O_{221}	I/O_{220}
F	I/O_{45}	I/O_{44}	I/O_{43}	I/O_{22}																			I/O_{242}	I/O_{219}	I/O_{218}	I/O_{217}
G	I/O_{48}	I/O_{47}	I/O_{46}	I/O_{63}																			I/O_{241}	I/O_{216}	I/O_{215}	I/O_{214}
H	I/O_{49}	I/O_{50}	I/O_{51}	V_{CCO}																			V_{CCO}	I/O_{211}	I/O_{212}	I/O_{213}
J	I/O_{52}	I/O_{53}	I/O_{54}	V_{CCO}																			V_{CCO}	I/O_{208}	I/O_{209}	I/O_{210}
K	I/O_{55}	I/O_{56}	I/O_{57}	NC																			NC	I/O_{205}	I/O_{206}	I/O_{207}
L	I0	I/O_{59}	I/O_{58}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{204}	I4	I/O_{197}
M	I/O_{61}	I/O_{60}	I1	GND							GND	GND	GND	GND	GND	GND							GND	I3	I/O_{203}	I/O_{202}
N	I/O_{64}	V_{CC}	I/O_{62}	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O_{201}	I/O_{200}	I/O_{199}
P	I/O_{65}	I/O_{66}	I/O_{67}	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O_{196}	V_{CC}	I/O_{198}
R	I/O_{68}	I/O_{69}	I/O_{70}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{193}	I/O_{194}	I/O_{195}
T	I/O_{71}	I/O_{84}	I/O_{85}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{178}	I/O_{179}	I/O_{192}
U	I/O_{88}	I/O_{87}	I/O_{86}	NC																			NC	I/O_{177}	I/O_{176}	I/O_{175}
V	I/O_{91}	I/O_{90}	I/O_{89}	V_{CCO}																			V_{CCO}	I/O_{174}	I/O_{173}	I/O_{172}
W	I/O_{94}	I/O_{93}	I/O_{92}	V_{CCO}																			V_{CCO}	I/O_{171}	I/O_{170}	I/O_{169}
Y	I/O_{95}	I/O_{72}	I/O_{73}	I/O_{110}																			I/O_{153}	I/O_{190}	I/O_{191}	I/O_{168}
AA	I/O_{74}	I/O_{75}	I/O_{76}	I/O_{111}																			I/O_{152}	I/O_{187}	I/O_{188}	I/O_{189}
AB	I/O_{77}	I/O_{78}	I/O_{79}	N/C																			NC	I/O_{184}	I/O_{185}	I/O_{186}
AC	I/O_{81}	I/O_{80}	I/O_{108}	N/C	NC	I/O_{112}	I/O_{113}	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O_{150}	I/O_{151}	NC	NC	I/O_{155}	I/O_{183}	I/O_{182}
AD	I/O_{109}	I/O_{82}	I/O_{83}	I/O_{117}	I/O_{97}	I/O_{100}	I/O_{102}	I/O_{105}	I/O_{120}	I/O_{123}	I/O_{126}	I/O_{129}	I2	I/O_{133}	I/O_{136}	I/O_{139}	I/O_{142}	I/O_{157}	I/O_{159}	I/O_{161}	I/O_{163}	I/O_{166}	I/O_{146}	I/O_{180}	I/O_{181}	I/O_{154}
AE	GND	NC	I/O_{115}	I/O_{116}	I/O_{119}	I/O_{98}	I/O_{101}	I/O_{103}	I/O_{106}	I/O_{121}	I/O_{124}	I/O_{127}	V_{CC}	I/O_{130}	I/O_{134}	I/O_{137}	I/O_{140}	I/O_{143}	I/O_{160}	I/O_{162}	I/O_{165}	I/O_{144}	I/O_{147}	I/O_{148}	NC	GND
AF	GND	GND	I/O_{114}	I/O_{118}	I/O_{96}	I/O_{99}	TMS	I/O_{104}	I/O_{107}	I/O_{122}	I/O_{125}	I/O_{128}	I/O_{131}	I/O_{132}	I/O_{135}	I/O_{138}	I/O_{141}	I/O_{156}	I/O_{158}	TDO	I/O_{164}	I/O_{167}	I/O_{145}	I/O_{149}	GND	GND

5.0V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military

5.0V Ordering Information (continued)

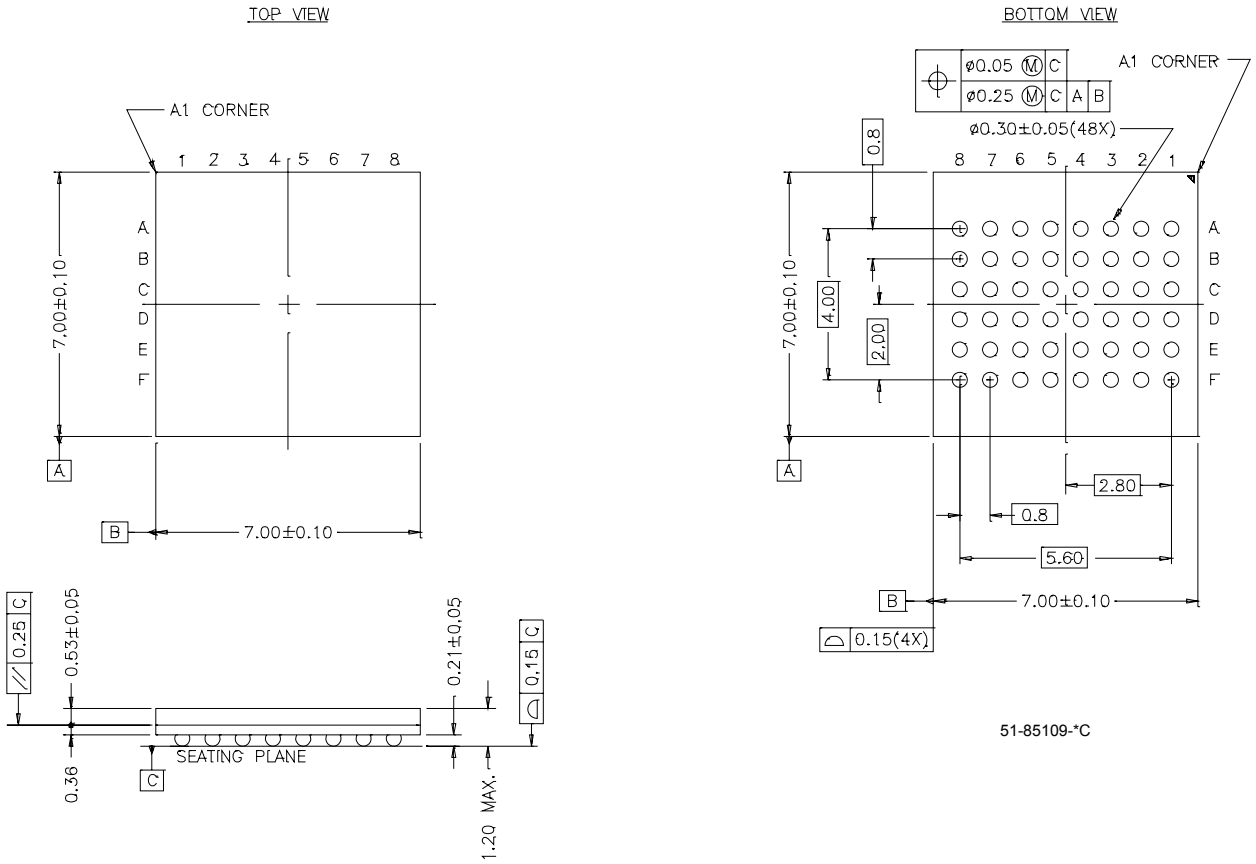
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	154	CY37256P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-154AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-154NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-154BGC	BG292	292-Ball Plastic Ball Grid Array	
	125	CY37256P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-125NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952302QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
	83	CY37256P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256P208-83NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		5962-9952301QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	125	CY37384P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
	83	CY37384P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	

3.3V Ordering Information (continued)

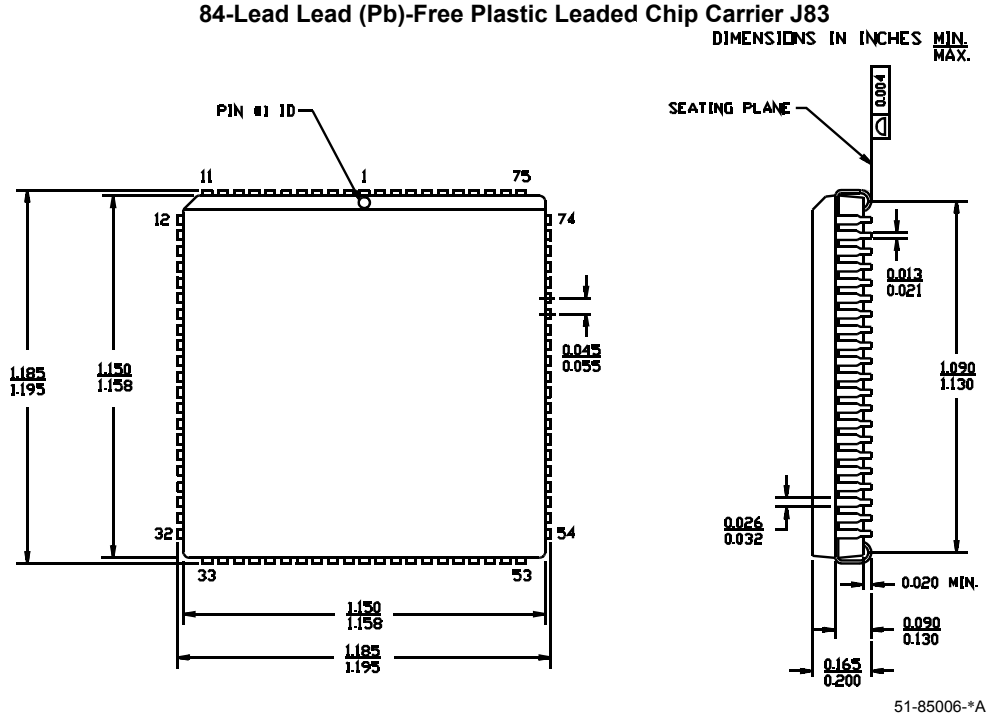
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	143	CY37064VP44-143AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-143BAC	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-143AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-143AXC	A100	100-Lead Lead Free Thin Quad Flatpack	
		CY37064VP100-143BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
	100	CY37064VP44-100AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-100BAC	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100AXC	A100	100-Lead Lead Free Thin Quad Flatpack	
		CY37064VP100-100BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37064VP44-100AI	A44	44-Lead Thin Quad Flatpack	Industrial
		CY37064VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-100BAI	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100BBI	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100AI	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100AXI	A100	100-Lead Lead Free Thin Quad Flatpack	
		5962-9952001QYA	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
128	125	CY37128VP100-125AC	A100	100-Lead Thin Quad Flat Pack	Commercial
		CY37128VP100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-125BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37128VP160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	83	CY37128VP100-83AC	A100	100-Lead Thin Quad Flat Pack	Commercial
		CY37128VP100-83AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-83AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83AI	A100	100-Lead Thin Quad Flat Pack	Industrial
		CY37128VP100-83AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83BBI	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-83AI	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		5962-9952201QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	100	CY37192VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37192VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial

Package Diagrams (continued)

48-Ball (7.0 mm x 7.0 mm x 1.2 mm, 0.80 pitch) Thin BGA BA48D

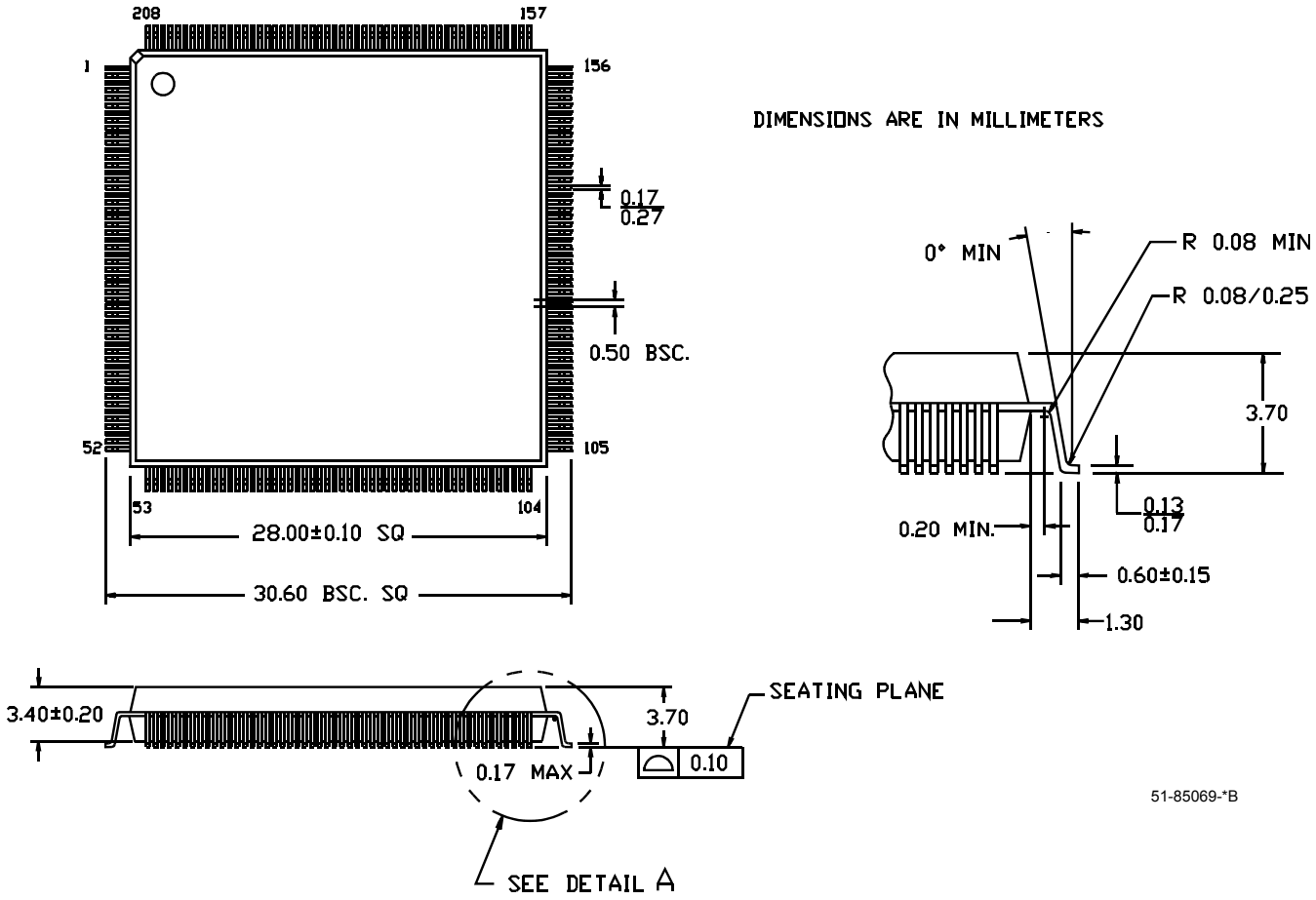


84-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J83



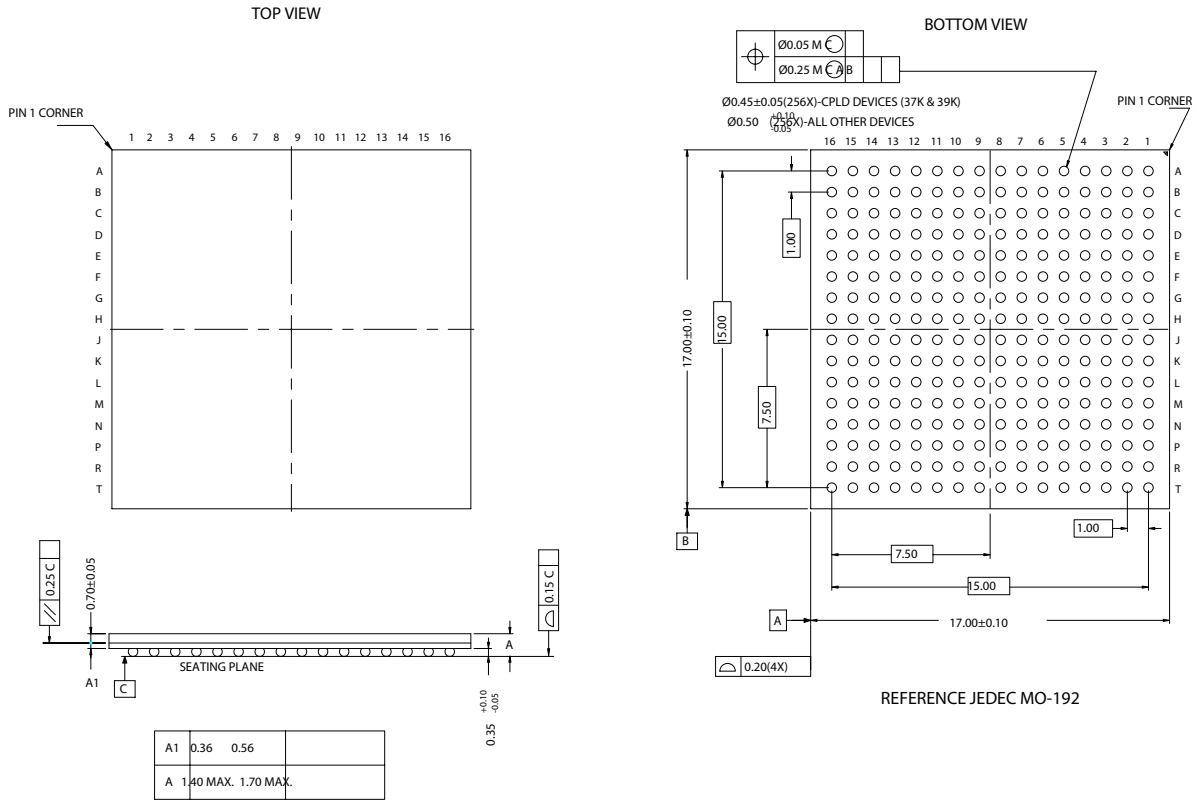
Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



Package Diagrams (continued)

256-Ball FBGA (17 x 17 mm) BB256

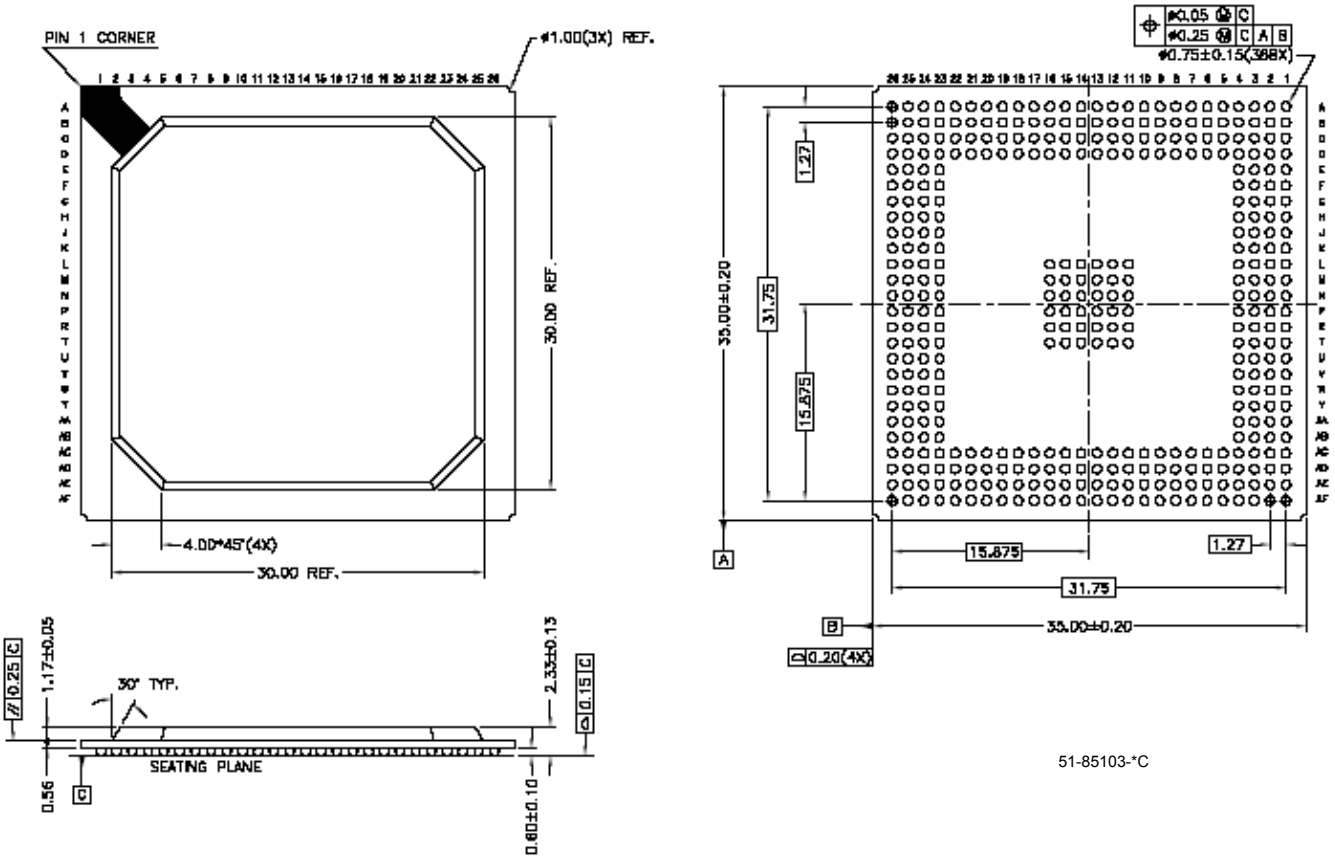


A1	0.36	0.56	
A	1.40 MAX.	1.70 MAX.	

51-85108-*F

Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388



51-85103-*C