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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	133
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37256p160-83axc

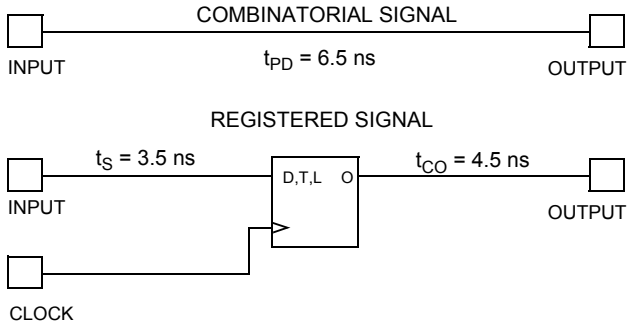


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

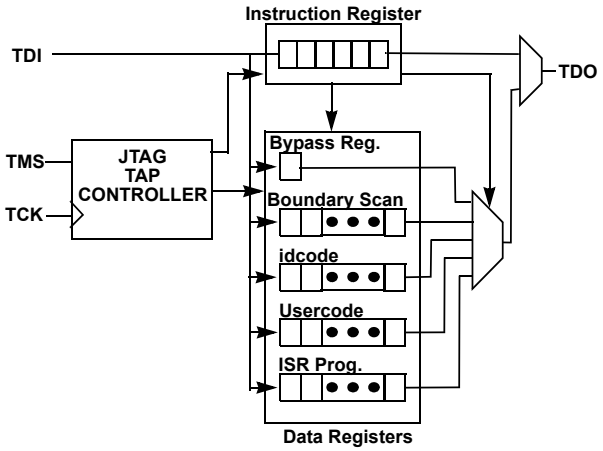


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC*, Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

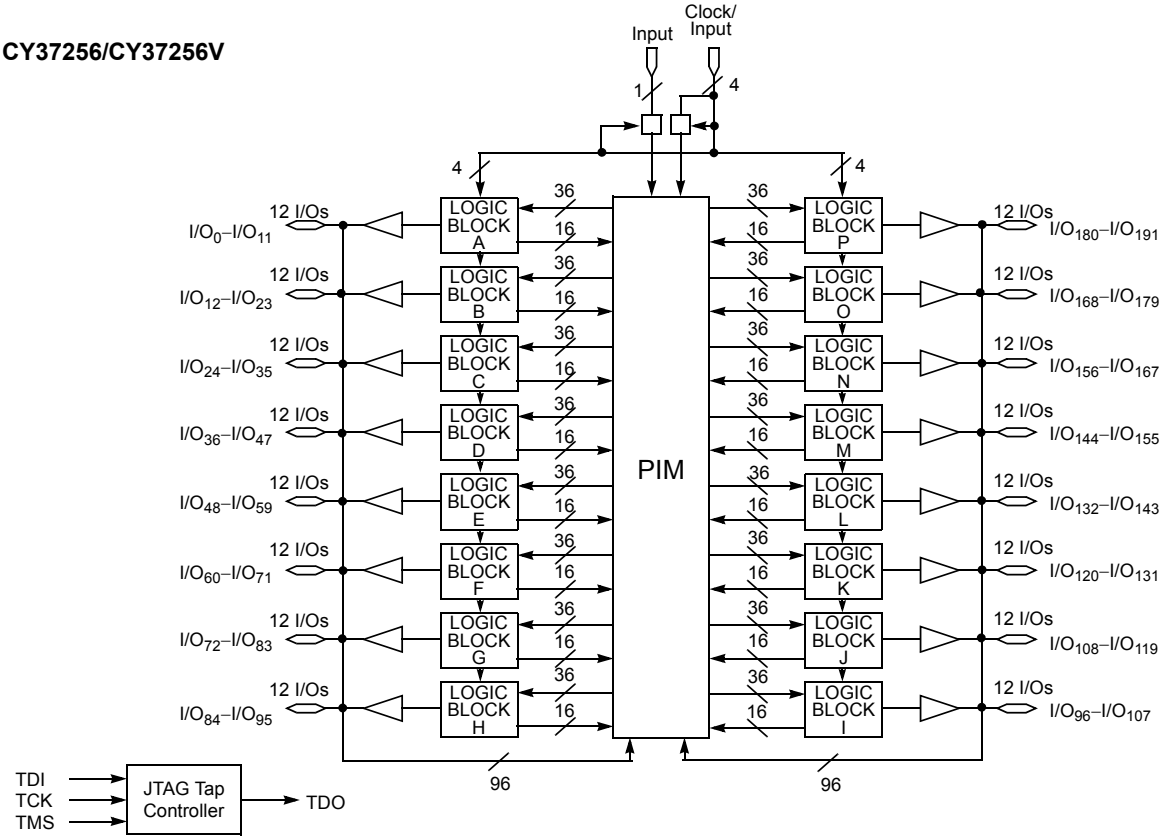
Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

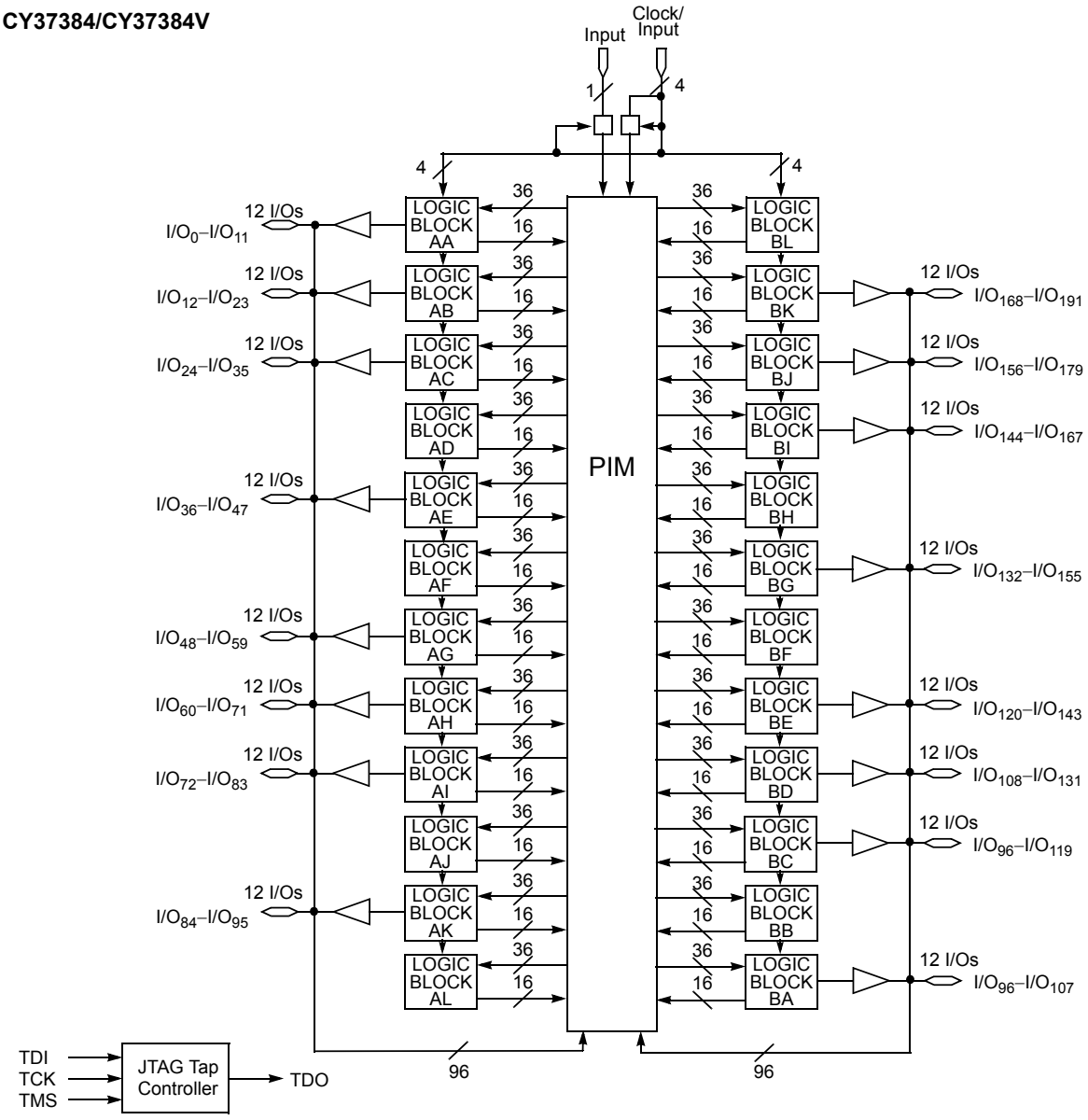
Logic Block Diagrams (continued)

CY37256/CY37256V



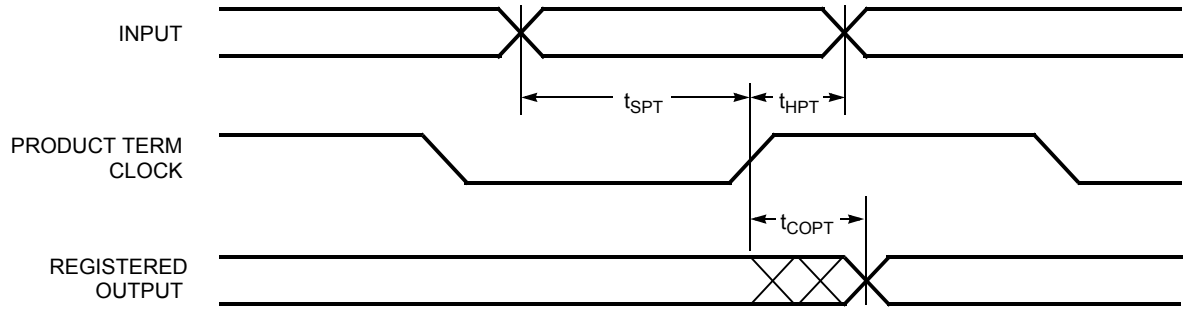
Logic Block Diagrams (continued)

CY37384/CY37384V

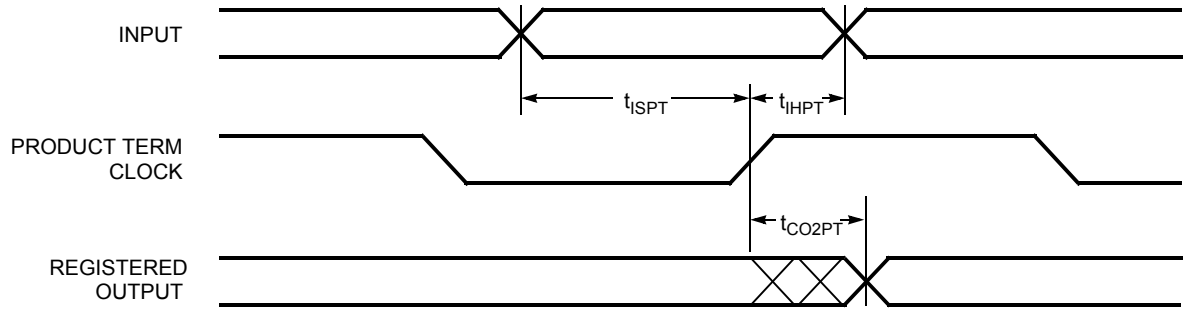


Switching Waveforms (continued)

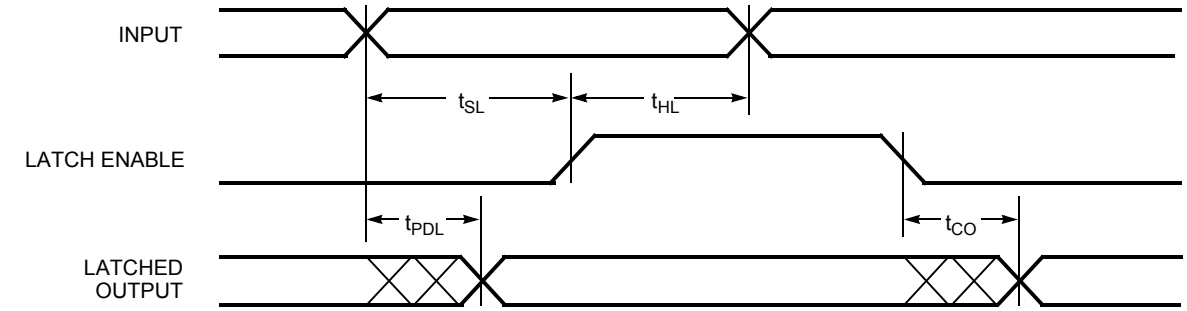
Registered Output with Product Term Clocking Input Going Through the Array



Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register

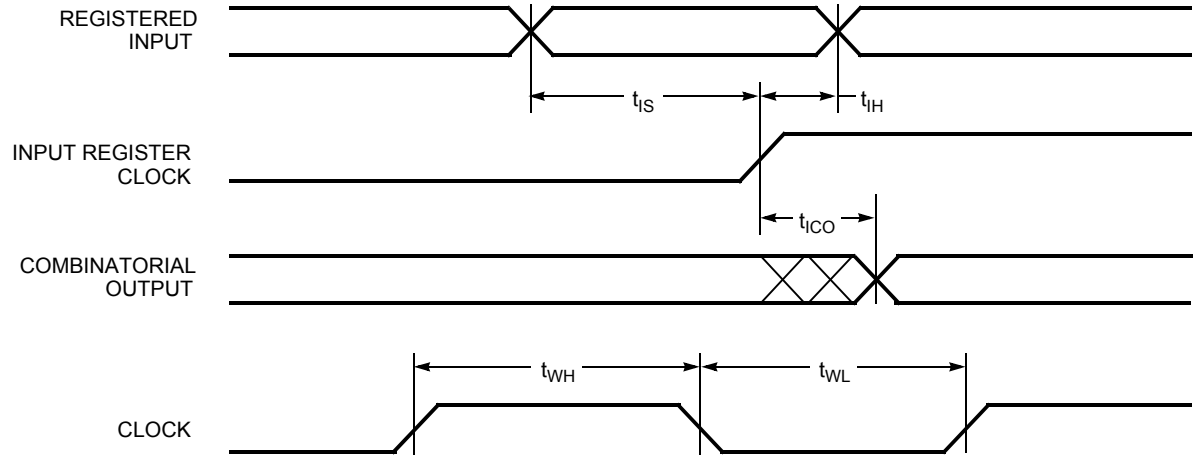


Latched Output

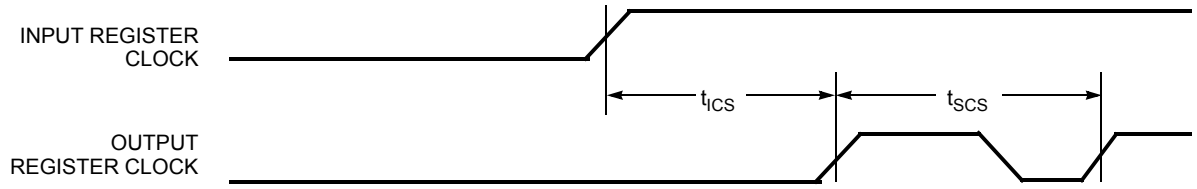


Switching Waveforms (continued)

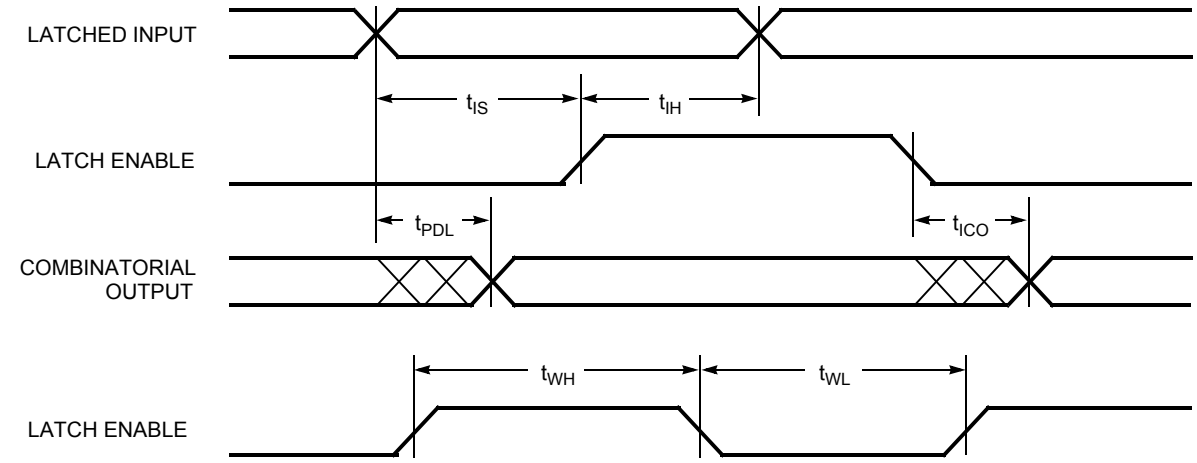
Registered Input



Clock to Clock

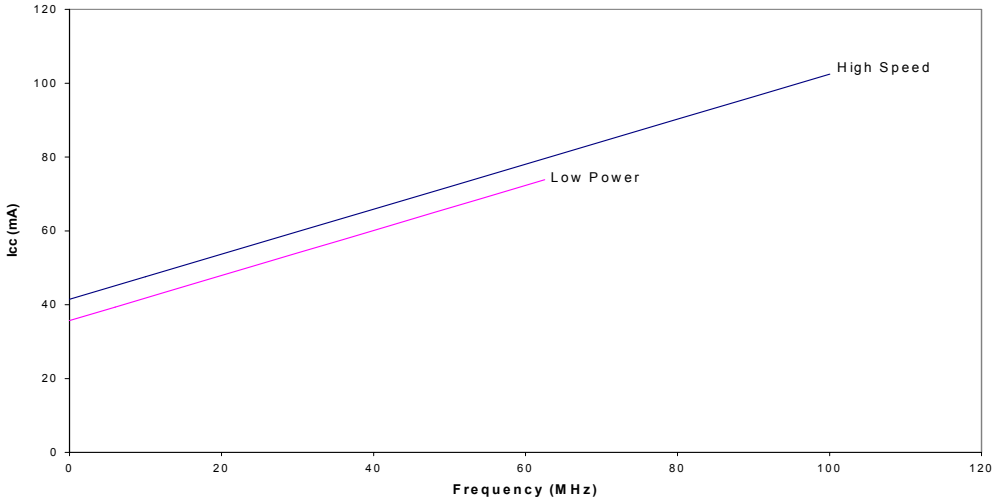


Latched Input



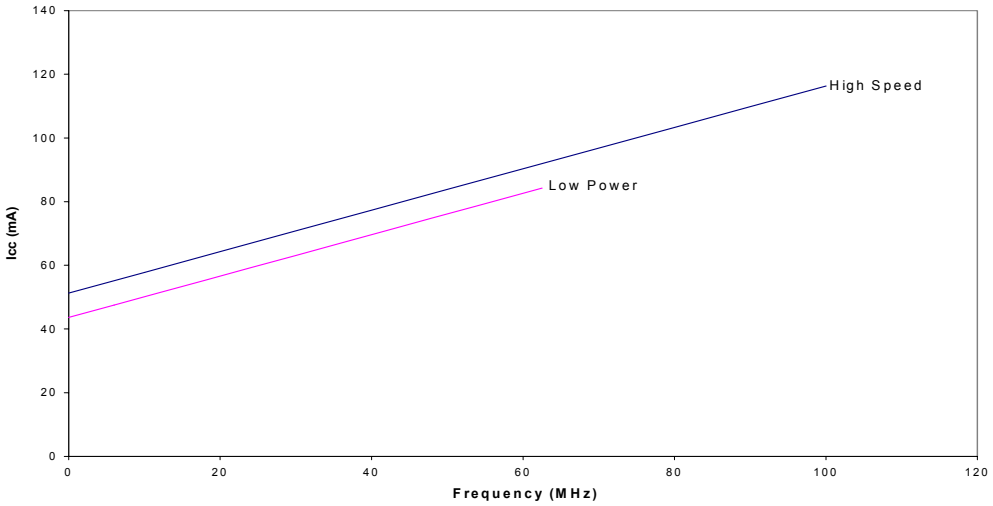
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

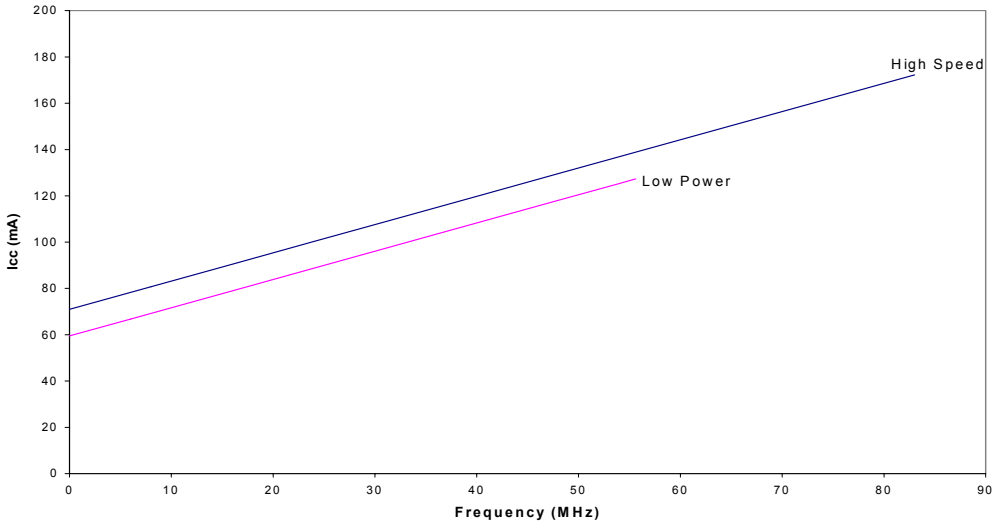
CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

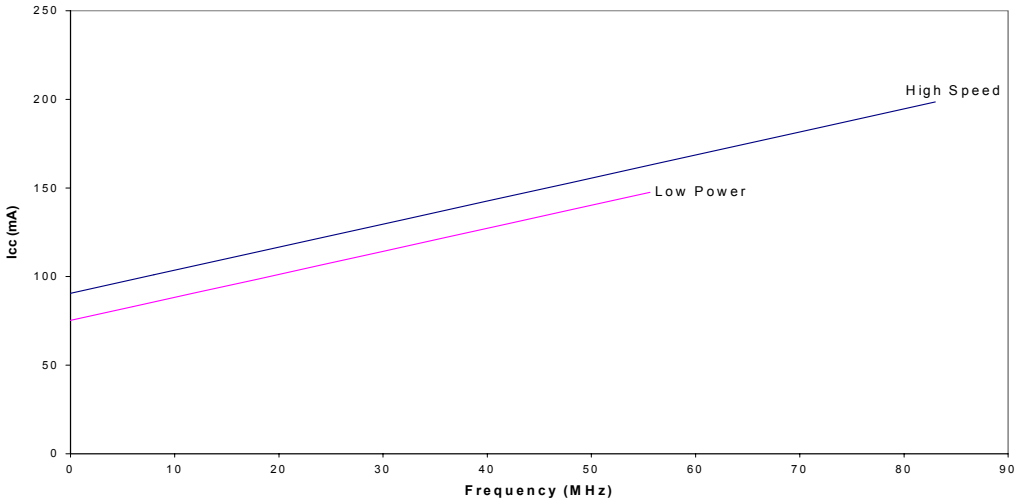
Typical 3.3V Power Consumption (continued)

CY37384V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

CY37512V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

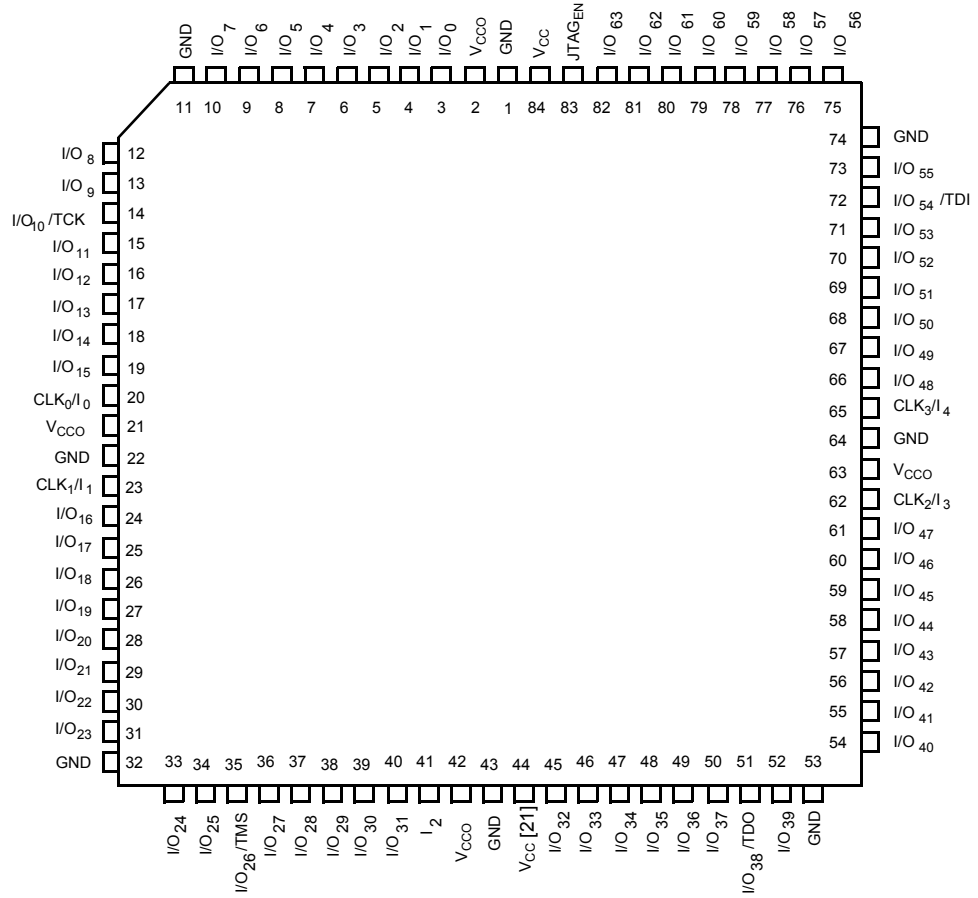
Pin Configurations[20] (continued)

48-ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O_5 TCK	V_{CC}	I/O_3	I/O_1	I/O_{31}	I/O_{30}	V_{CC}	I/O_{27} TDI
B	V_{CC}	I/O_4	I/O_2	I/O_0	I/O_{29}	I/O_{28}	I/O_{26}	CLK_1/ I_4
C	CLK_2/ I_0	I/O_7	I/O_6	GND	GND	I/O_{25}	I/O_{24}	I_3
D	$JTAG_{EN}$	I/O_8	I/O_9	GND	GND	I/O_{22}	I/O_{23}	CLK_3/ I_2
E	CLK_0/ I_1	I/O_{12}	I/O_{11}	I/O_{10}	I/O_{16}	I/O_{20}	I/O_{21}	V_{CC}
F	I/O_{13} TMS	V_{CC}	I/O_{14}	I/O_{15}	I/O_{17}	I/O_{18}	V_{CC}	I/O_{19} TDO

Note:
20. For 3.3V versions (Ultra37000V), $V_{CCO} = V_{CC}$.

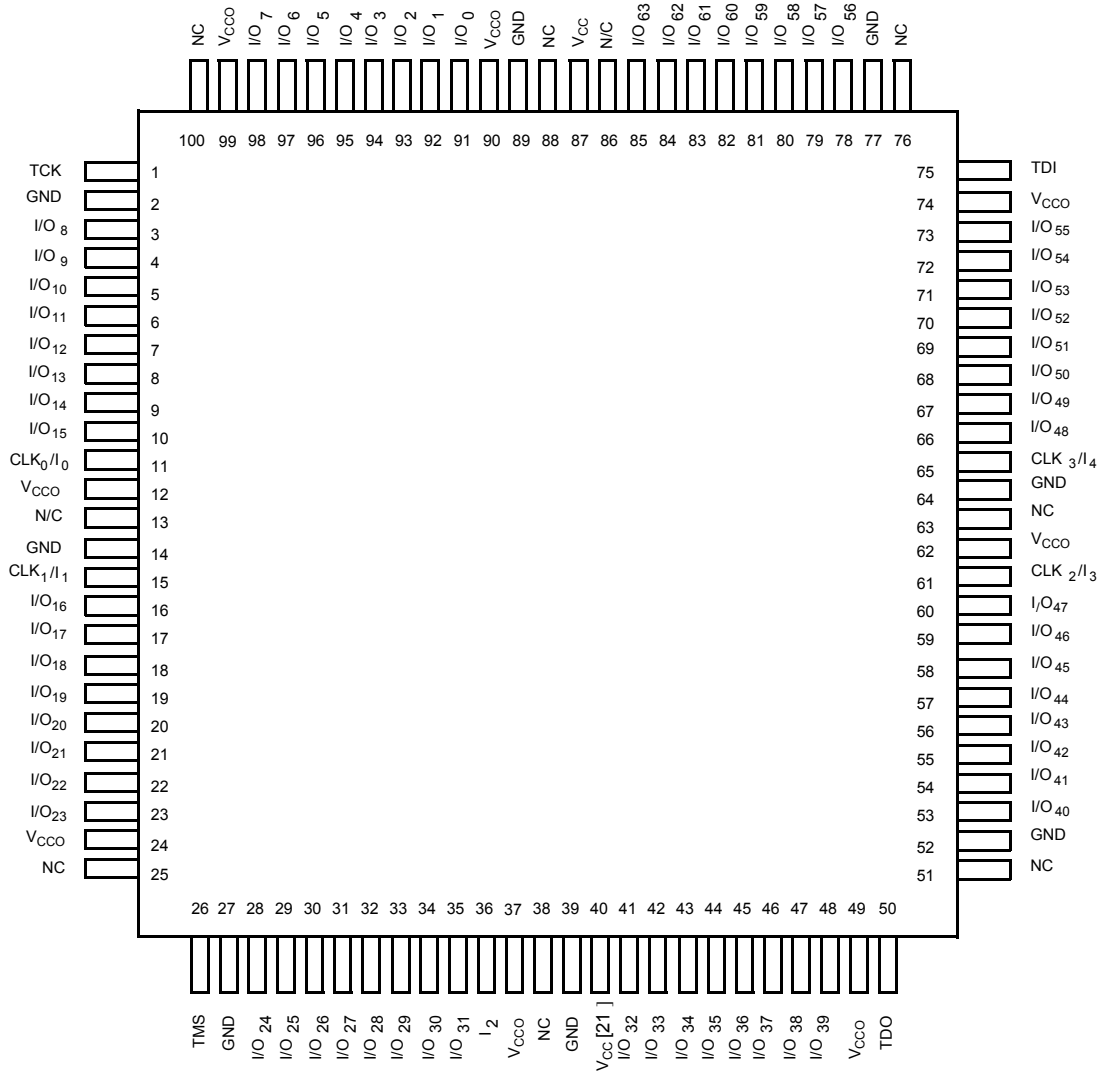
84-lead PLCC (J83) / CLCC (Y84)
Top View



Note:
21. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

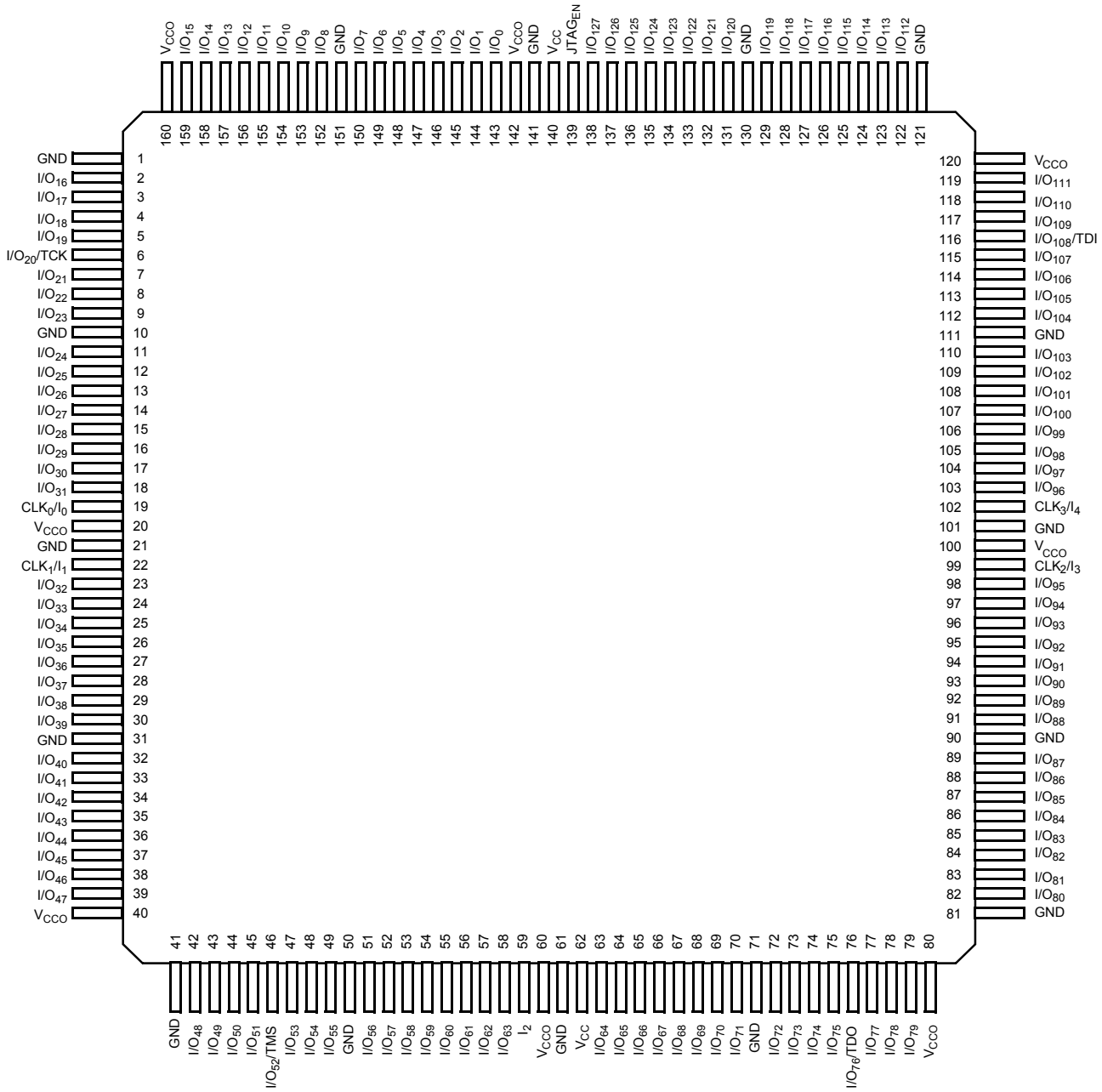
Pin Configurations[20] (continued)

100-lead TQFP (A100)
Top View



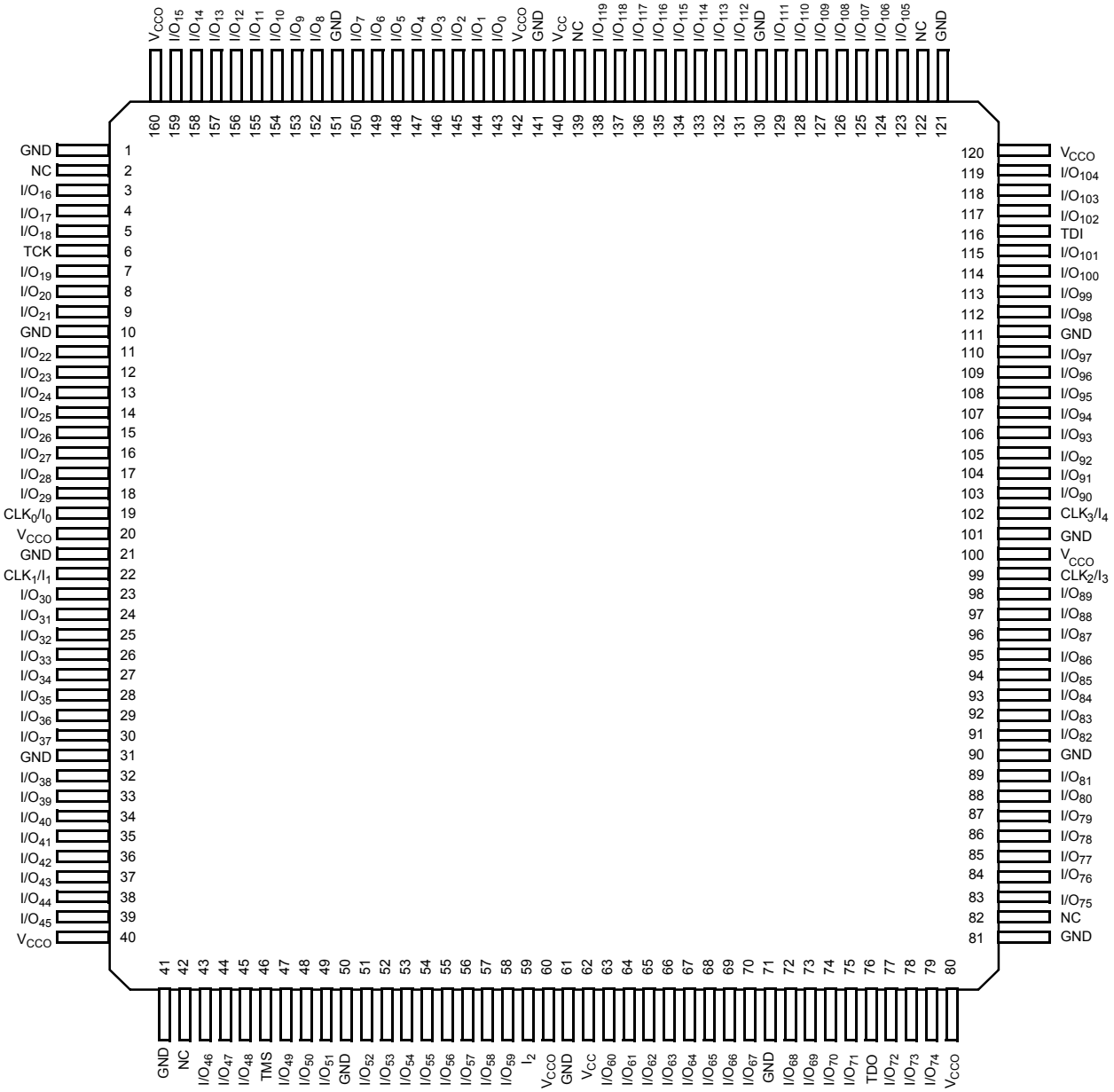
Pin Configurations[20] (continued)

160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View



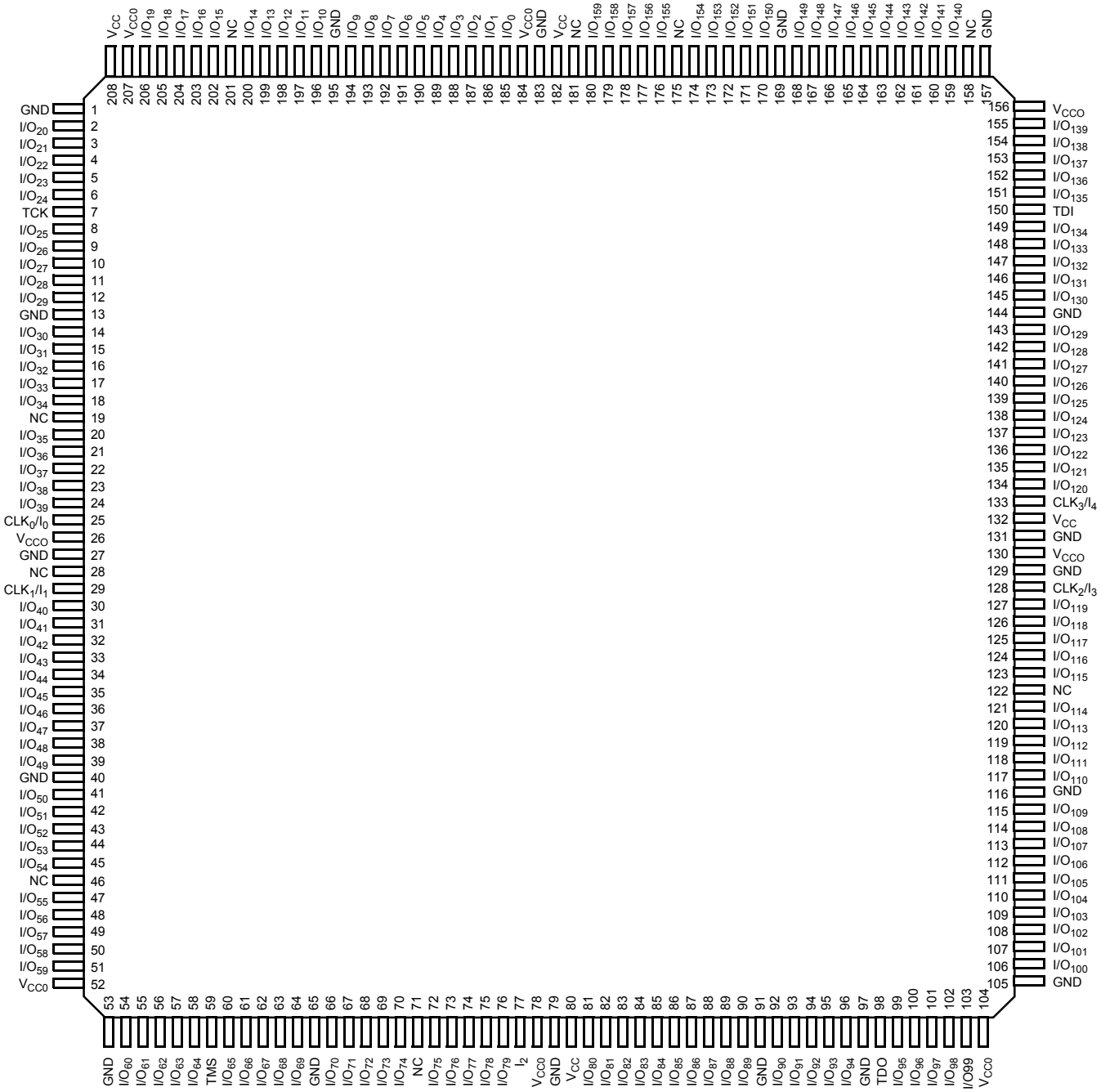
Pin Configurations[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View

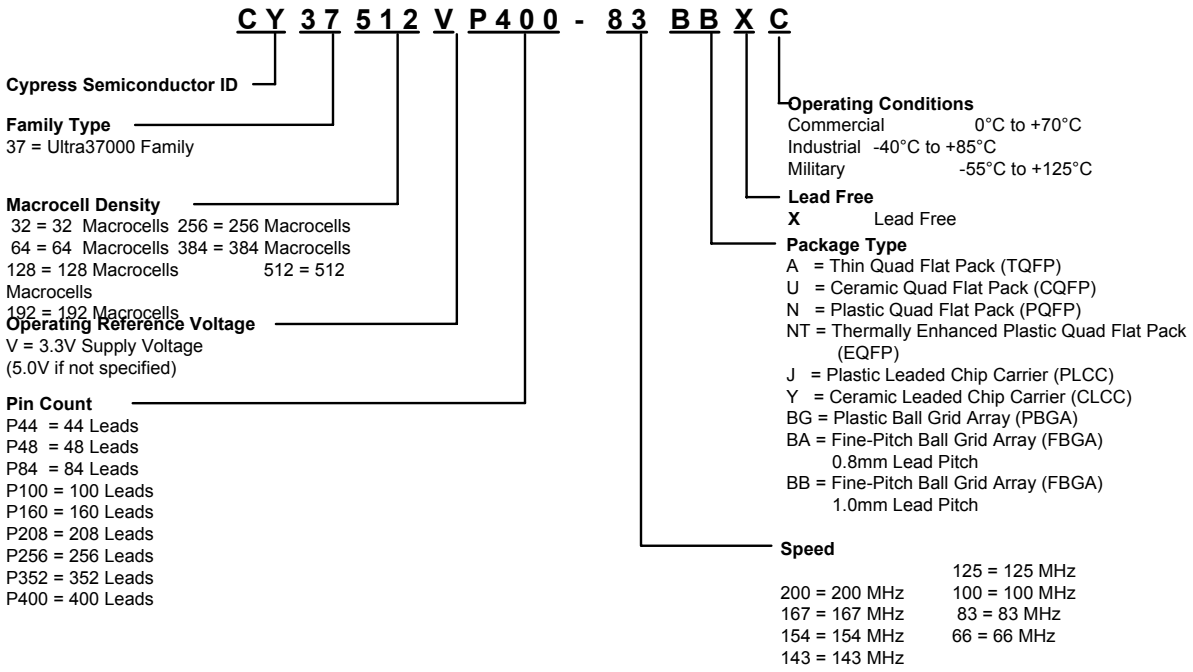


Pin Configurations[20] (continued)

208-Lead PQFP (N208) / CQFP (U208)
Top View



Ordering Information



5.0V Ordering Information

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	200	CY37032P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-200AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-200JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
	154	CY37032P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
	125	CY37032P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37032P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
64	200	CY37064P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-200AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-200JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-200JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-200AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-200AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	

5.0V Ordering Information (continued)

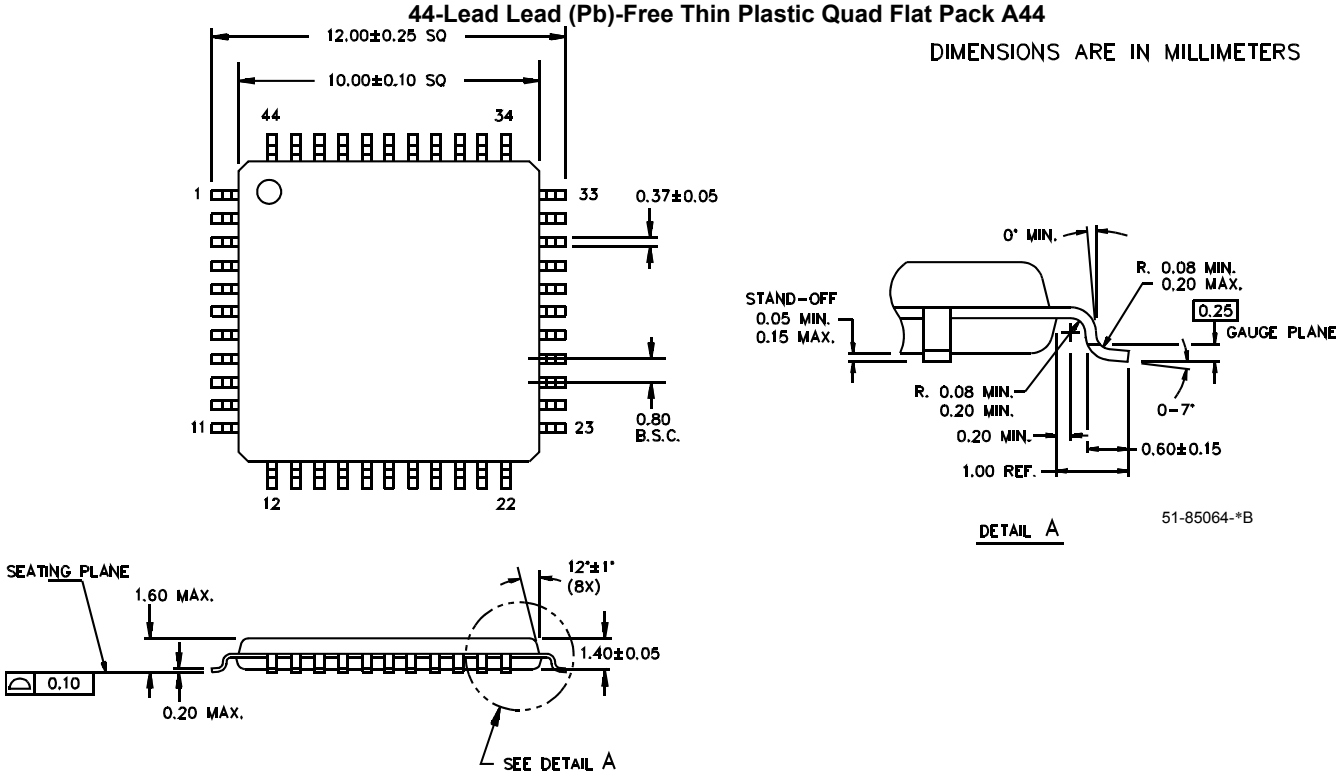
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-125BGC	BG388	388-Ball Plastic Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-100BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512P352-83BGI	BG388	388-Ball Plastic Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

3.3V Ordering Information

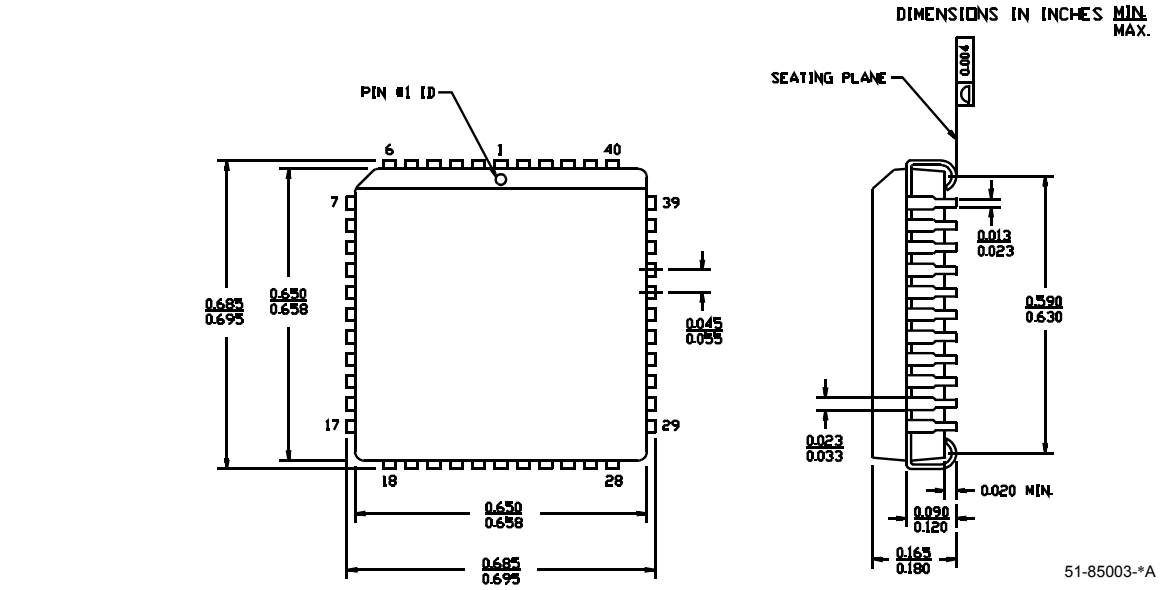
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-143BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAC	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032VP48-100BAI	BA50	48-Ball Fine Pitch Ball Grid Array	
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP44-100JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	

Package Diagrams

44-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack A44

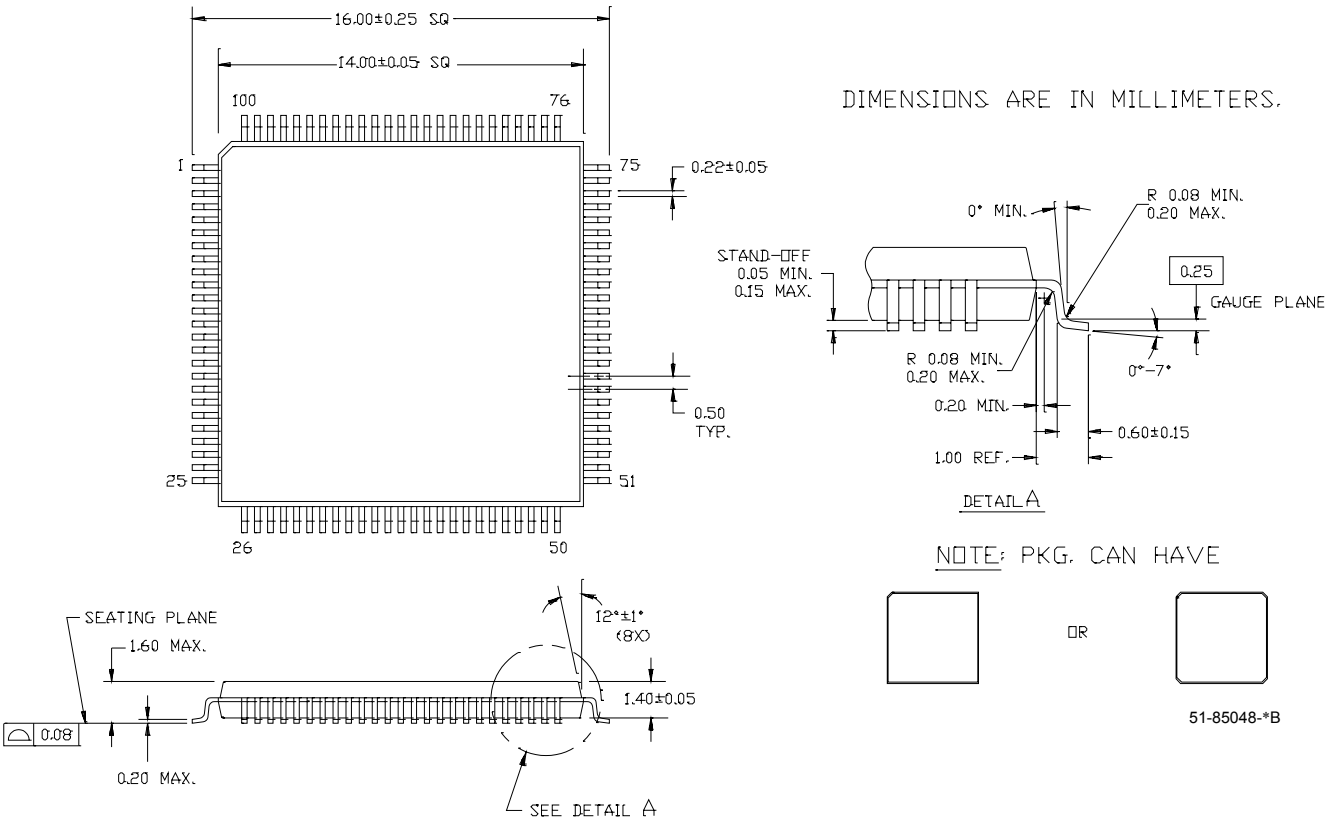


44-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J67



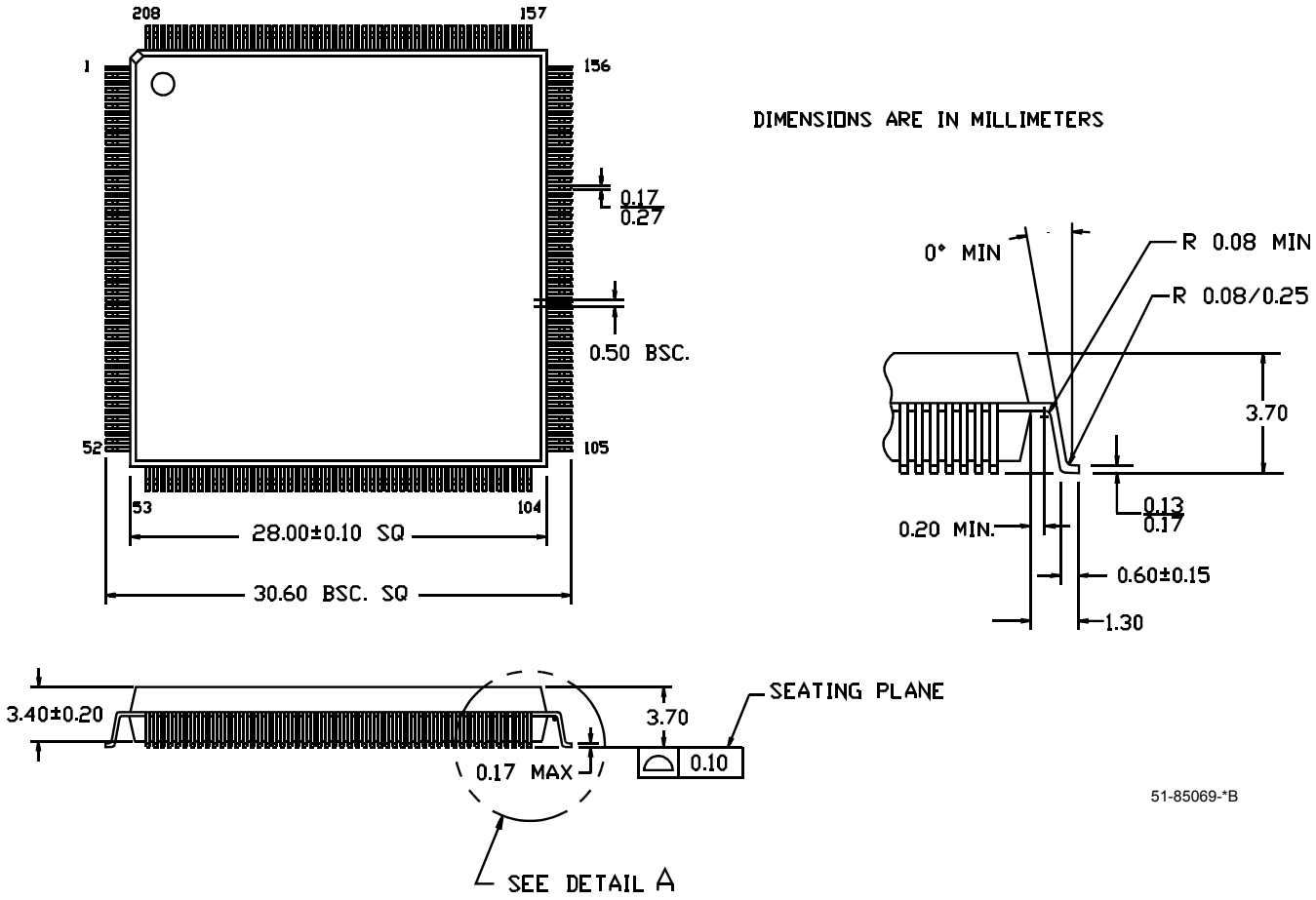
Package Diagrams (continued)

100-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (TQFP) A100



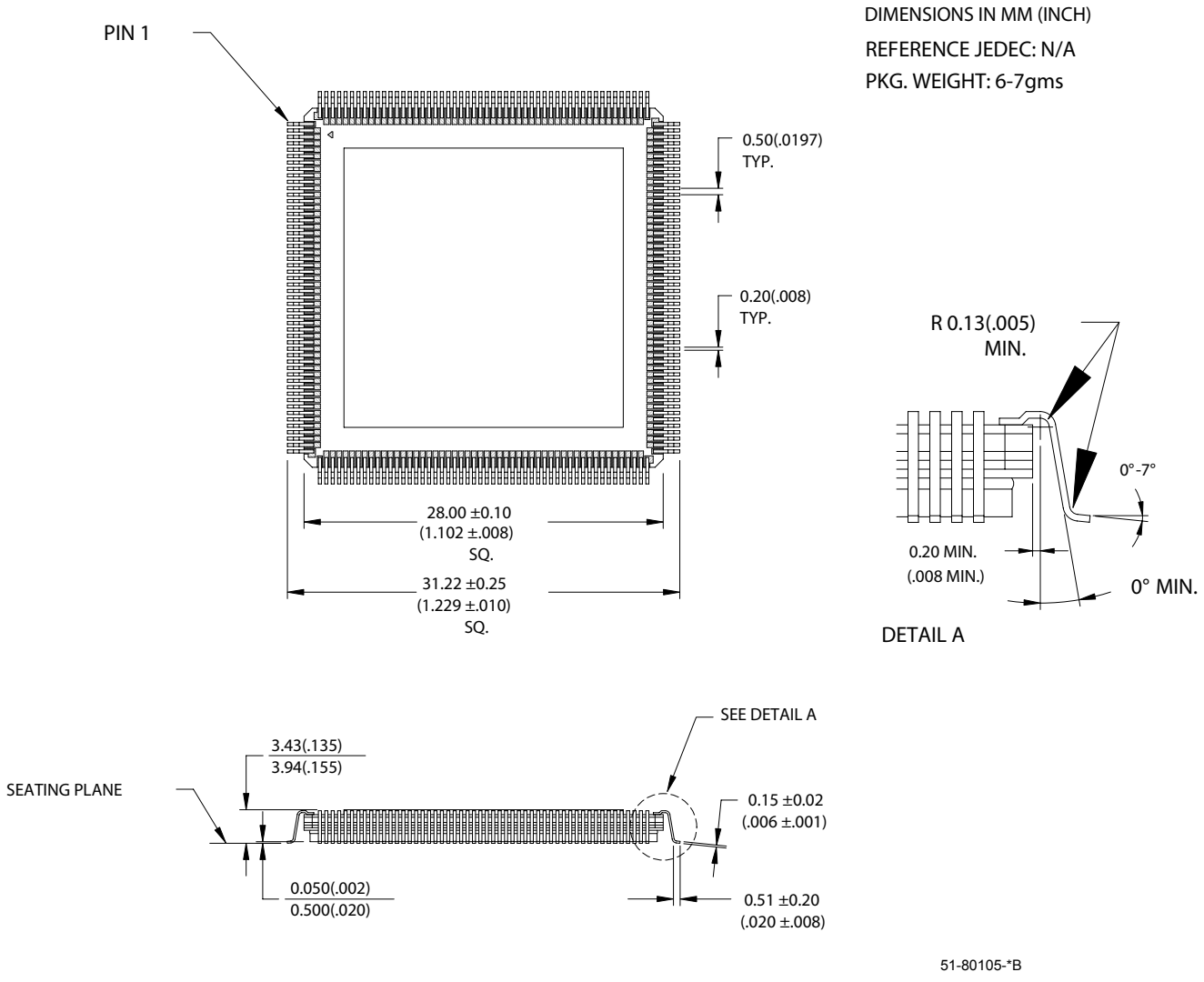
Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



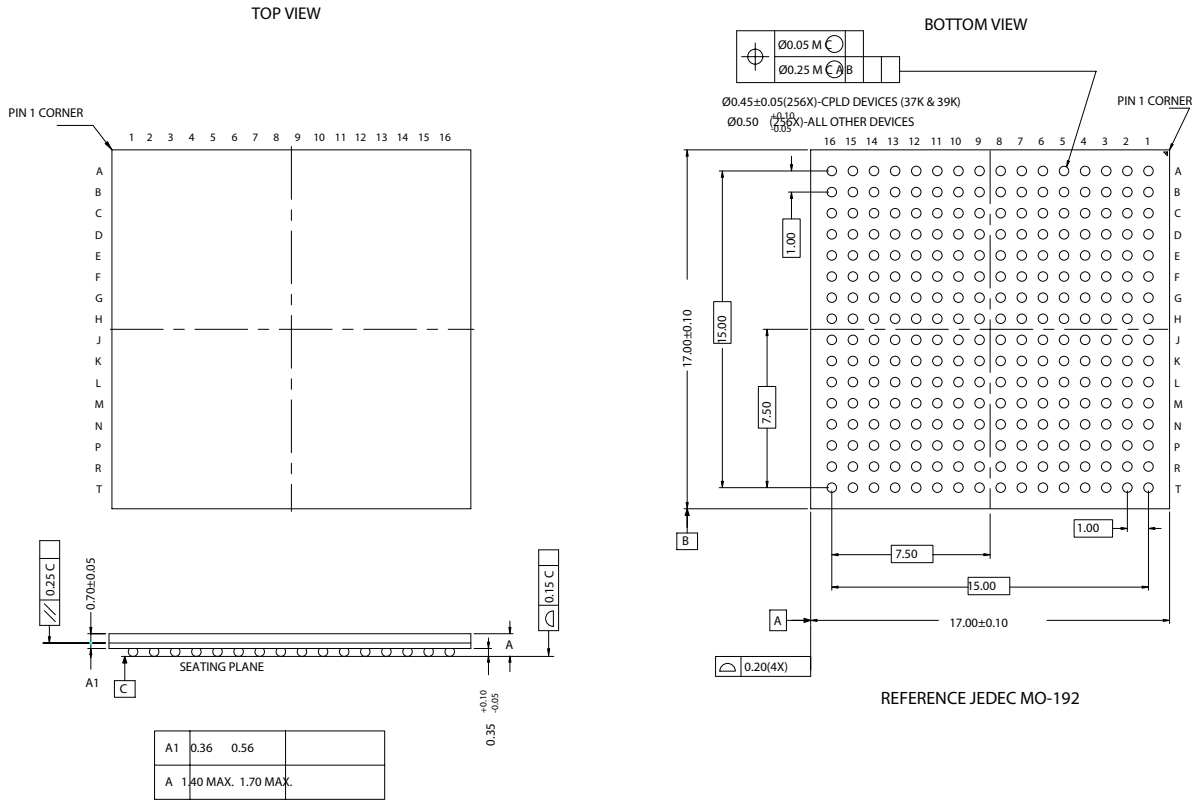
Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208



Package Diagrams (continued)

256-Ball FBGA (17 x 17 mm) BB256

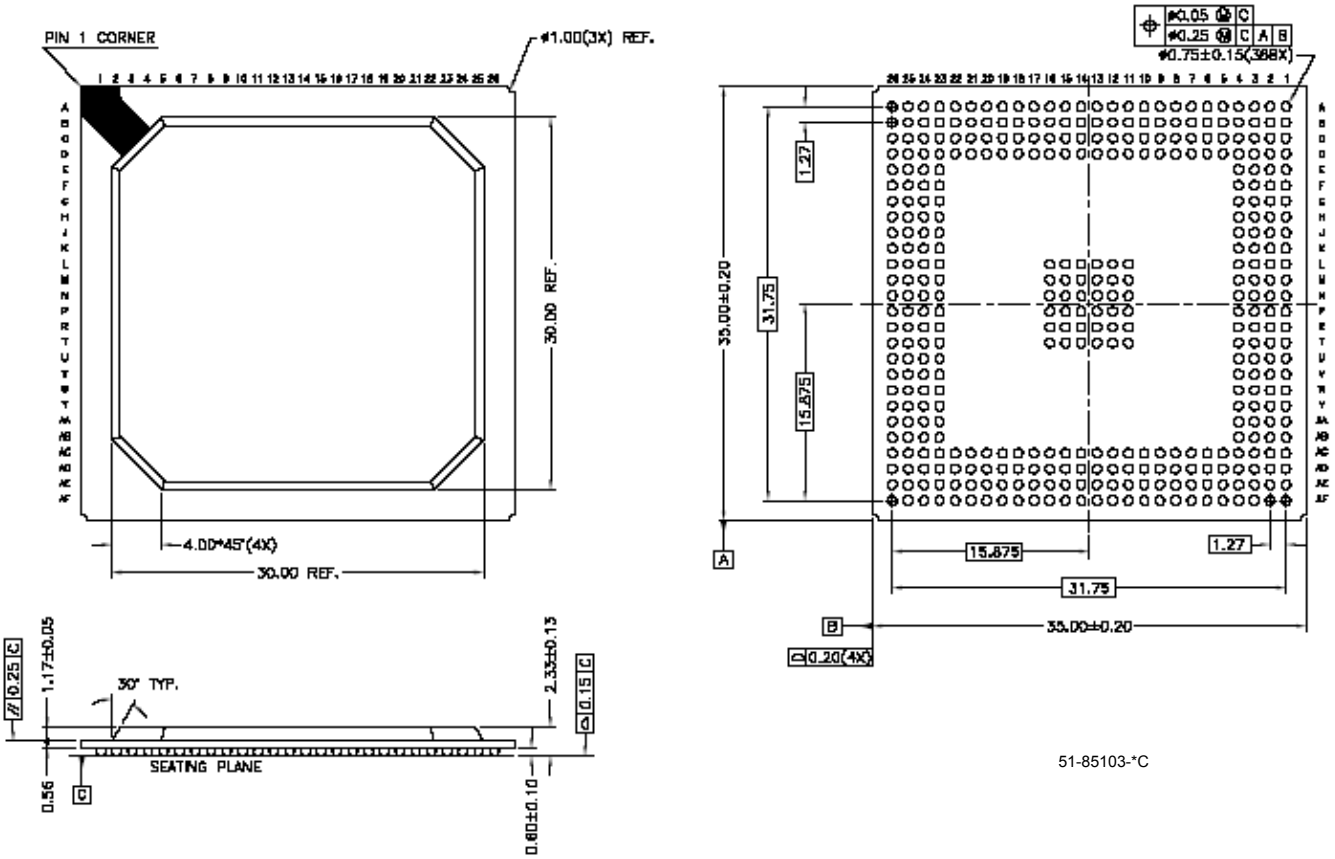


A1	0.36	0.56	
A	1.40 MAX.	1.70 MAX.	

51-85108-*F

Package Diagrams (continued)

388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388



51-85103-*C