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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	165
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37256p208-125nxi

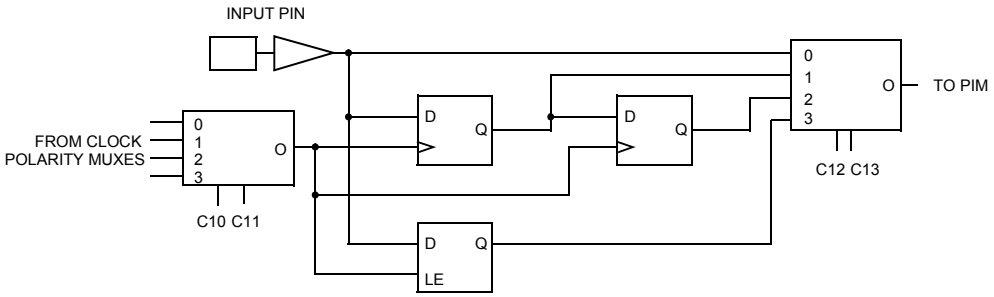


Figure 3. Input Macrocell

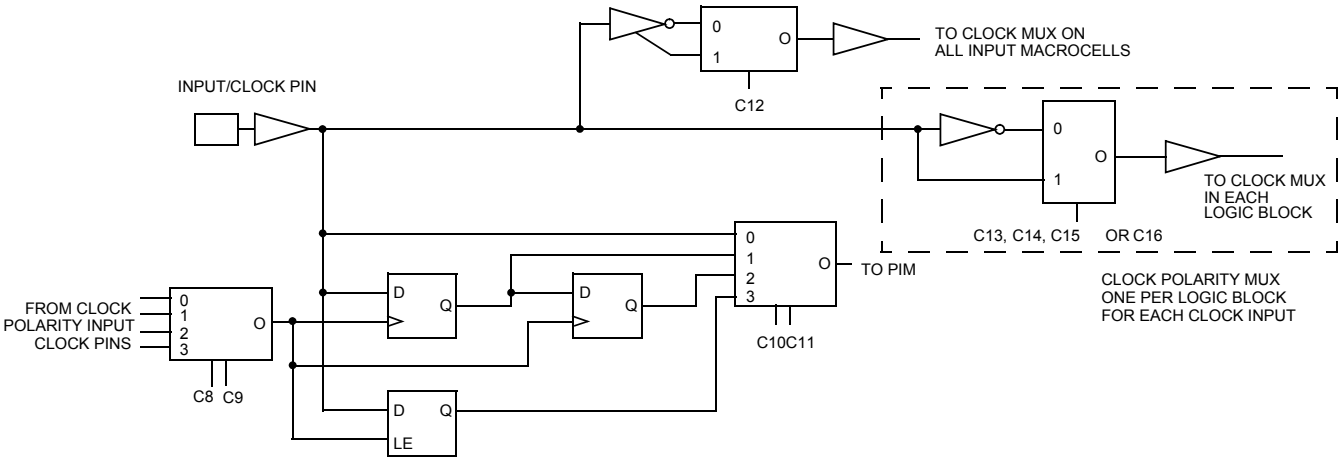


Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

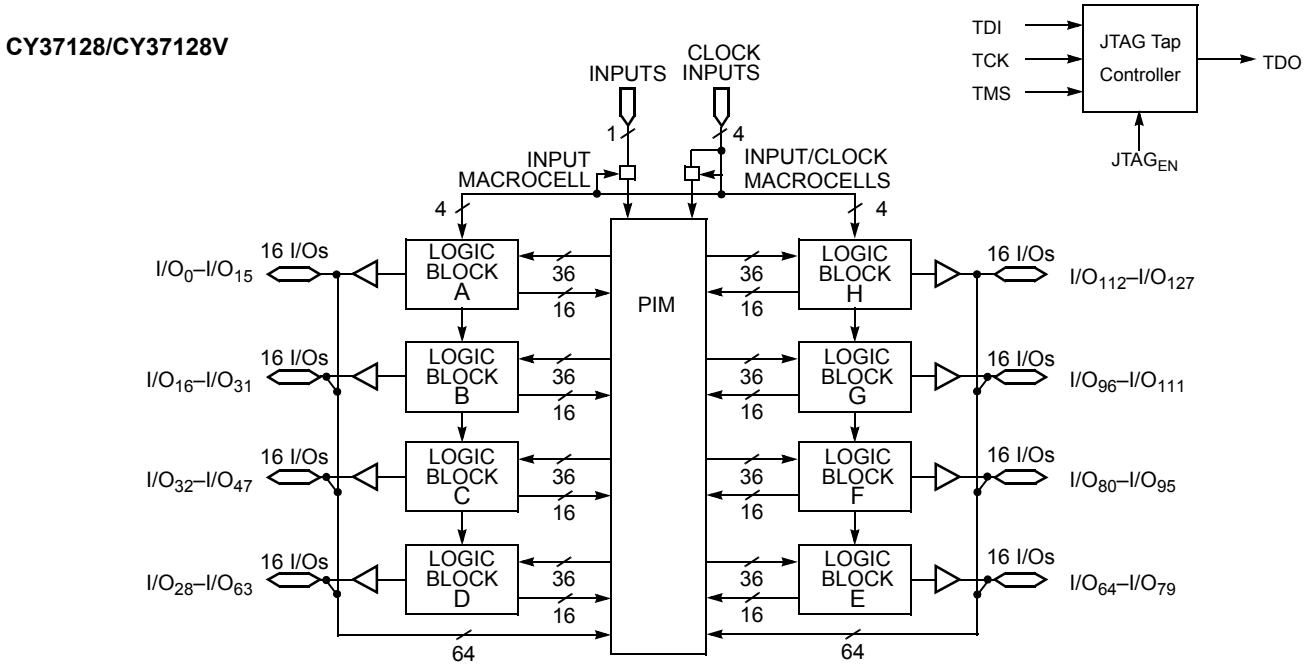
The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

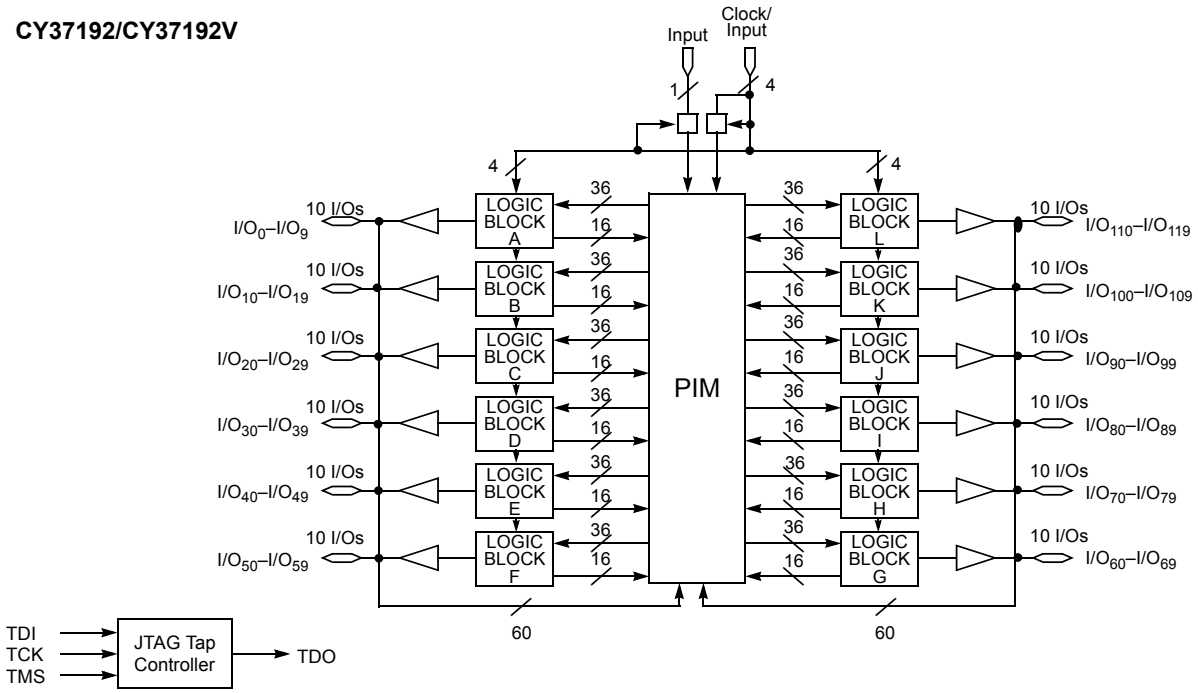
The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

Logic Block Diagrams (continued)

CY37128/CY37128V



CY37192/CY37192V



5.0V Device Characteristics Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage..... 4.5 to 5.5V

Current into Outputs ..... 16 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[5]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l)[6]			4.2	V
			I_{OH} = 0 µA (Ind/Mil)[6]			4.5	V
			I_{OH} = –100 µA (Com'l)[6]			3.6	V
			I_{OH} = –150 µA (Ind/Mil)[6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled "An Introduction to In System Reprogramming with the Ultra37000."
3. T_A is the "Instant On" case temperature.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

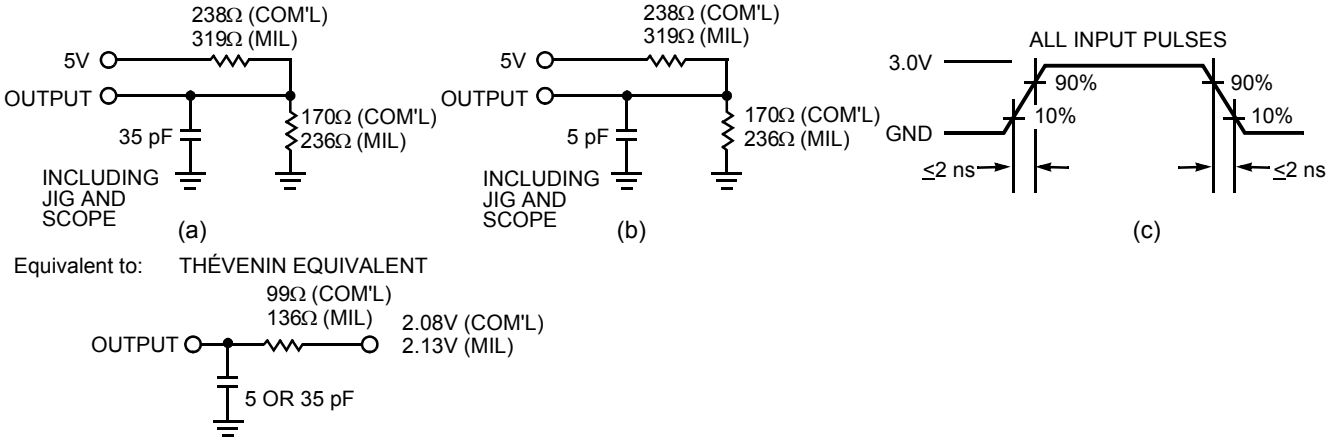
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

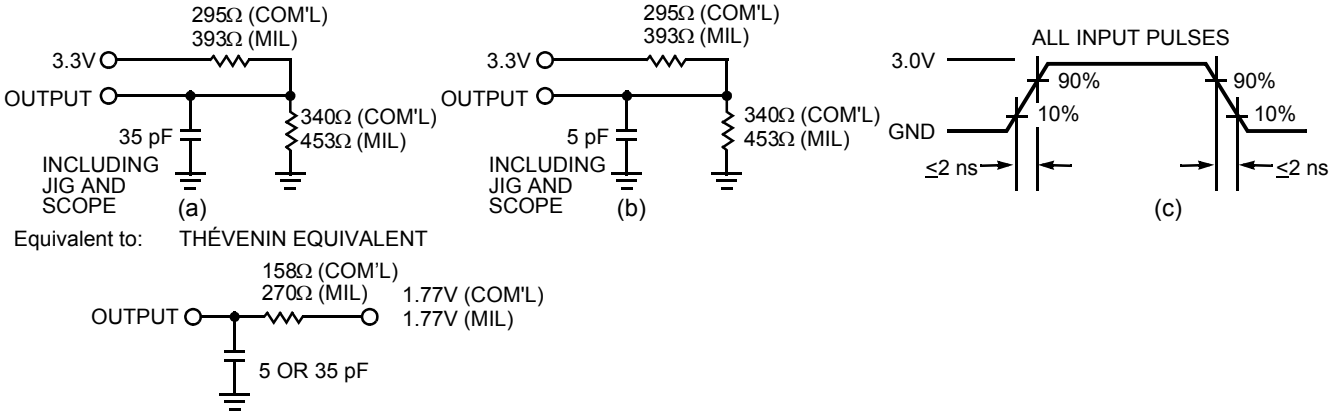
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Characteristics

5.0V AC Test Loads and Waveforms



3.3V AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range [12]

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t_{PD}[13, 14, 15]		6		6.5		7.5		8.5		10		12		15		20	ns
t_{PDL}[13, 14, 15]		11		12.5		14.5		16		16.5		17		19		22	ns
t_{PDLL}[13, 14, 15]		12		13.5		15.5		17		17.5		18		20		24	ns
t_{EA}[13, 14, 15]		8		8.5		11		13		14		16		19		24	ns
t_{ER}[11, 13]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t_{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{IS}	2		2		2		2		2		2.5		3		4		ns
t_{IH}	2		2		2		2		2		2.5		3		4		ns
t_{ICO}[13, 14, 15]		11		11		11		12.5		12.5		16		19		24	ns
t_{ICOL}[13, 14, 15]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t_{CO}[14, 15]		4		4		4.5		6		6.5[16]		6.5[17]		8[18]		10	ns
t_{S}[13]	4		4		5		5		5.5[16]		6[17]		8[18]		10		ns
t_{H}	0		0		0		0		0		0		0		0		ns
t_{CO2}[13, 14, 15]		9.5		10		11		12		14		16		19		24	ns
t_{SCS}[13]	5		6		6.5		7		8[16]		10		12		15		ns
t_{SL}[13]	7.5		7.5		8.5		9		10		12		15		15		ns
t_{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t_{COPT}[13, 14, 15]		7		10		10		13		13		13		15		20	ns
t_{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{ISPT}[13]	0		0		0		0		0		0		0		0		ns
t_{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t_{CO2PT}[13, 14, 15]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t_{ICS}[13]	5		6		6		7		8[16]		10		12		15		ns
Operating Frequency Parameters																	
f_{MAX1}	200		167		154		143		125[16]		100		83		66		MHz
f_{MAX2}	200		200		200		167		154		153[17]		125[18]		100		MHz
f_{MAX3}	125		125		105		91		83		80[17]		62.5		50		MHz
f_{MAX4}	167		167		154		125		118		100		83		66		MHz
Reset/Preset Parameters																	
t_{RW}	8		8		8		8		10		12		15		20		ns
t_{RR}[13]	10		10		10		10		12		14		17		22		ns

Notes:

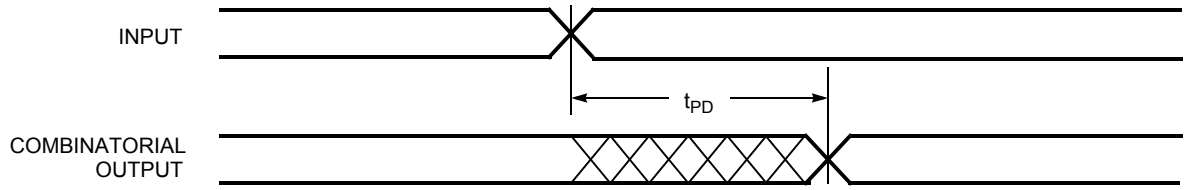
16. The following values correspond to the CY37512 and CY37384 devices: t_{CO} = 5 ns, t_S = 6.5 ns, t_{SCS} = 8.5 ns, t_{ICS} = 8.5 ns, f_{MAX1} = 118 MHz.
17. The following values correspond to the CY37192V and CY37256V devices: t_{CO} = 6 ns, t_S = 7 ns, f_{MAX2} = 143 MHz, f_{MAX3} = 77 MHz, and f_{MAX4} = 100 MHz; and for the CY37512 devices: t_S = 7 ns.
18. The following values correspond to the CY37512V and CY37384V devices: t_{CO} = 6.5 ns, t_S = 9.5 ns, and f_{MAX2} = 105 MHz.

Switching Characteristics Over the Operating Range (continued)[12]

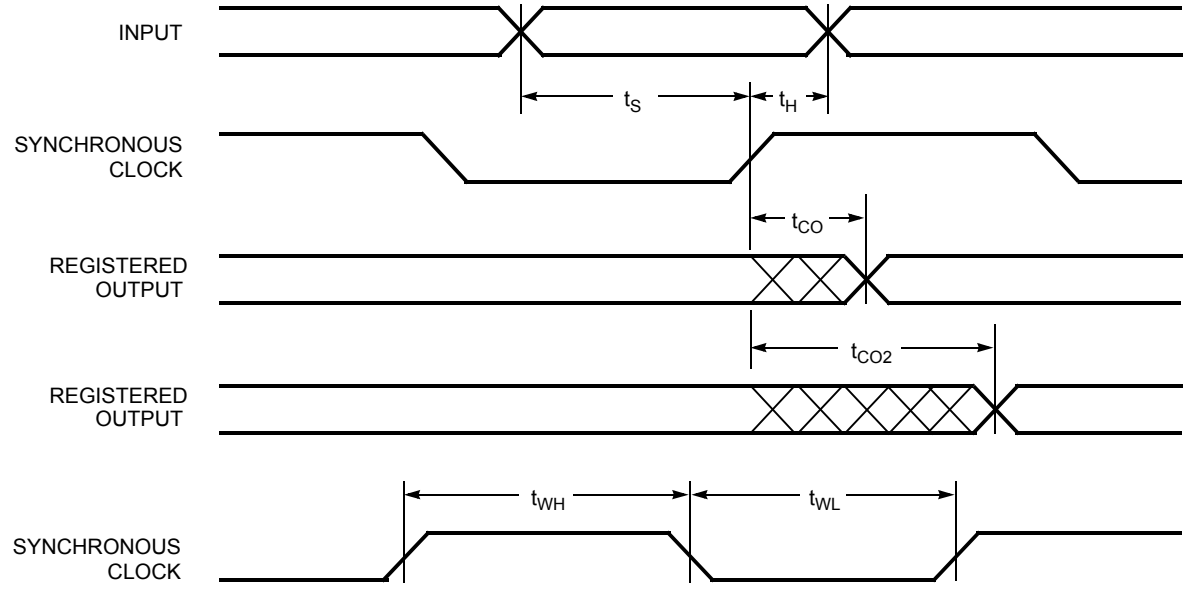
Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RO}[13, 14, 15]		12		13		13		14		15		18		21		26	ns
t_{PW}	8		8		8		8		10		12		15		20		ns
t_{PR}[13]	10		10		10		10		12		14		17		22		ns
t_{PO}[13, 14, 15]		12		13		13		14		15		18		21		26	ns
User Option Parameters																	
t_{LP}		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{SLEW}		3		3		3		3		3		3		3		3	ns
$t_{3.3IO}$[19]		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
JTAG Timing Parameters																	
$t_{S\ JTAG}$	0		0		0		0		0		0		0		0		ns
$t_{H\ JTAG}$	20		20		20		20		20		20		20		20		ns
$t_{CO\ JTAG}$		20		20		20		20		20		20		20		20	ns
f_{JTAG}		20		20		20		20		20		20		20		20	MHz

Switching Waveforms

Combinatorial Output



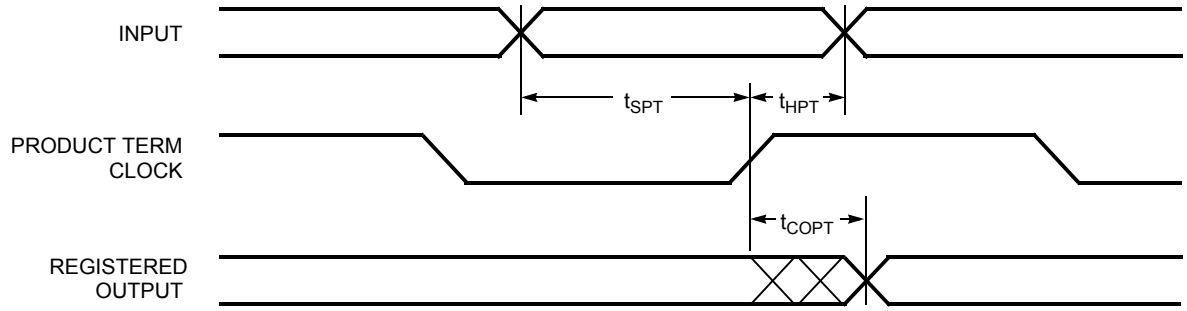
Registered Output with Synchronous Clocking



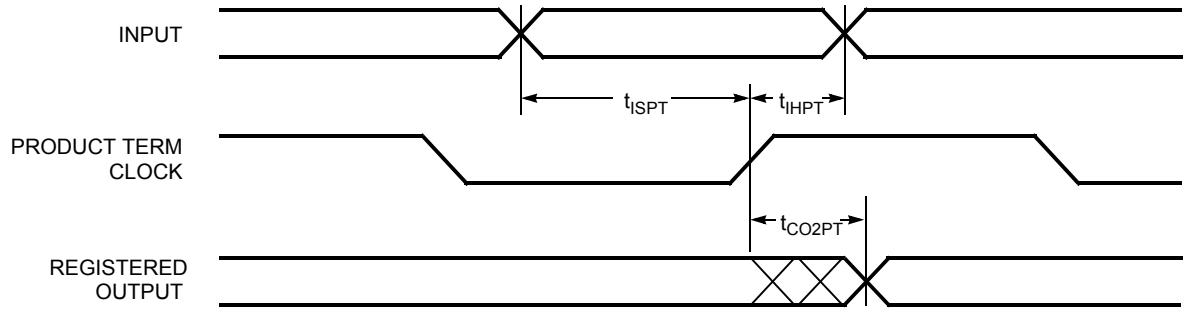
Note:
19. Only applicable to the 5V devices.

Switching Waveforms (continued)

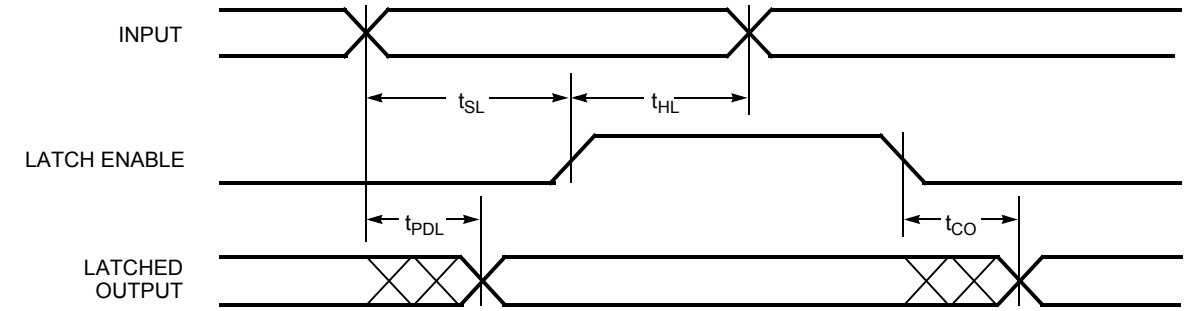
Registered Output with Product Term Clocking Input Going Through the Array



Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register

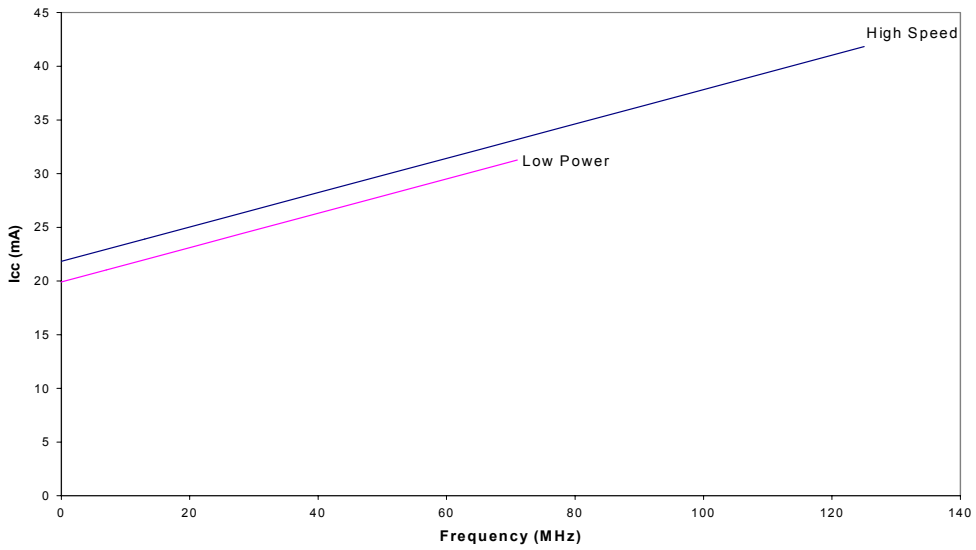


Latched Output



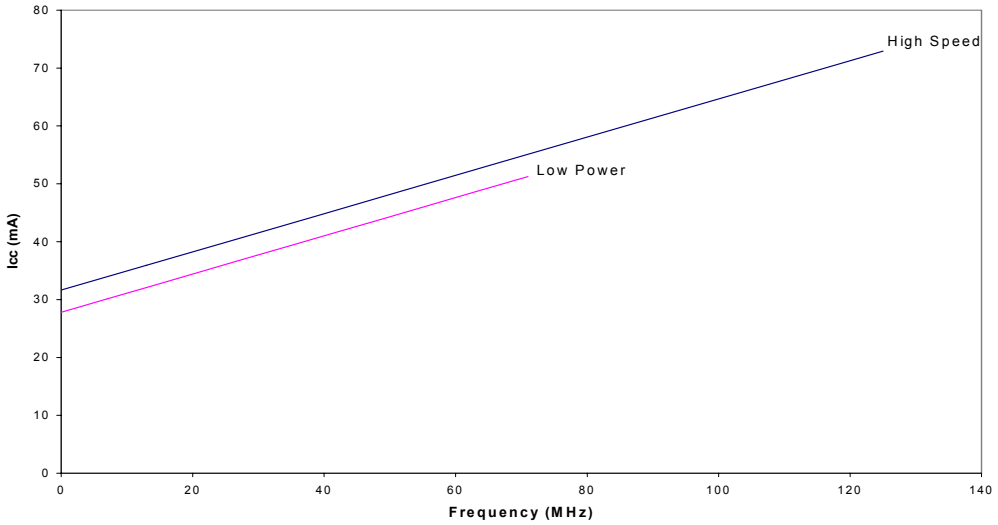
Typical 3.3V Power Consumption (continued)

CY37064V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

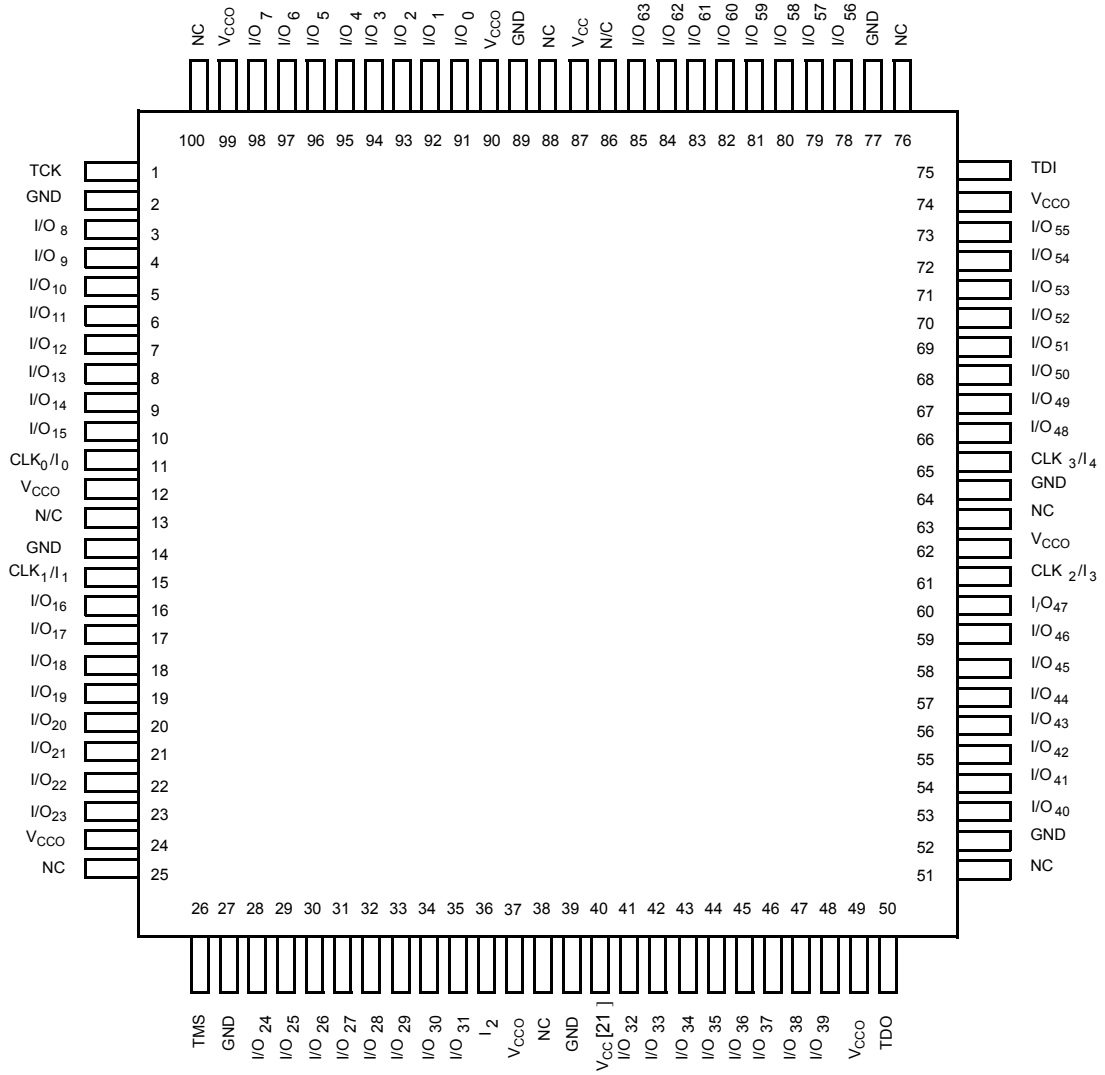
CY37128V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

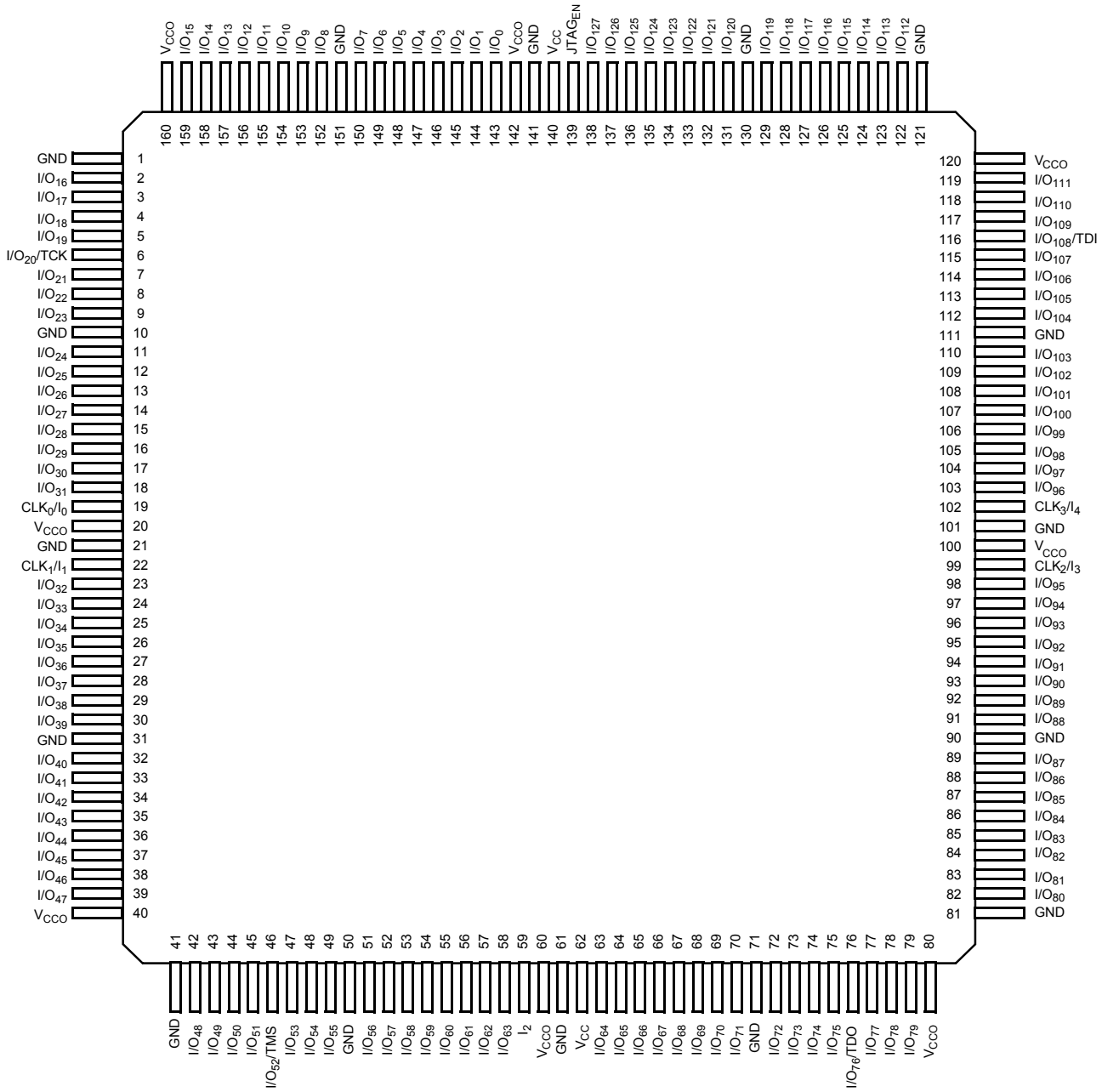
Pin Configurations[20] (continued)

100-lead TQFP (A100)
Top View



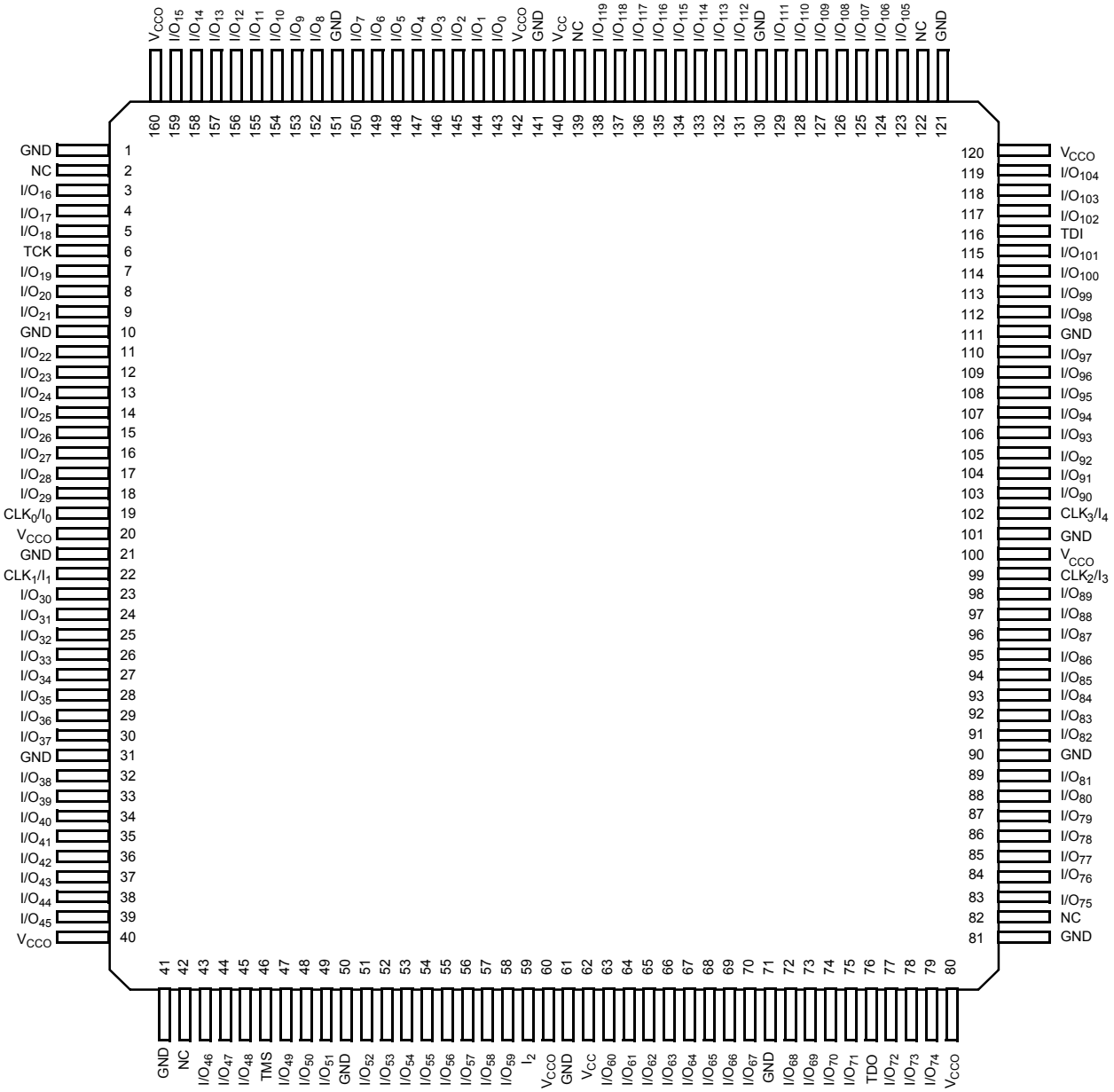
Pin Configurations[20] (continued)

160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View



Pin Configurations[20] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[20] (continued)

292-Ball PBGA (BG292)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O_{21}	NC	I/O_{16}	I/O_{12}	I/O_{9}	I/O_{7}	I/O_{4}	I/O_{0}	I/O_{190}	I/O_{189}	I/O_{186}	I/O_{182}	NC	I/O_{178}	I/O_{175}	NC	NC	I/O_{169}	I/O_{168}	A
B	I/O_{23}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{15}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{1}	I/O_{191}	I/O_{187}	I/O_{185}	I/O_{181}	NC	NC	I/O_{174}	I/O_{171}	I/O_{170}	NC	I/O_{166}	B
C	NC	NC	I/O_{22}	NC	I/O_{17}	I/O_{14}	I/O_{10}	I/O_{6}	I/O_{2}	NC	I/O_{188}	I/O_{184}	I/O_{180}	I/O_{179}	I/O_{176}	I/O_{173}	I/O_{172}	I/O_{167}	I/O_{165}	I/O_{162}	C
D	I/O_{24}	NC	NC	GND	NC	V_{CCO}	I/O_{13}	GND	I/O_{3}	NC	V_{CC}	I/O_{183}	GND	I/O_{177}	V_{CCO}	NC	GND	I/O_{164}	TDI	I/O_{160}	D
E	I/O_{27}	I/O_{26}	I/O_{25}	NC													I/O_{163}	I/O_{161}	I/O_{159}	I/O_{156}	E
F	I/O_{30}	TCK	I/O_{28}	V_{CCO}													V_{CCO}	I/O_{158}	NC	I/O_{154}	F
G	I/O_{33}	I/O_{32}	I/O_{31}	I/O_{29}													I/O_{157}	I/O_{155}	I/O_{153}	I/O_{152}	G
H	I/O_{35}	NC	I/O_{34}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{151}	I/O_{150}	I/O_{149}	H
J	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{36}				GND	GND	GND	GND	GND	GND				I/O_{148}	I/O_{147}	I/O_{146}	I/O_{145}	J
K	I/O_{42}	I/O_{40}	I/O_{41}	V_{CC}				GND	GND	GND	GND	GND	GND				I/O_{144}	CLK_3/I_4	NC	NC	K
L	I/O_{43}	I/O_{44}	I/O_{45}	I/O_{46}				GND	GND	GND	GND	GND	GND				V_{CC}	CLK_2/I_3	I/O_{143}	NC	L
M	I/O_{47}	CLK_0/I_0	CLK_1/I_1	I/O_{48}				GND	GND	GND	GND	GND	GND				I/O_{139}	I/O_{140}	I/O_{141}	I/O_{142}	M
N	I/O_{49}	I/O_{50}	I/O_{51}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{136}	I/O_{137}	I/O_{138}	N
P	I/O_{52}	I/O_{53}	I/O_{55}	I/O_{58}													I/O_{131}	I/O_{133}	I/O_{134}	I/O_{135}	P
R	I/O_{54}	I/O_{56}	I/O_{59}	V_{CCO}													V_{CCO}	I/O_{130}	NC	I/O_{132}	R
T	I/O_{57}	I/O_{60}	I/O_{62}	I/O_{65}													I/O_{124}	I/O_{127}	I/O_{128}	I/O_{129}	T
U	I/O_{61}	I/O_{63}	I/O_{66}	GND	I/O_{76}	V_{CCO}	I/O_{82}	GND	I/O_{91}	V_{CC}	I/O_{98}	I/O_{102}	GND	I/O_{112}	V_{CCO}	NC	GND	I/O_{123}	I/O_{122}	I/O_{126}	U
V	I/O_{64}	I/O_{67}	I/O_{69}	I/O_{75}	I/O_{78}	I/O_{81}	I/O_{85}	I/O_{88}	I/O_{92}	I_2	I/O_{97}	I/O_{101}	I/O_{105}	I/O_{109}	I/O_{113}	TDO	I/O_{114}	I/O_{117}	I/O_{121}	I/O_{125}	V
W	I/O_{68}	I/O_{70}	I/O_{72}	I/O_{74}	I/O_{79}	I/O_{83}	I/O_{86}	I/O_{89}	I/O_{93}	I/O_{95}	I/O_{96}	I/O_{100}	I/O_{104}	I/O_{107}	I/O_{110}	NC	NC	I/O_{115}	I/O_{118}	I/O_{120}	W
Y	I/O_{71}	I/O_{73}	I/O_{77}	TMS	I/O_{80}	I/O_{84}	I/O_{87}	I/O_{90}	I/O_{94}	NC	NC	I/O_{99}	I/O_{103}	I/O_{106}	I/O_{108}	I/O_{111}	NC	NC	I/O_{116}	I/O_{119}	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

3.3V Ordering Information (continued)

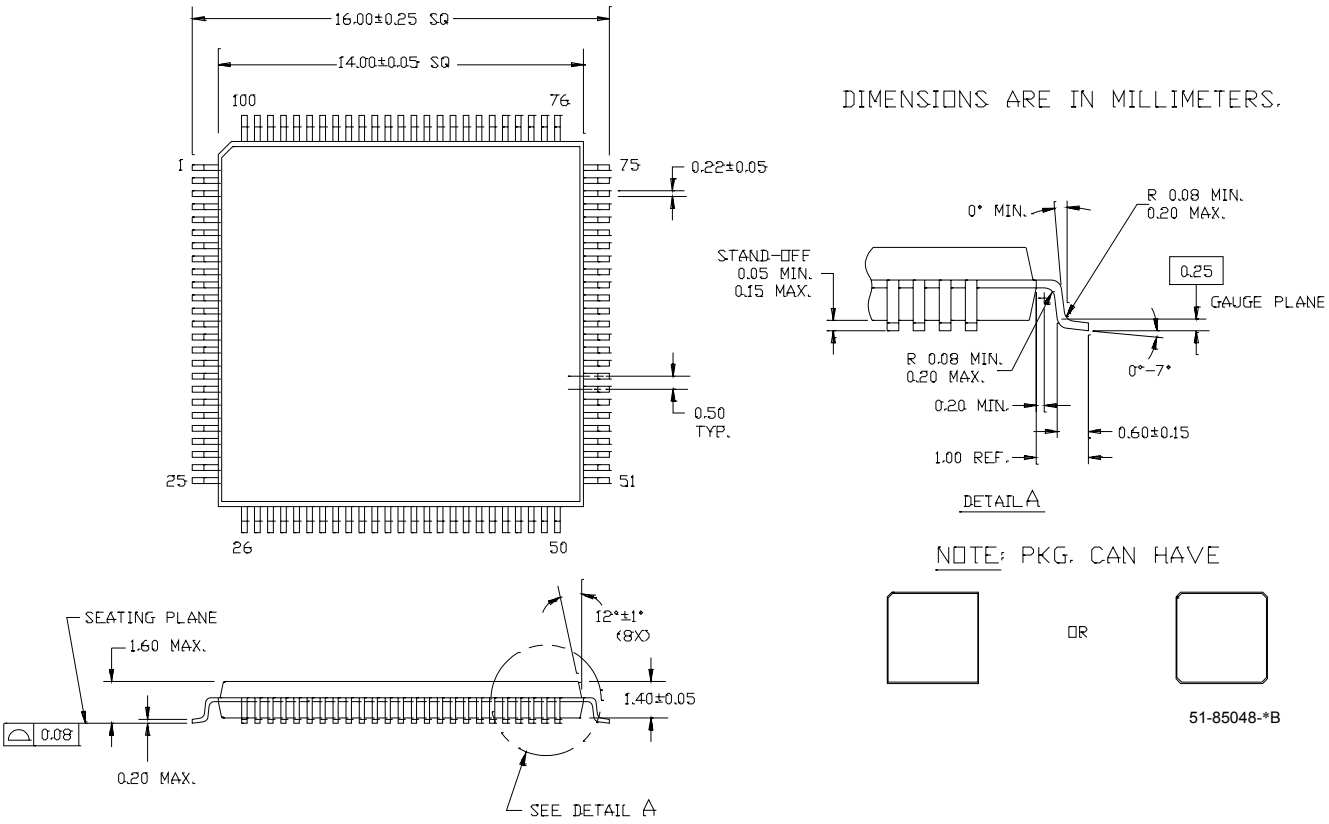
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	143	CY37064VP44-143AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-143AXC	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-143BAC	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-143AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-143AXC	A100	100-Lead Lead Free Thin Quad Flatpack	
		CY37064VP100-143BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
	100	CY37064VP44-100AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-100AXC	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-100BAC	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100AXC	A100	100-Lead Lead Free Thin Quad Flatpack	
		CY37064VP100-100BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37064VP44-100AI	A44	44-Lead Thin Quad Flatpack	Industrial
		CY37064VP44-100AXI	A44	44-Lead Lead Free Thin Quad Flatpack	
		CY37064VP48-100BAI	BA50	48-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100BBI	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37064VP100-100AI	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100AXI	A100	100-Lead Lead Free Thin Quad Flatpack	
		5962-9952001QYA	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
128	125	CY37128VP100-125AC	A100	100-Lead Thin Quad Flat Pack	Commercial
		CY37128VP100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-125BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-125AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37128VP160-125AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	83	CY37128VP100-83AC	A100	100-Lead Thin Quad Flat Pack	Commercial
		CY37128VP100-83AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83BBC	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-83AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-83AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83AI	A100	100-Lead Thin Quad Flat Pack	Industrial
		CY37128VP100-83AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37128VP100-83BBI	BB100	100-Ball Fine-Pitch Ball Grid Array	
		CY37128VP160-83AI	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP160-83AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
		5962-9952201QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	100	CY37192VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37192VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37192VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial

3.3V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

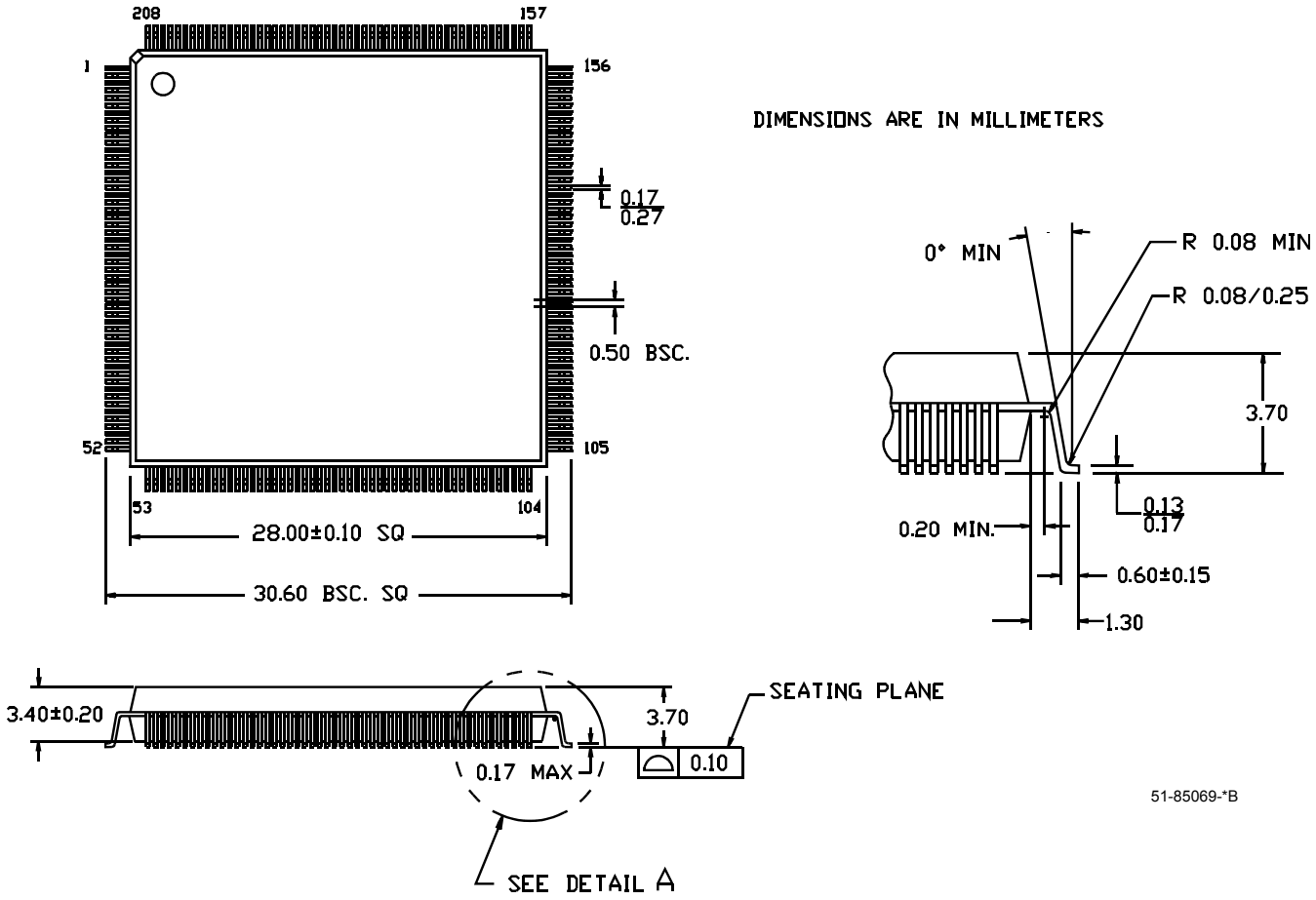
Package Diagrams (continued)

100-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (TQFP) A100



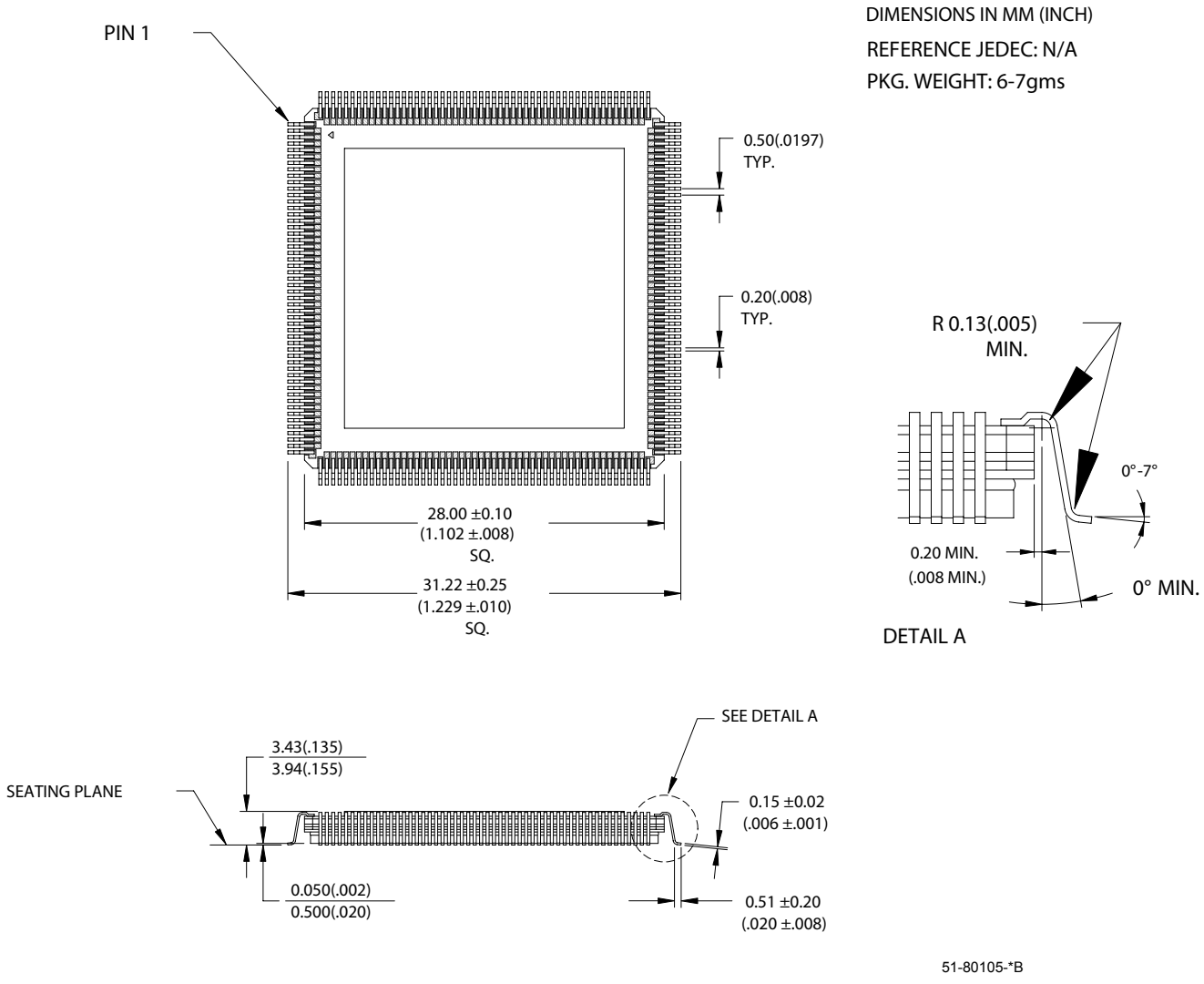
Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



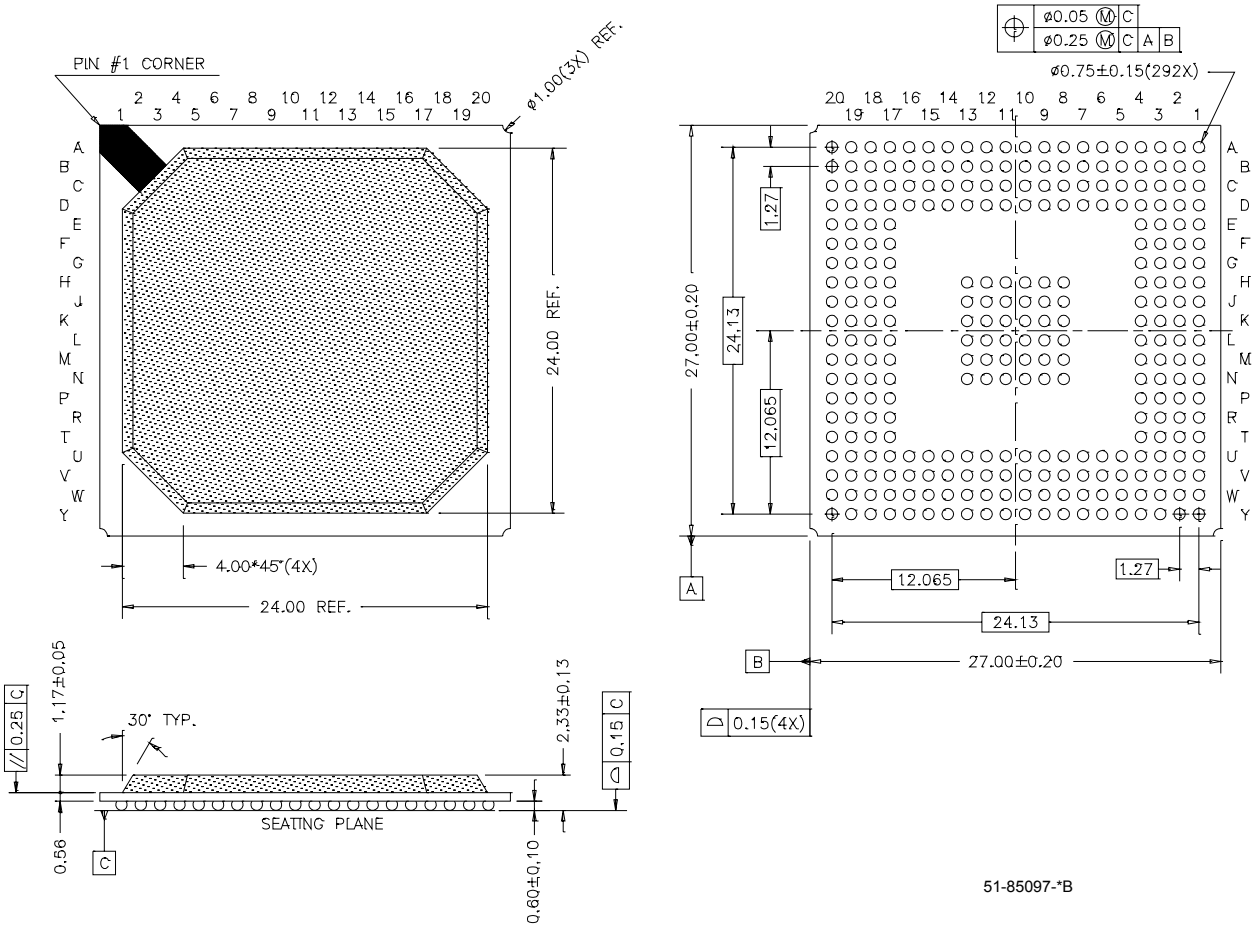
Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208



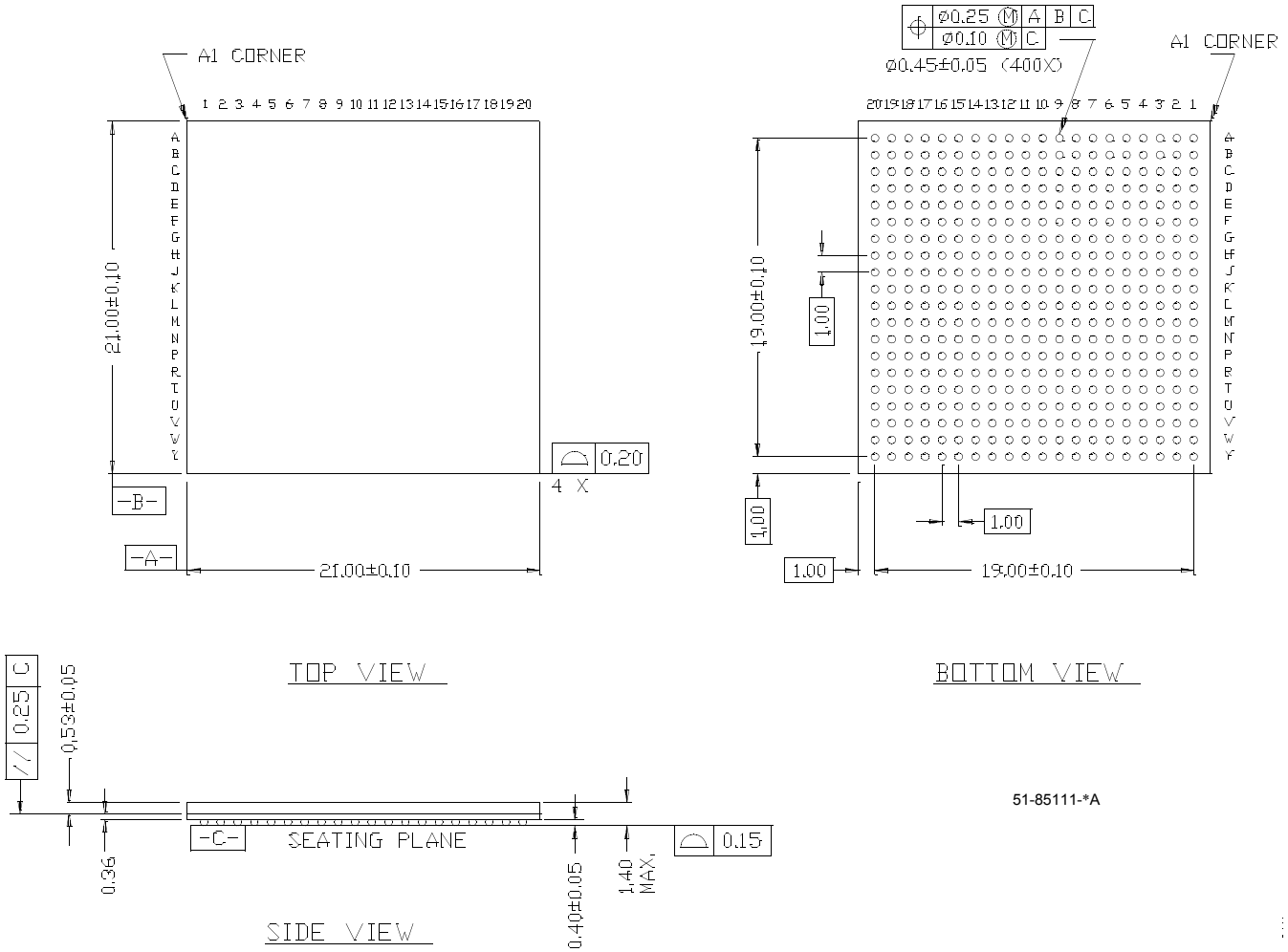
Package Diagrams (continued)

292-Ball Plastic Ball Grid Array PBGA (27 x 27 x 2.33 mm) BG292



Package Diagrams (continued)

400-Ball FBGA (21 x 21 x 1.4 mm) BB400



Addendum

3.3V Operating Range

(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.16V