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### Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In-System Reprogrammable™ (ISR™) CMOS |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | - |
| Number of Macrocells | 256 |
| Number of Gates | - |
| Number of I/O | 197 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 292-BGA |
| Supplier Device Package | 292-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy37256p256-154bgc |

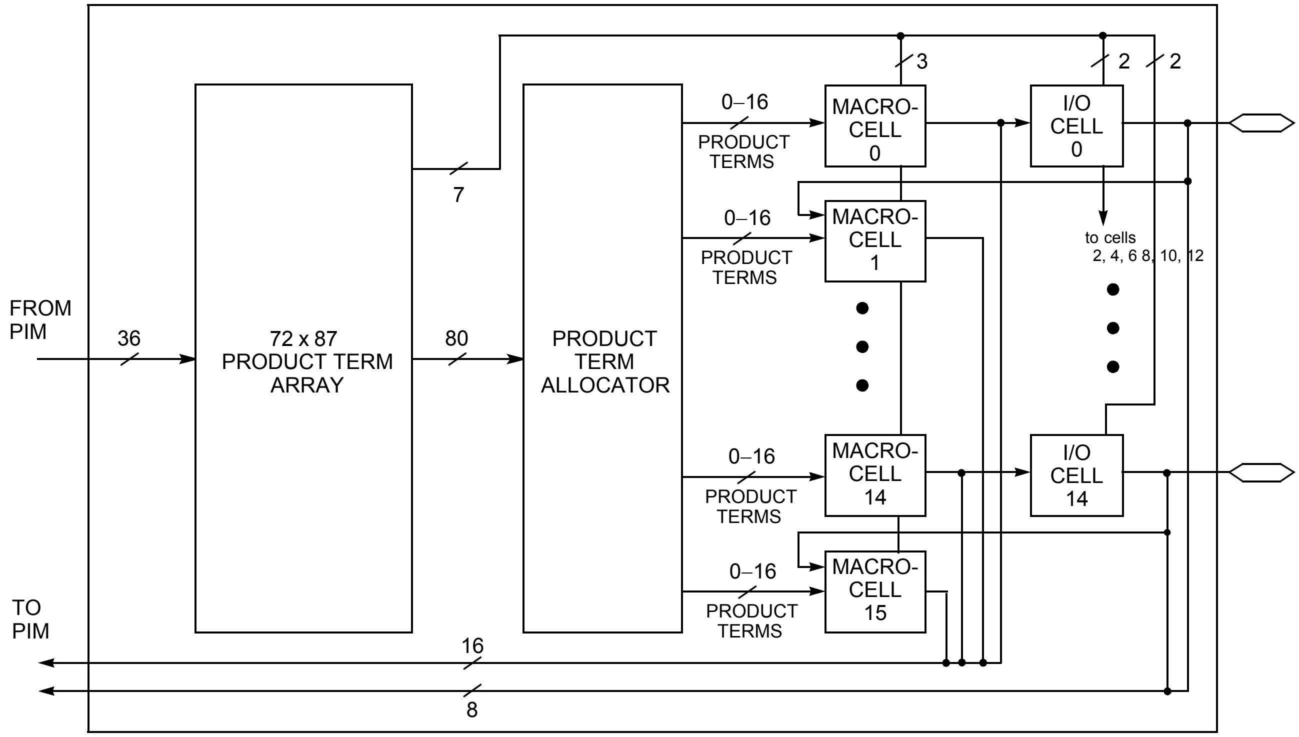



**Figure 1. Logic Block with 50% Buried Macrocells**

*Low-Power Option*

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

### Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

*Product Term Steering*

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

*Product Term Sharing*

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

### Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

*Buried Macrocell*

*Figure 2* displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

*I/O Macrocell*

*Figure 2* illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

*Bus Hold Capabilities on all I/Os*

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to $V_{CC}$ or GND. For more information, see the application note *Understanding Bus-Hold—A Feature of Cypress CPLDs*.

*Programmable Slew Rate Control*

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

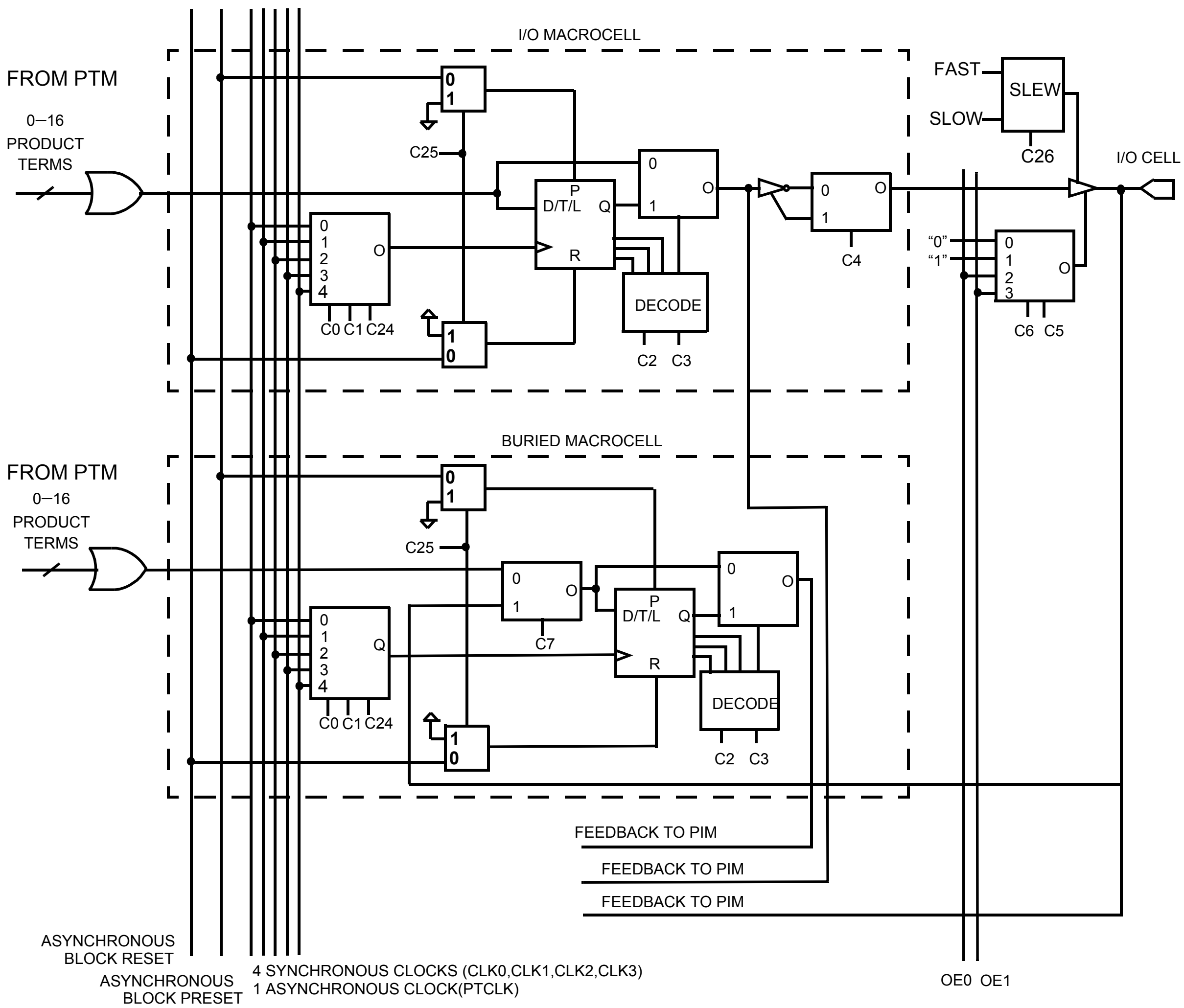



**Figure 2. I/O and Buried Macrocells**

## 5.0V Device Characteristics
## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ................................–65°C to +150°C

Ambient Temperature with
Power Applied...........................................–55°C to +125°C

Supply Voltage to Ground Potential ...............–0.5V to +7.0V

DC Voltage Applied to Outputs
in High-Z State...............................................–0.5V to +7.0V

DC Input Voltage ..........................................–0.5V to +7.0V

DC Program Voltage........................................... 4.5 to 5.5V

Current into Outputs .................................................. 16 mA

Static Discharge Voltage.......................................... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current.................................................... > 200 mA

## Operating Range[2]

| Range | Ambient Temperature[2] | Junction Temperature | Output Condition | $V_{CC}$ | $V_{CCO}$ |
|---|---|---|---|---|---|
| Commercial | 0°C to +70°C | 0°C to +90°C | 5V | 5V ± 0.25V | 5V ± 0.25V |
| | | | 3.3V | 5V ± 0.25V | 3.3V ± 0.3V |
| Industrial | –40°C to +85°C | –40°C to +105°C | 5V | 5V ± 0.5V | 5V ± 0.5V |
| | | | 3.3V | 5V ± 0.5V | 3.3V ± 0.3V |
| Military[3] | –55°C to +125°C | –55°C to +130°C | 5V | 5V ± 0.5V | 5V ± 0.5V |
| | | | 3.3V | 5V ± 0.5V | 3.3V ± 0.3V |

## 5.0V Device Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | $I_{OH}$ = –3.2 mA (Com'l/Ind)[4] | 2.4 | | | V |
| | | | $I_{OH}$ = –2.0 mA (Mil)[4] | 2.4 | | | V |
| $V_{OHZ}$ | Output HIGH Voltage with Output Disabled[5] | $V_{CC}$ = Max. | $I_{OH}$ = 0 μA (Com'l)[6] | | | 4.2 | V |
| | | | $I_{OH}$ = 0 μA (Ind/Mil)[6] | | | 4.5 | V |
| | | | $I_{OH}$ = –100 μA (Com'l)[6] | | | 3.6 | V |
| | | | $I_{OH}$ = –150 μA (Ind/Mil)[6] | | | 3.6 | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. | $I_{OL}$ = 16 mA (Com'l/Ind)[4] | | | 0.5 | V |
| | | | $I_{OL}$ = 12 mA (Mil)[4] | | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs[7] | | 2.0 | | $V_{CCmax}$ | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs[7] | | –0.5 | | 0.8 | V |
| $I_{IX}$ | Input Load Current | $V_I$ = GND OR $V_{CC}$, Bus-Hold Disabled | | –10 | | 10 | μA |
| $I_{OZ}$ | Output Leakage Current | $V_O$ = GND or $V_{CC}$, Output Disabled, Bus-Hold Disabled | | –50 | | 50 | μA |
| $I_{OS}$ | Output Short Circuit Current[5, 8] | $V_{CC}$ = Max., $V_{OUT}$ = 0.5V | | –30 | | –160 | mA |
| $I_{BHL}$ | Input Bus-Hold LOW Sustaining Current | $V_{CC}$ = Min., $V_{IL}$ = 0.8V | | +75 | | | μA |
| $I_{BHH}$ | Input Bus-Hold HIGH Sustaining Current | $V_{CC}$ = Min., $V_{IH}$ = 2.0V | | –75 | | | μA |
| $I_{BHLO}$ | Input Bus-Hold LOW Overdrive Current | $V_{CC}$ = Max. | | | | +500 | μA |
| $I_{BHHO}$ | Input Bus-Hold HIGH Overdrive Current | $V_{CC}$ = Max. | | | | –500 | μA |

**Notes:**

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled "An Introduction to In System Reprogramming with the Ultra37000."
3. $T_A$ is the "Instant On" case temperature.
4. $I_{OH}$ = –2 mA, $I_{OL}$ = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. $V_{OUT}$ = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

## Inductance[5]

| Parameter | Description | Test Conditions | 44-Lead TQFP | 44-Lead PLCC | 44-Lead CLCC | 84-Lead PLCC | 84-Lead CLCC | 100-Lead TQFP | 160-Lead TQFP | 208-Lead PQFP | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| L | Maximum Pin Inductance | $V_{IN}$ = 3.3V at f = 1 MHz | 2 | 5 | 2 | 8 | 5 | 8 | 9 | 11 | nH |

## Capacitance[5]

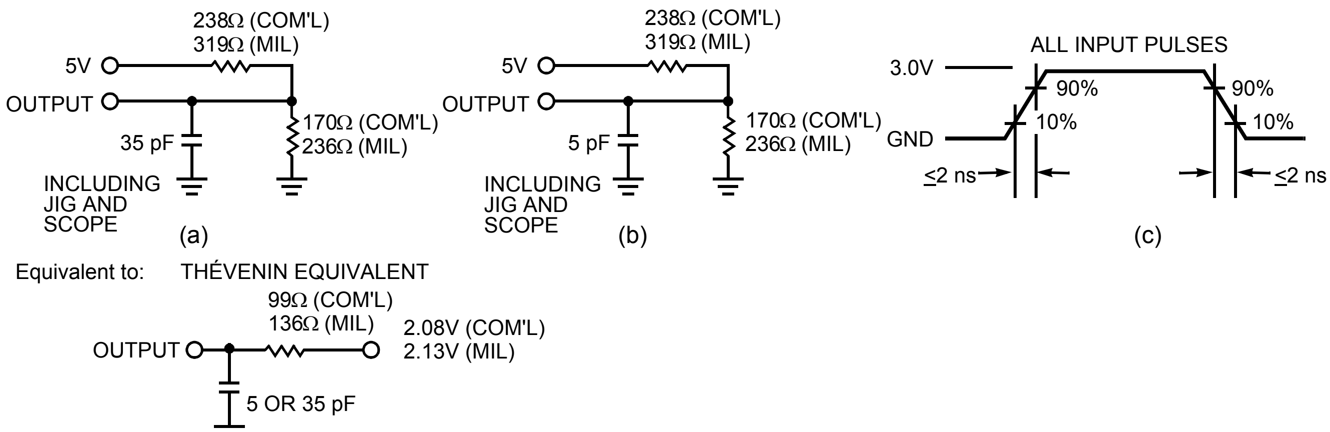
| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance | $V_{IN}$ = 3.3V at f = 1 MHz at $T_A$ = 25°C | 8 | pF |
| $C_{CLK}$ | Clock Signal Capacitance | $V_{IN}$ = 3.3V at f = 1 MHz at $T_A$ = 25°C | 12 | pF |
| $C_{DP}$ | Dual Functional Pins[9] | $V_{IN}$ = 3.3V at f = 1 MHz at $T_A$ = 25°C | 16 | pF |

## Endurance Characteristics[5]

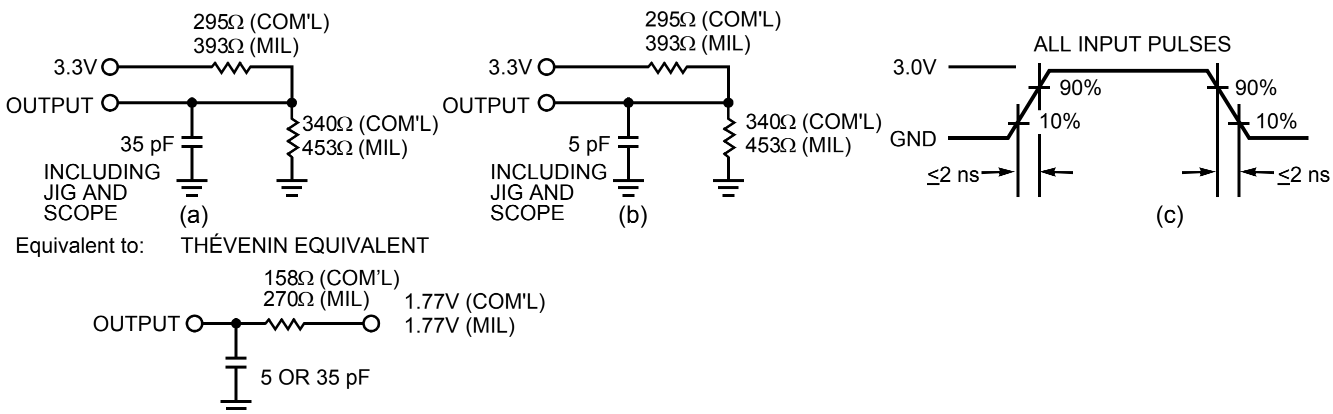
| Parameter | Description | Test Conditions | Min. | Typ. | Unit |
|---|---|---|---|---|---|
| N | Minimum Reprogramming Cycles | Normal Programming Conditions[2] | 1,000 | 10,000 | Cycles |

## AC Characteristics

### 5.0V AC Test Loads and Waveforms




### 3.3V AC Test Loads and Waveforms



## Switching Characteristics Over the Operating Range (continued)[12]

| Parameter | Description | Unit |
|---|---|---|
| **Product Term Clocking Parameters** | | |
| $t_{COPT}$[13, 14, 15] | Product Term Clock or Latch Enable (PTCLK) to Output | ns |
| $t_{SPT}$ | Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK) | ns |
| $t_{HPT}$ | Register or Latch Data Hold Time | ns |
| $t_{ISPT}$[13] | Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK) | ns |
| $t_{IHPT}$ | Buried Register Used as an Input Register or Latch Data Hold Time | ns |
| $t_{CO2PT}$[13, 14, 15] | Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array) | ns |
| **Pipelined Mode Parameters** | | |
| $t_{ICS}$[13] | Input Register Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) to Output Register Synchronous Clock ($CLK_0$, $CLK_1$, $CLK_2$, or $CLK_3$) | ns |
| **Operating Frequency Parameters** | | |
| $f_{MAX1}$ | Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5] | MHz |
| $f_{MAX2}$ | Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5] | MHz |
| $f_{MAX3}$ | Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)[5] | MHz |
| $f_{MAX4}$ | Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[5] | MHz |
| **Reset/Preset Parameters** | | |
| $t_{RW}$ | Asynchronous Reset Width[5] | ns |
| $t_{RR}$[13] | Asynchronous Reset Recovery Time[5] | ns |
| $t_{RO}$[13, 14, 15] | Asynchronous Reset to Output | ns |
| $t_{PW}$ | Asynchronous Preset Width[5] | ns |
| $t_{PR}$[13] | Asynchronous Preset Recovery Time[5] | ns |
| $t_{PO}$[13, 14, 15] | Asynchronous Preset to Output | ns |
| **User Option Parameters** | | |
| $t_{LP}$ | Low Power Adder | ns |
| $t_{SLEW}$ | Slow Output Slew Rate Adder | ns |
| $t_{3.3IO}$ | 3.3V I/O Mode Timing Adder[5] | ns |
| **JTAG Timing Parameters** | | |
| $t_{S\ JTAG}$ | Set-up Time from TDI and TMS to TCK[5] | ns |
| $t_{H\ JTAG}$ | Hold Time on TDI and TMS[5] | ns |
| $t_{CO\ JTAG}$ | Falling Edge of TCK to TDO[5] | ns |
| $f_{JTAG}$ | Maximum JTAG Tap Controller Frequency[5] | ns |

## Switching Characteristics Over the Operating Range [12]

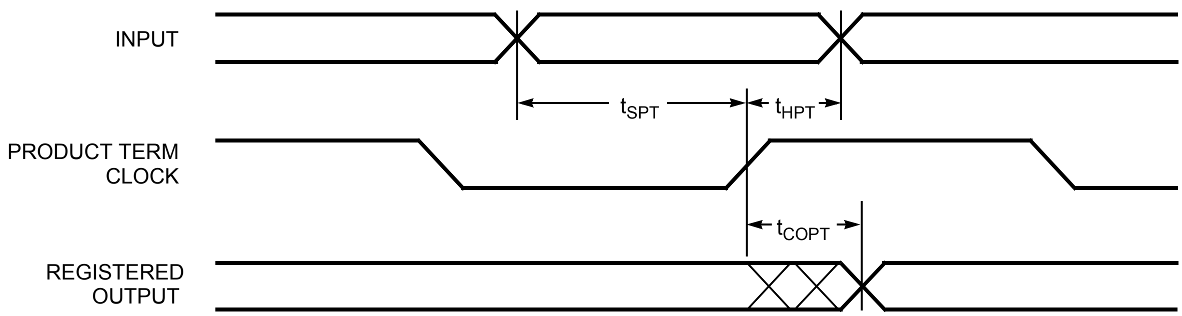
| Parameter | 200 MHz Min. | 200 MHz Max. | 167 MHz Min. | 167 MHz Max. | 154 MHz Min. | 154 MHz Max. | 143 MHz Min. | 143 MHz Max. | 125 MHz Min. | 125 MHz Max. | 100 MHz Min. | 100 MHz Max. | 83 MHz Min. | 83 MHz Max. | 66 MHz Min. | 66 MHz Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Combinatorial Mode Parameters** | | | | | | | | | | | | | | | | | |
| $t_{PD}$ [13, 14, 15] | | 6 | | 6.5 | | 7.5 | | 8.5 | | 10 | | 12 | | 15 | | 20 | ns |
| $t_{PDL}$ [13, 14, 15] | | 11 | | 12.5 | | 14.5 | | 16 | | 16.5 | | 17 | | 19 | | 22 | ns |
| $t_{PDLL}$ [13, 14, 15] | | 12 | | 13.5 | | 15.5 | | 17 | | 17.5 | | 18 | | 20 | | 24 | ns |
| $t_{EA}$ [13, 14, 15] | | 8 | | 8.5 | | 11 | | 13 | | 14 | | 16 | | 19 | | 24 | ns |
| $t_{ER}$ [11, 13] | | 8 | | 8.5 | | 11 | | 13 | | 14 | | 16 | | 19 | | 24 | ns |
| **Input Register Parameters** | | | | | | | | | | | | | | | | | |
| $t_{WL}$ | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 3 | | 3 | | 4 | | 5 | | ns |
| $t_{WH}$ | 2.5 | | 2.5 | | 2.5 | | 2.5 | | 3 | | 3 | | 4 | | 5 | | ns |
| $t_{IS}$ | 2 | | 2 | | 2 | | 2 | | 2 | | 2.5 | | 3 | | 4 | | ns |
| $t_{IH}$ | 2 | | 2 | | 2 | | 2 | | 2 | | 2.5 | | 3 | | 4 | | ns |
| $t_{ICO}$ [13, 14, 15] | | 11 | | 11 | | 11 | | 12.5 | | 12.5 | | 16 | | 19 | | 24 | ns |
| $t_{ICOL}$ [13, 14, 15] | | 12 | | 12 | | 12 | | 14 | | 16 | | 18 | | 21 | | 26 | ns |
| **Synchronous Clocking Parameters** | | | | | | | | | | | | | | | | | |
| $t_{CO}$ [14, 15] | | 4 | | 4 | | 4.5 | | 6 | | 6.5[16] | | 6.5[17] | | 8[18] | | 10 | ns |
| $t_{S}$ [13] | 4 | | 4 | | 5 | | 5 | | 5.5[16] | | 6[17] | | 8[18] | | 10 | | ns |
| $t_{H}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{CO2}$ [13, 14, 15] | | 9.5 | | 10 | | 11 | | 12 | | 14 | | 16 | | 19 | | 24 | ns |
| $t_{SCS}$ [13] | 5 | | 6 | | 6.5 | | 7 | | 8[16] | | 10 | | 12 | | 15 | | ns |
| $t_{SL}$ [13] | 7.5 | | 7.5 | | 8.5 | | 9 | | 10 | | 12 | | 15 | | 15 | | ns |
| $t_{HL}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| **Product Term Clocking Parameters** | | | | | | | | | | | | | | | | | |
| $t_{COPT}$ [13, 14, 15] | | 7 | | 10 | | 10 | | 13 | | 13 | | 13 | | 15 | | 20 | ns |
| $t_{SPT}$ | 2.5 | | 2.5 | | 2.5 | | 3 | | 5 | | 5.5 | | 6 | | 7 | | ns |
| $t_{HPT}$ | 2.5 | | 2.5 | | 2.5 | | 3 | | 5 | | 5.5 | | 6 | | 7 | | ns |
| $t_{ISPT}$ [13] | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{IHPT}$ | 6 | | 6.5 | | 6.5 | | 7.5 | | 9 | | 11 | | 14 | | 19 | | ns |
| $t_{CO2PT}$ [13, 14, 15] | | 12 | | 14 | | 15 | | 19 | | 19 | | 21 | | 24 | | 30 | ns |
| **Pipelined Mode Parameters** | | | | | | | | | | | | | | | | | |
| $t_{ICS}$ [13] | 5 | | 6 | | 6 | | 7 | | 8[16] | | 10 | | 12 | | 15 | | ns |
| **Operating Frequency Parameters** | | | | | | | | | | | | | | | | | |
| $f_{MAX1}$ | 200 | | 167 | | 154 | | 143 | | 125[16] | | 100 | | 83 | | 66 | | MHz |
| $f_{MAX2}$ | 200 | | 200 | | 200 | | 167 | | 154 | | 153[17] | | 125[18] | | 100 | | MHz |
| $f_{MAX3}$ | 125 | | 125 | | 105 | | 91 | | 83 | | 80[17] | | 62.5 | | 50 | | MHz |
| $f_{MAX4}$ | 167 | | 167 | | 154 | | 125 | | 118 | | 100 | | 83 | | 66 | | MHz |
| **Reset/Preset Parameters** | | | | | | | | | | | | | | | | | |
| $t_{RW}$ | 8 | | 8 | | 8 | | 8 | | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{RR}$ [13] | 10 | | 10 | | 10 | | 10 | | 12 | | 14 | | 17 | | 22 | | ns |

**Notes:**

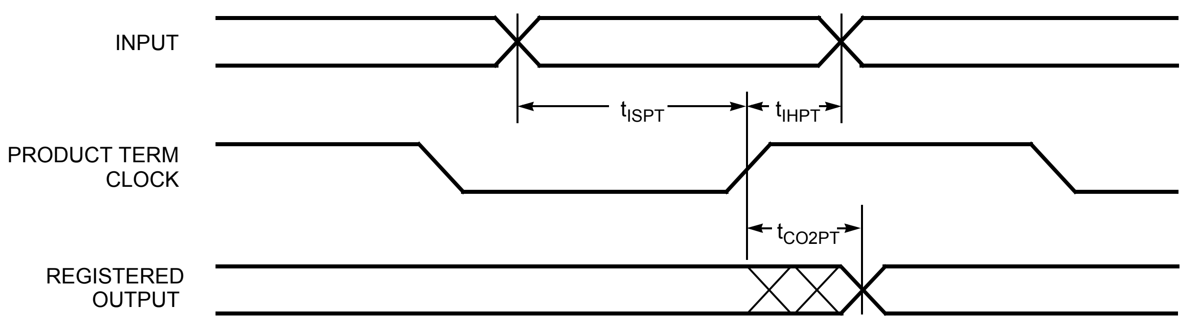
16. The following values correspond to the CY37512 and CY37384 devices: $t_{CO}$ = 5 ns, $t_S$ = 6.5 ns, $t_{SCS}$ = 8.5 ns, $t_{ICS}$ = 8.5 ns, $f_{MAX1}$ = 118 MHz.
17. The following values correspond to the CY37192V and CY37256V devices: $t_{CO}$ = 6 ns, $t_S$ = 7 ns, $f_{MAX2}$ = 143 MHz, $f_{MAX3}$ = 77 MHz, and $f_{MAX4}$ = 100 MHz; and for the CY37512 devices: $t_S$ = 7 ns.
18. The following values correspond to the CY37512V and CY37384V devices: $t_{CO}$ = 6.5 ns, $t_S$ = 9.5 ns, and $f_{MAX2}$ = 105 MHz.

## Switching Waveforms (continued)

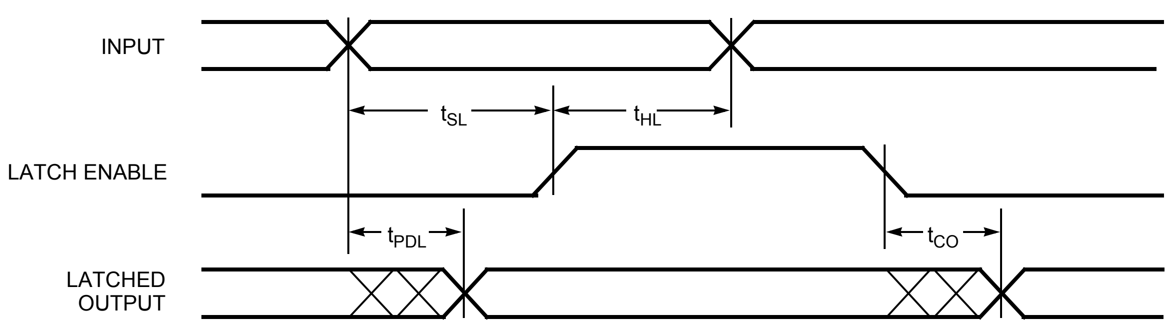
**Registered Output with Product Term Clocking Input Going Through the Array**




**Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register**

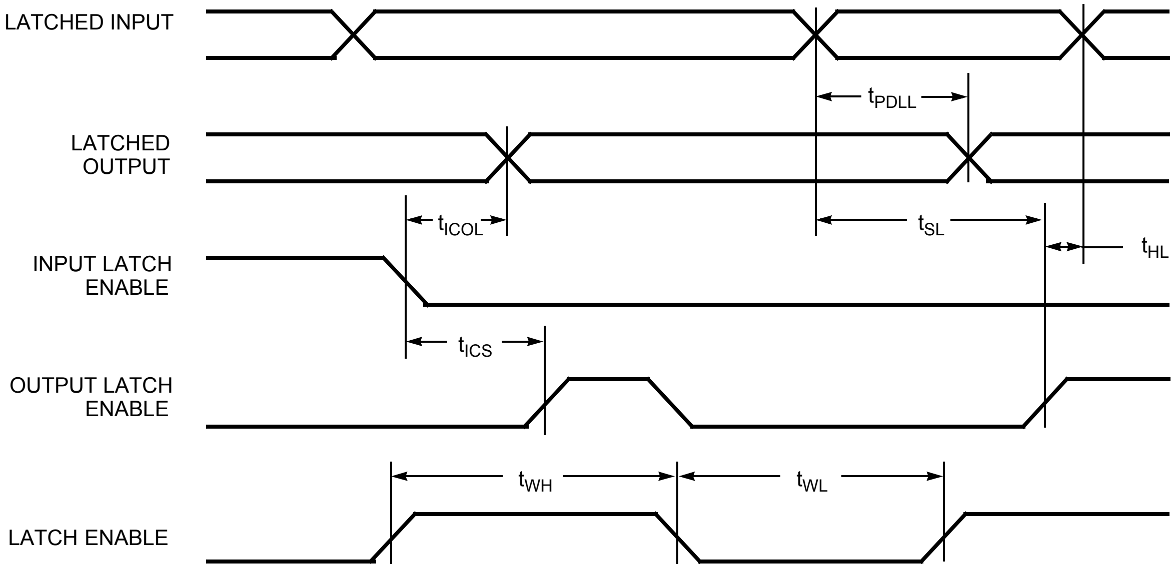



**Latched Output**

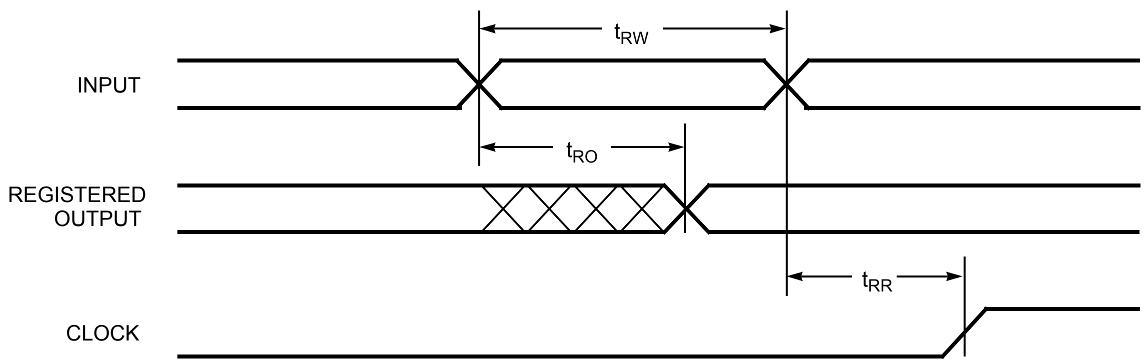


## Switching Waveforms (continued)

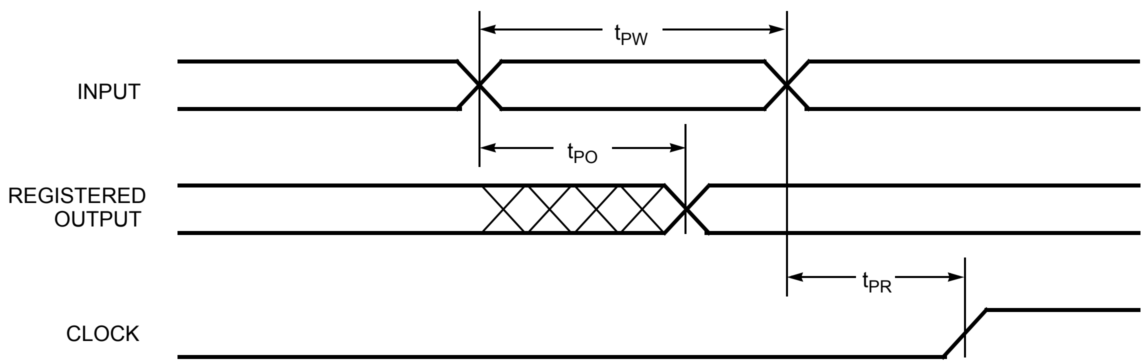
### Latched Input and Output



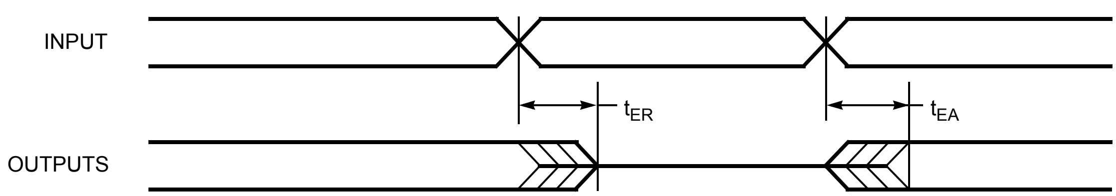

### Asynchronous Reset




### Asynchronous Preset

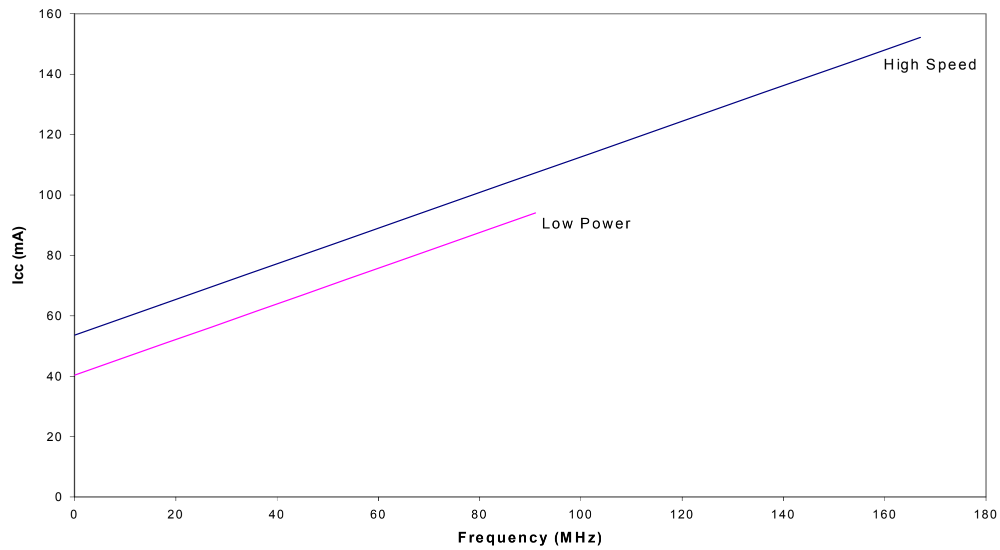



### Output Enable/Disable



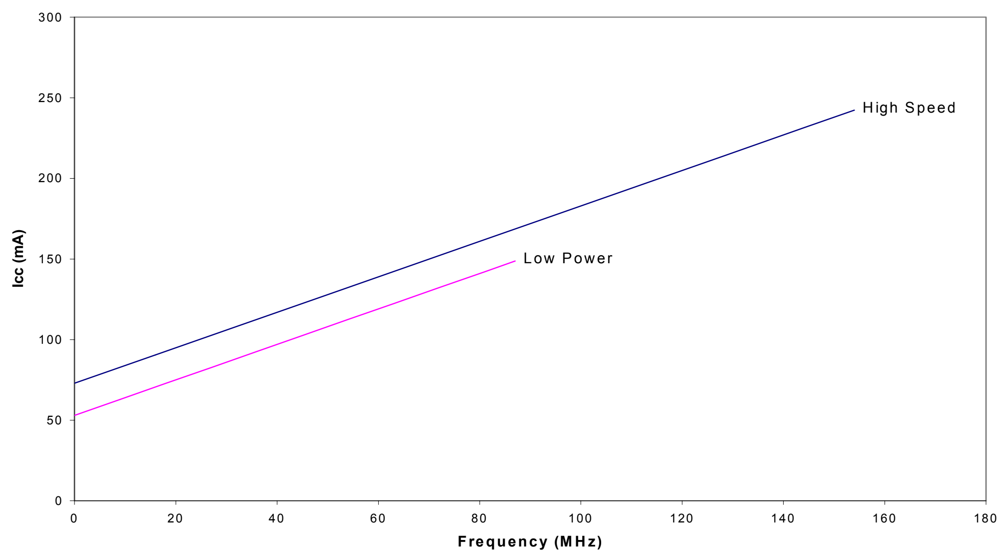
**Typical 5.0V Power Consumption** (continued)

**CY37128**




The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
$V_{CC}$ = 5.0V, $T_A$ = Room Temperature

**CY37192**

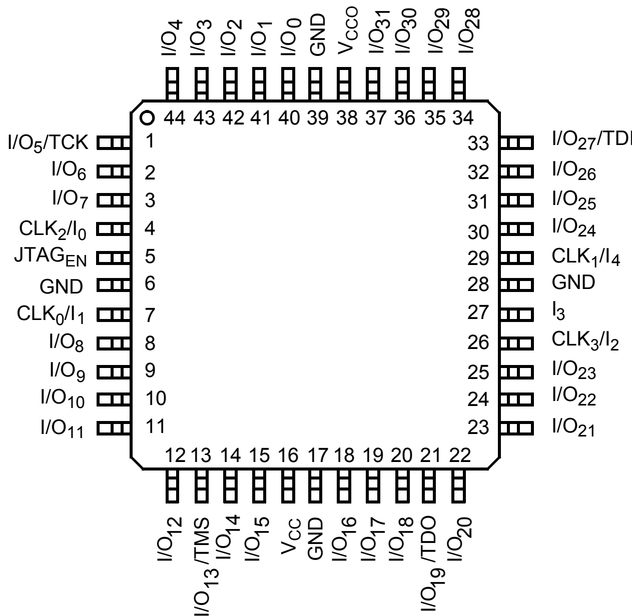



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
$V_{CC}$ = 5.0V, $T_A$ = Room Temperature

## Pin Configurations[20]

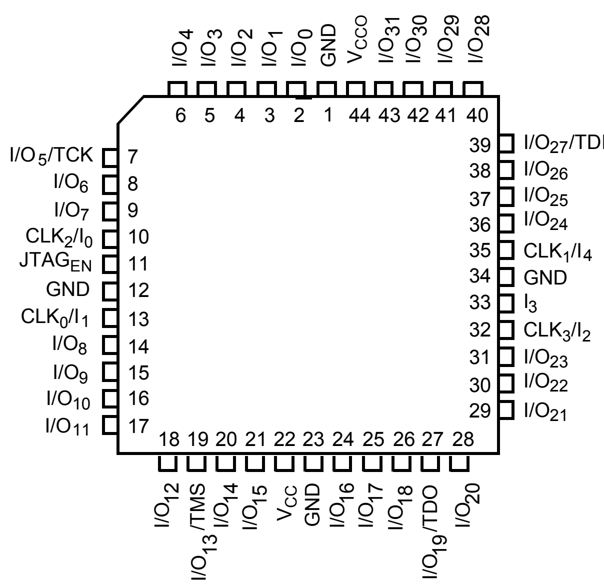
**44-pin TQFP (A44)**

**Top View**



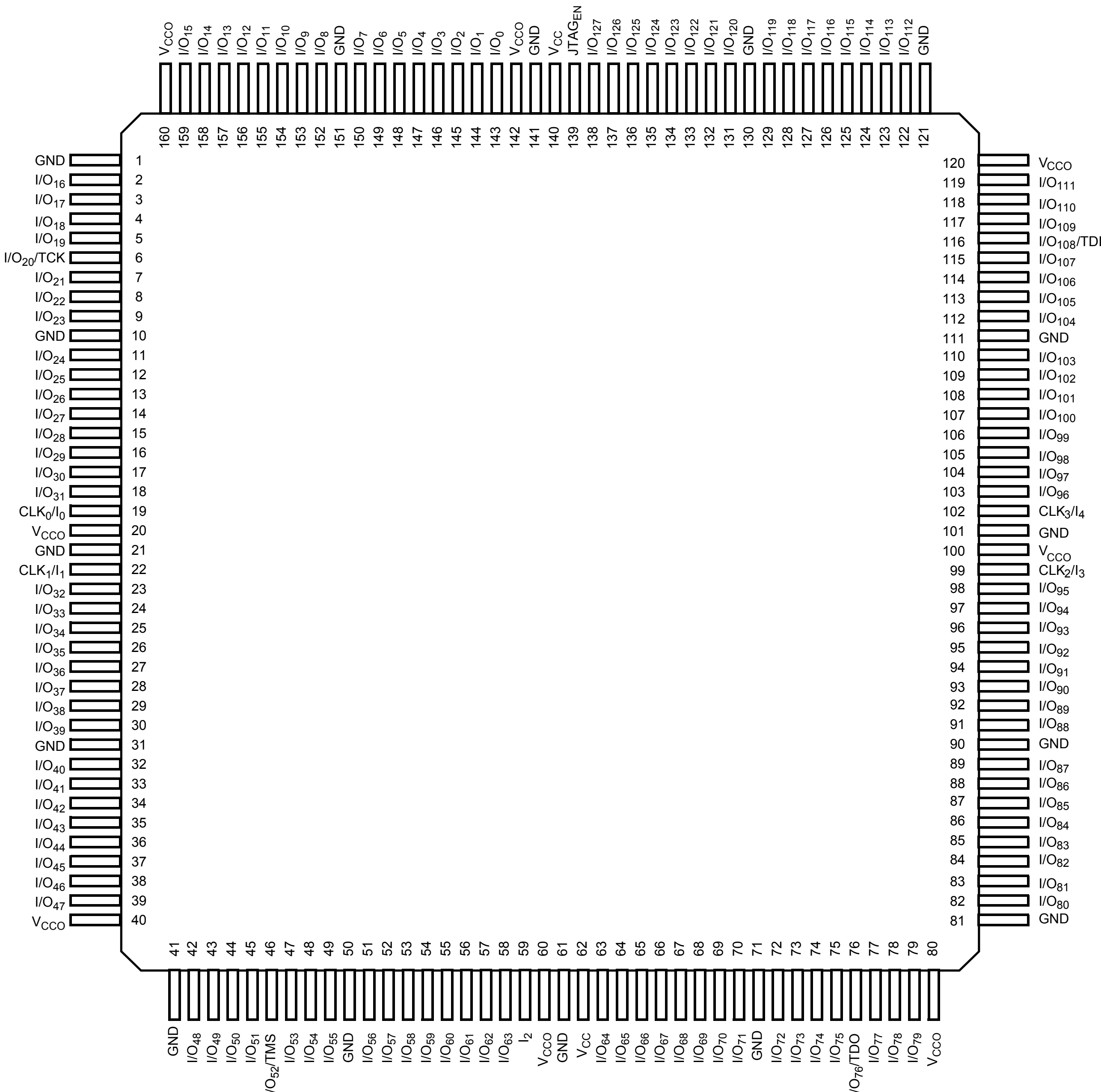

**44-pin PLCC (J67) / CLCC (Y67)**

**Top View**



## Pin Configurations[20] (continued)

**160-Lead TQFP (A160) / CQFP (U162)**
**for CY37128(V) and CY37256(V)**
**Top View**



## Pin Configurations[20] (continued)

### 256-Ball Fine-Pitch BGA (BB256)
### Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | GND | I/O$_{26}$ | I/O$_{24}$ | I/O$_{20}$ | $V_{CC}$ | I/O$_{11}$ | GND | GND | I/O$_{186}$ | $V_{CC}$ | I/O$_{177}$ | I/O$_{172}$ | I/O$_{167}$ | GND | GND |
| B | GND | I/O$_{27}$ | I/O$_{25}$ | I/O$_{23}$ | I/O$_{19}$ | I/O$_{15}$ | I/O$_{10}$ | GND | GND | I/O$_{185}$ | I/O$_{181}$ | I/O$_{176}$ | I/O$_{171}$ | I/O$_{166}$ | I/O$_{165}$ | GND |
| C | I/O$_{29}$ | I/O$_{28}$ | NC | I/O$_{22}$ | I/O$_{18}$ | I/O$_{14}$ | I/O$_{9}$ | I/O$_{4}$ | I/O$_{191}$ | I/O$_{184}$ | I/O$_{180}$ | I/O$_{175}$ | I/O$_{170}$ | NC | I/O$_{163}$ | I/O$_{164}$ |
| D | I/O$_{32}$ | I/O$_{31}$ | I/O$_{30}$ | NC | I/O$_{17}$ | I/O$_{13}$ | I/O$_{8}$ | I/O$_{3}$ | I/O$_{190}$ | I/O$_{183}$ | I/O$_{179}$ | I/O$_{174}$ | I/O$_{169}$ | I/O$_{160}$ | I/O$_{161}$ | I/O$_{162}$ |
| E | I/O$_{35}$ | I/O$_{34}$ | I/O$_{33}$ | I/O$_{21}$ | I/O$_{16}$ | I/O$_{12}$ | I/O$_{7}$ | I/O$_{2}$ | I/O$_{189}$ | $V_{CC}$ | I/O$_{178}$ | I/O$_{173}$ | I/O$_{168}$ | I/O$_{157}$ | I/O$_{158}$ | I/O$_{159}$ |
| F | $V_{CC}$ | I/O$_{38}$ | I/O$_{37}$ | I/O$_{36}$ | TCK | $V_{CC}$ | I/O$_{6}$ | I/O$_{1}$ | I/O$_{188}$ | I/O$_{182}$ | $V_{CC}$ | TDI | I/O$_{154}$ | I/O$_{155}$ | I/O$_{156}$ | $V_{CC}$ |
| G | I/O$_{43}$ | I/O$_{42}$ | I/O$_{41}$ | I/O$_{40}$ | $V_{CC}$ | I/O$_{39}$ | I/O$_{5}$ | I/O$_{0}$ | I/O$_{187}$ | I/O$_{148}$ | I/O$_{149}$ | CLK$_{3}$ /I$_{4}$ | I/O$_{150}$ | I/O$_{151}$ | I/O$_{152}$ | I/O$_{153}$ |
| H | GND | GND | I/O$_{47}$ | I/O$_{46}$ | CLK$_{0}$ /I$_{0}$ | I/O$_{45}$ | I/O$_{44}$ | GND | GND | I/O$_{144}$ | I/O$_{145}$ | CLK$_{2}$ /I$_{3}$ | I/O$_{146}$ | I/O$_{147}$ | GND | GND |
| J | GND | GND | I/O$_{51}$ | I/O$_{50}$ | NC | I/O$_{49}$ | I/O$_{48}$ | GND | GND | I/O$_{140}$ | I/O$_{141}$ | I$_{2}$ | I/O$_{142}$ | I/O$_{143}$ | GND | GND |
| K | I/O$_{57}$ | I/O$_{56}$ | I/O$_{55}$ | I/O$_{54}$ | CLK$_{1}$ /I$_{1}$ | I/O$_{53}$ | I/O$_{52}$ | I/O$_{91}$ | I/O$_{96}$ | I/O$_{101}$ | I/O$_{135}$ | $V_{CC}$ | I/O$_{136}$ | I/O$_{137}$ | I/O$_{138}$ | I/O$_{139}$ |
| L | $V_{CC}$ | I/O$_{60}$ | I/O$_{59}$ | I/O$_{58}$ | TMS | $V_{CC}$ | I/O$_{86}$ | I/O$_{92}$ | I/O$_{97}$ | I/O$_{102}$ | $V_{CC}$ | TDO | I/O$_{132}$ | I/O$_{133}$ | I/O$_{134}$ | $V_{CC}$ |
| M | I/O$_{63}$ | I/O$_{62}$ | I/O$_{61}$ | I/O$_{72}$ | I/O$_{77}$ | I/O$_{82}$ | $V_{CC}$ | I/O$_{93}$ | I/O$_{98}$ | I/O$_{103}$ | I/O$_{108}$ | I/O$_{112}$ | I/O$_{117}$ | I/O$_{129}$ | I/O$_{130}$ | I/O$_{131}$ |
| N | I/O$_{66}$ | I/O$_{65}$ | I/O$_{64}$ | I/O$_{73}$ | I/O$_{78}$ | I/O$_{83}$ | I/O$_{87}$ | I/O$_{94}$ | I/O$_{99}$ | I/O$_{104}$ | I/O$_{109}$ | I/O$_{113}$ | NC | I/O$_{126}$ | I/O$_{127}$ | I/O$_{128}$ |
| P | I/O$_{68}$ | I/O$_{67}$ | NC | I/O$_{74}$ | I/O79 | I/O$_{84}$ | I/O$_{88}$ | I/O$_{95}$ | I/O$_{100}$ | I/O$_{105}$ | I/O$_{110}$ | I/O$_{114}$ | I/O$_{118}$ | NC | I/O$_{124}$ | I/O$_{125}$ |
| R | GND | I/O$_{69}$ | I/O$_{70}$ | I/O$_{75}$ | I/O$_{80}$ | I/O$_{85}$ | I/O$_{89}$ | GND | GND | I/O$_{106}$ | I/O$_{111}$ | I/O$_{115}$ | I/O$_{119}$ | I/O$_{121}$ | I/O$_{123}$ | GND |
| T | GND | GND | I/O$_{71}$ | I/O$_{76}$ | I/O$_{81}$ | $V_{CC}$ | I/O$_{90}$ | GND | GND | I/O$_{107}$ | $V_{CC}$ | I/O$_{116}$ | I/O$_{120}$ | I/O$_{122}$ | GND | GND |

## 5.0V Ordering Information (continued)

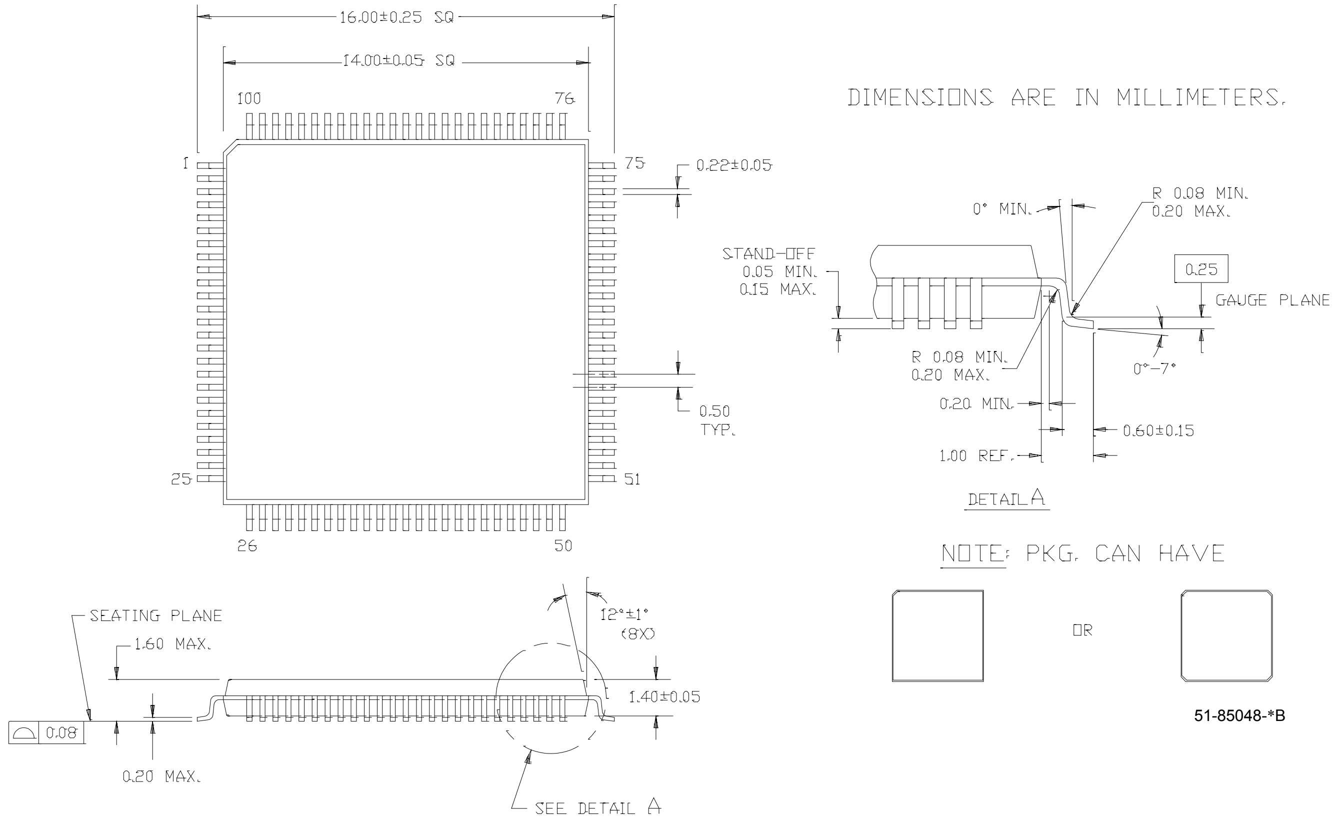
| Macrocells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|---|
| 128 | 167 | CY37128P84-167JC | J83 | 84-Lead Plastic Leaded Chip Carrier | Commercial |
| | | CY37128P84-167JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | | CY37128P100-167AC | A100 | 100-Lead Thin Quad Flat Pack | |
| | | CY37128P100-167AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128P160-167AC | A160 | 160-Lead Thin Quad Flat Pack | |
| | | CY37128P160-167AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | 125 | CY37128P84-125JC | J83 | 84-Lead Plastic Leaded Chip Carrier | Commercial |
| | | CY37128P84-125JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | | CY37128P100-125AC | A100 | 100-Lead Thin Quad Flat Pack | |
| | | CY37128P100-125AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128P160-125AC | A160 | 160-Lead Thin Quad Flat Pack | |
| | | CY37128P160-125AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128P84-125JI | J83 | 84-Lead Plastic Leaded Chip Carrier | Industrial |
| | | CY37128P84-125JXI | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | | CY37128P100-125AI | A100 | 100-Lead Thin Quad Flat Pack | |
| | | CY37128P100-125AXI | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128P160-125AI | A160 | 160-Lead Thin Quad Flat Pack | |
| | | CY37128P160-125AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | 5962-9952102QYA | Y84 | 84-Lead Ceramic Leaded Chip Carrier | Military |
| | 100 | CY37128P84-100JC | J83 | 84-Lead Plastic Leaded Chip Carrier | Commercial |
| | | CY37128P84-100JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | | CY37128P100-100AC | A100 | 100-Lead Thin Quad Flat Pack | |
| | | CY37128P100-100AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128P160-100AC | A160 | 160-Lead Thin Quad Flat Pack | |
| | | CY37128P160-100AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128P84-100JI | J83 | 84-Lead Plastic Leaded Chip Carrier | Industrial |
| | | CY37128P100-100AI | A100 | 100-Lead Thin Quad Flat Pack | |
| | | CY37128P100-100AXI | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128P160-100AI | A160 | 160-Lead Thin Quad Flat Pack | |
| | | 5962-9952101QYA | Y84 | 84-Lead Ceramic Leaded Chip Carrier | Military |
| 192 | 154 | CY37192P160-154AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial |
| | | CY37192P160-154AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | 125 | CY37192P160-125AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial |
| | | CY37192P160-125AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37192P160-125AI | A160 | 160-Lead Thin Quad Flat Pack | Industrial |
| | | CY37192P160-125AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | 83 | CY37192P160-83AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial |
| | | CY37192P160-83AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37192P160-83AI | A160 | 160-Lead Thin Quad Flat Pack | Industrial |
| | | CY37192P160-83AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |

## 3.3V Ordering Information (continued)

| Macrocells | Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|---|
| 64 | 143 | CY37064VP44-143AC | A44 | 44-Lead Thin Quad Flatpack | Commercial |
| | | CY37064VP44-143AXC | A44 | 44-Lead Lead Free Thin Quad Flatpack | |
| | | CY37064VP48-143BAC | BA50 | 48-Ball Fine-Pitch Ball Grid Array | |
| | | CY37064VP100-143AC | A100 | 100-Lead Thin Quad Flatpack | |
| | | CY37064VP100-143AXC | A100 | 100-Lead Lead Free Thin Quad Flatpack | |
| | | CY37064VP100-143BBC | BB100 | 100-Ball Fine-Pitch Ball Grid Array | |
| | 100 | CY37064VP44-100AC | A44 | 44-Lead Thin Quad Flatpack | Commercial |
| | | CY37064VP44-100AXC | A44 | 44-Lead Lead Free Thin Quad Flatpack | |
| | | CY37064VP48-100BAC | BA50 | 48-Ball Fine-Pitch Ball Grid Array | |
| | | CY37064VP100-100AC | A100 | 100-Lead Thin Quad Flatpack | |
| | | CY37064VP100-100AXC | A100 | 100-Lead Lead Free Thin Quad Flatpack | |
| | | CY37064VP100-100BBC | BB100 | 100-Ball Fine-Pitch Ball Grid Array | |
| | | CY37064VP44-100AI | A44 | 44-Lead Thin Quad Flatpack | Industrial |
| | | CY37064VP44-100AXI | A44 | 44-Lead Lead Free Thin Quad Flatpack | |
| | | CY37064VP48-100BAI | BA50 | 48-Ball Fine-Pitch Ball Grid Array | |
| | | CY37064VP100-100BBI | BB100 | 100-Ball Fine-Pitch Ball Grid Array | |
| | | CY37064VP100-100AI | A100 | 100-Lead Thin Quad Flatpack | |
| | | CY37064VP100-100AXI | A100 | 100-Lead Lead Free Thin Quad Flatpack | |
| | | 5962-9952001QYA | Y67 | 44-Lead Ceramic Leaded Chip Carrier | Military |
| 128 | 125 | CY37128VP100-125AC | A100 | 100-Lead Thin Quad Flat Pack | Commercial |
| | | CY37128VP100-125AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128VP100-125BBC | BB100 | 100-Ball Fine-Pitch Ball Grid Array | |
| | | CY37128VP160-125AC | A160 | 160-Lead Thin Quad Flat Pack | |
| | | CY37128VP160-125AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128VP160-125AI | A160 | 160-Lead Thin Quad Flat Pack | Industrial |
| | | CY37128VP160-125AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | 83 | CY37128VP100-83AC | A100 | 100-Lead Thin Quad Flat Pack | Commercial |
| | | CY37128VP100-83AXC | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128VP100-83BBC | BB100 | 100-Ball Fine-Pitch Ball Grid Array | |
| | | CY37128VP160-83AC | A160 | 160-Lead Thin Quad Flat Pack | |
| | | CY37128VP160-83AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128VP100-83AI | A100 | 100-Lead Thin Quad Flat Pack | Industrial |
| | | CY37128VP100-83AXI | A100 | 100-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37128VP100-83BBI | BB100 | 100-Ball Fine-Pitch Ball Grid Array | |
| | | CY37128VP160-83AI | A160 | 160-Lead Thin Quad Flat Pack | |
| | | CY37128VP160-83AXI | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | 5962-9952201QYA | Y84 | 84-Lead Ceramic Leaded Chip Carrier | Military |
| 192 | 100 | CY37192VP160-100AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial |
| | | CY37192VP160-100AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | 66 | CY37192VP160-66AC | A160 | 160-Lead Thin Quad Flat Pack | Commercial |
| | | CY37192VP160-66AXC | A160 | 160-Lead Lead Free Thin Quad Flat Pack | |
| | | CY37192VP160-66AI | A160 | 160-Lead Thin Quad Flat Pack | Industrial |

## Package Diagrams (continued)

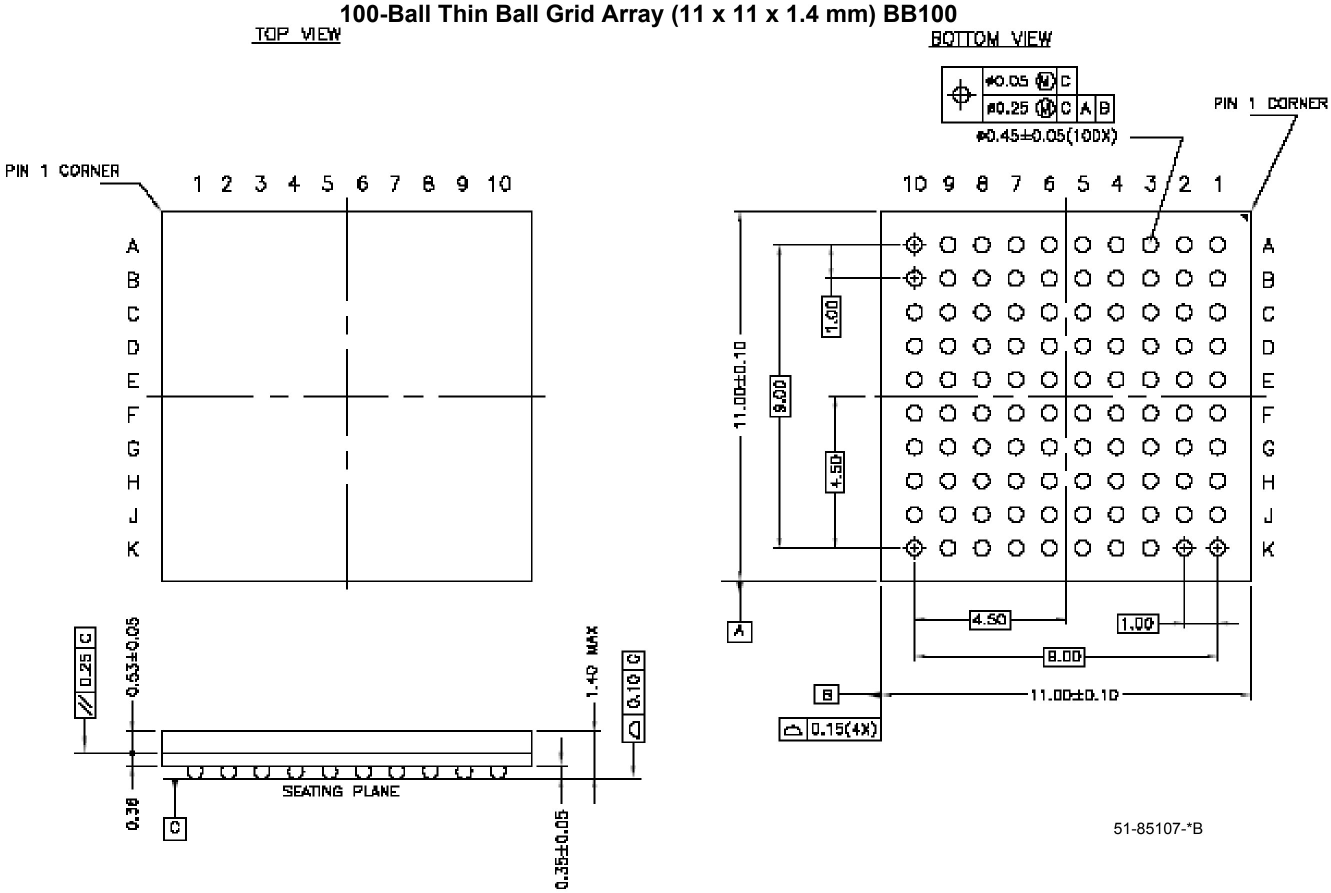
### 100-Lead Lead (Pb)-Free Thin Plastic Quad Flat Pack (TQFP) A100




51-85048-*B

## Package Diagrams (continued)

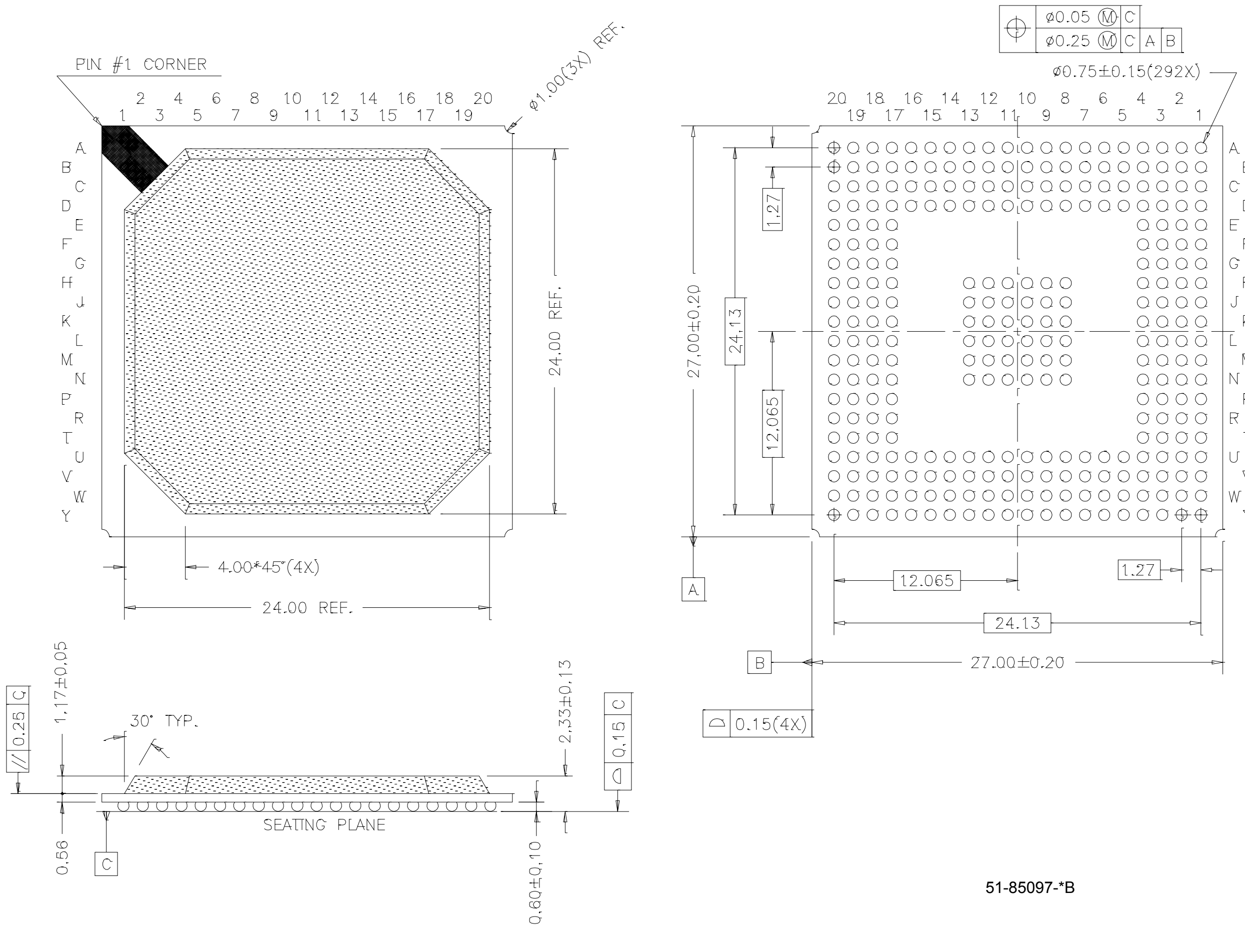
### 100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100




51-85107-*B

**Package Diagrams** (continued)

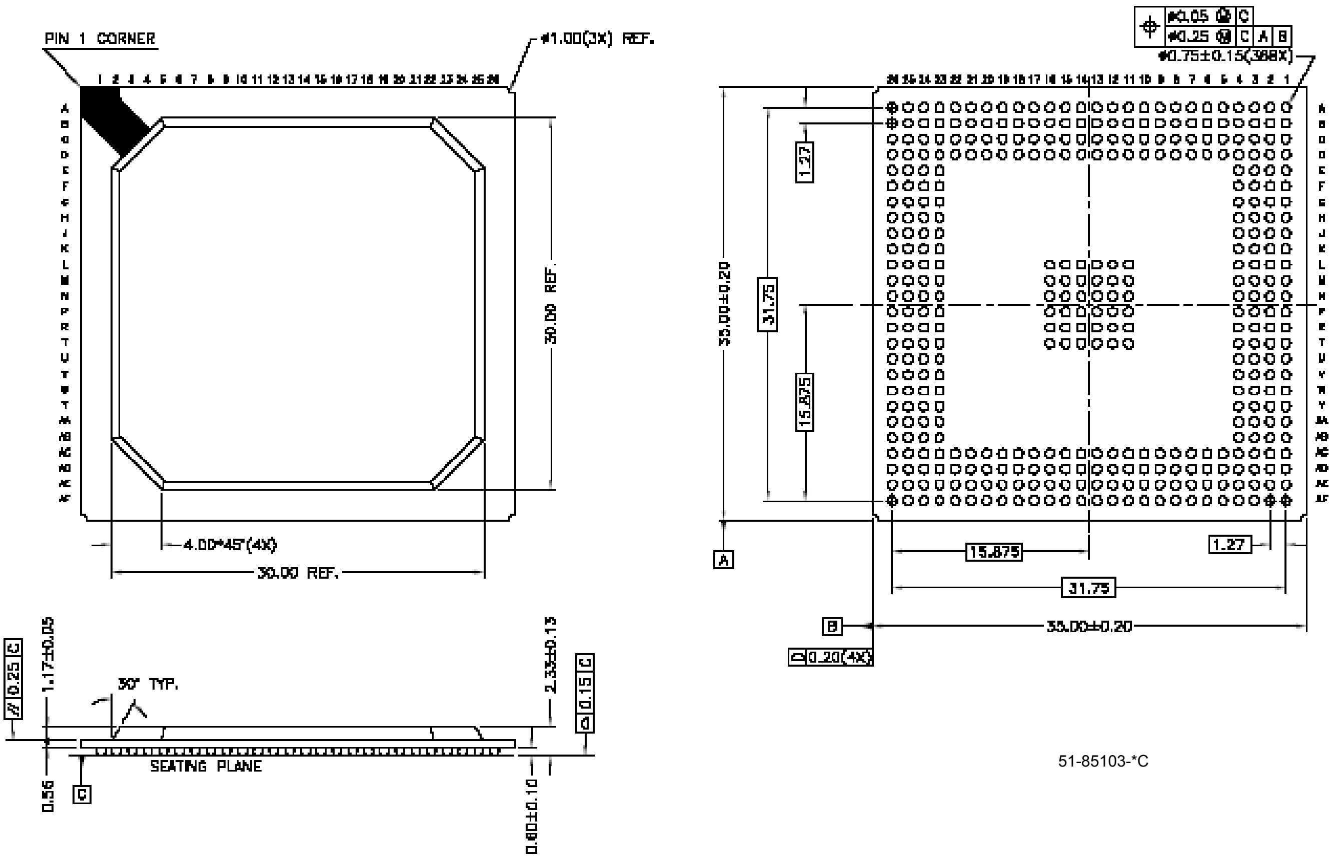
**292-Ball Plastic Ball Grid Array PBGA (27 x 27 x 2.33 mm) BG292**




51-85097-*B

## Package Diagrams (continued)

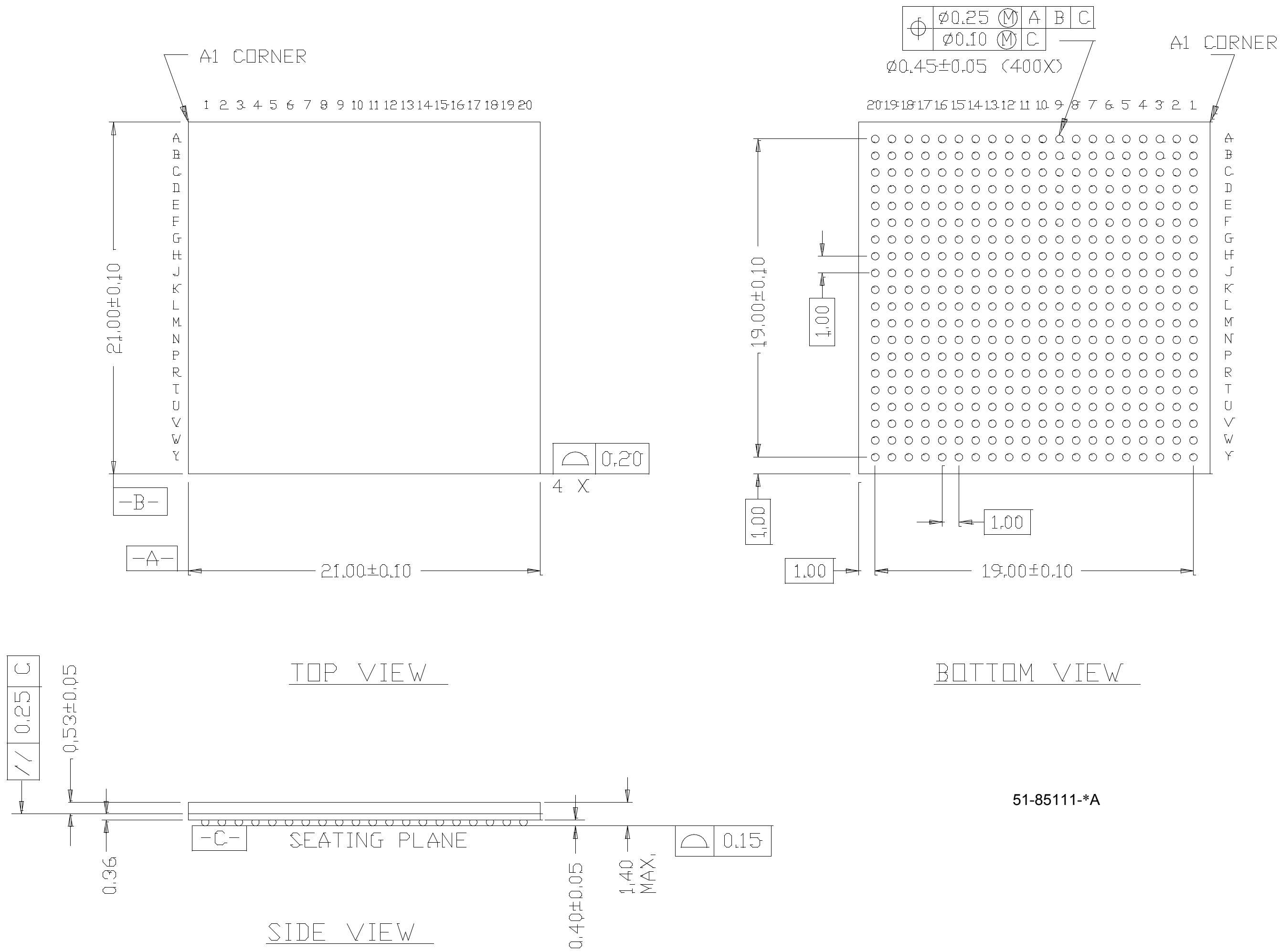
**388-Ball Plastic Ball Grid Array PBGA (35 x 35 x 2.33 mm) BG388**




51-85103-*C

## Package Diagrams (continued)

**400-Ball FBGA (21 x 21 x 1.4 mm) BB400**




51-85111-*A

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## Addendum

### 3.3V Operating Range

**(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)**

| Range | Ambient Temperature[2] | Junction Temperature | $V_{CC}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0°C to +90°C | 3.3V ± 0.16V |