Infineon Technologies - CY37256VP160-66AXC Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In-System Reprogrammable™ (ISR™) CMOS
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	133
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy37256vp160-66axc

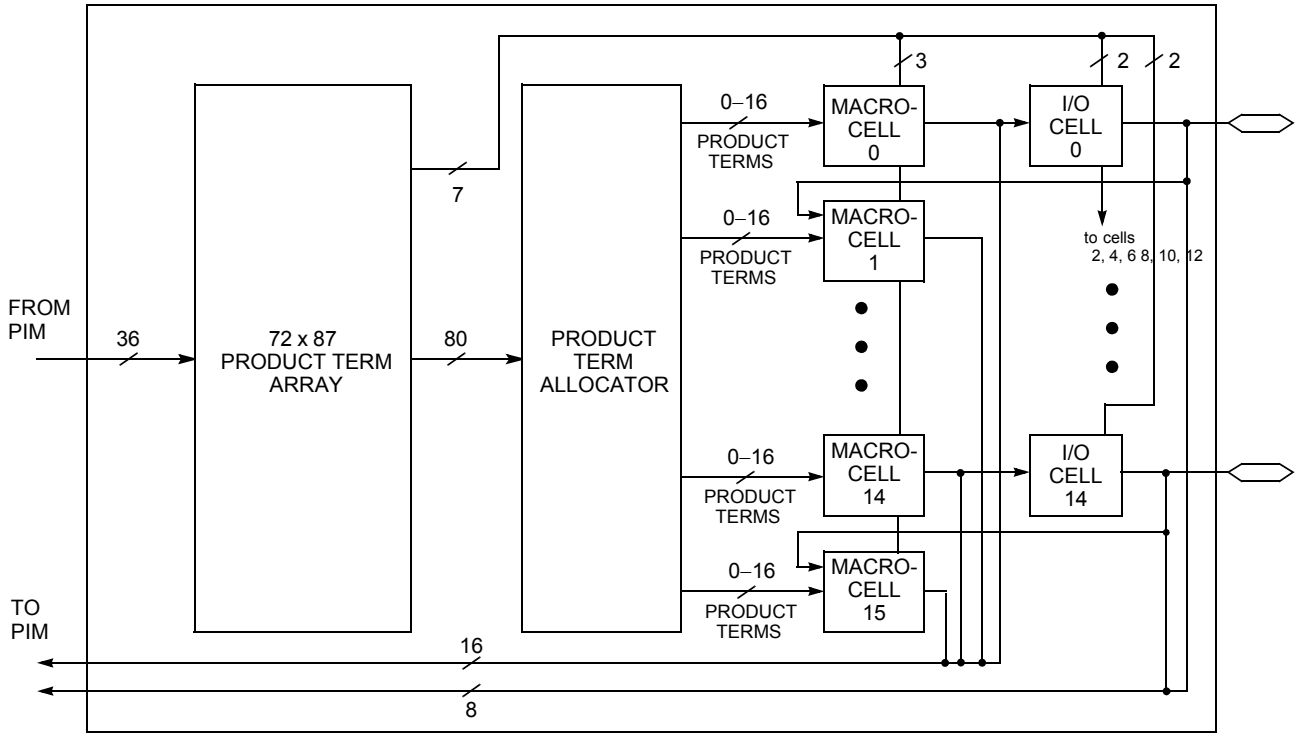


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

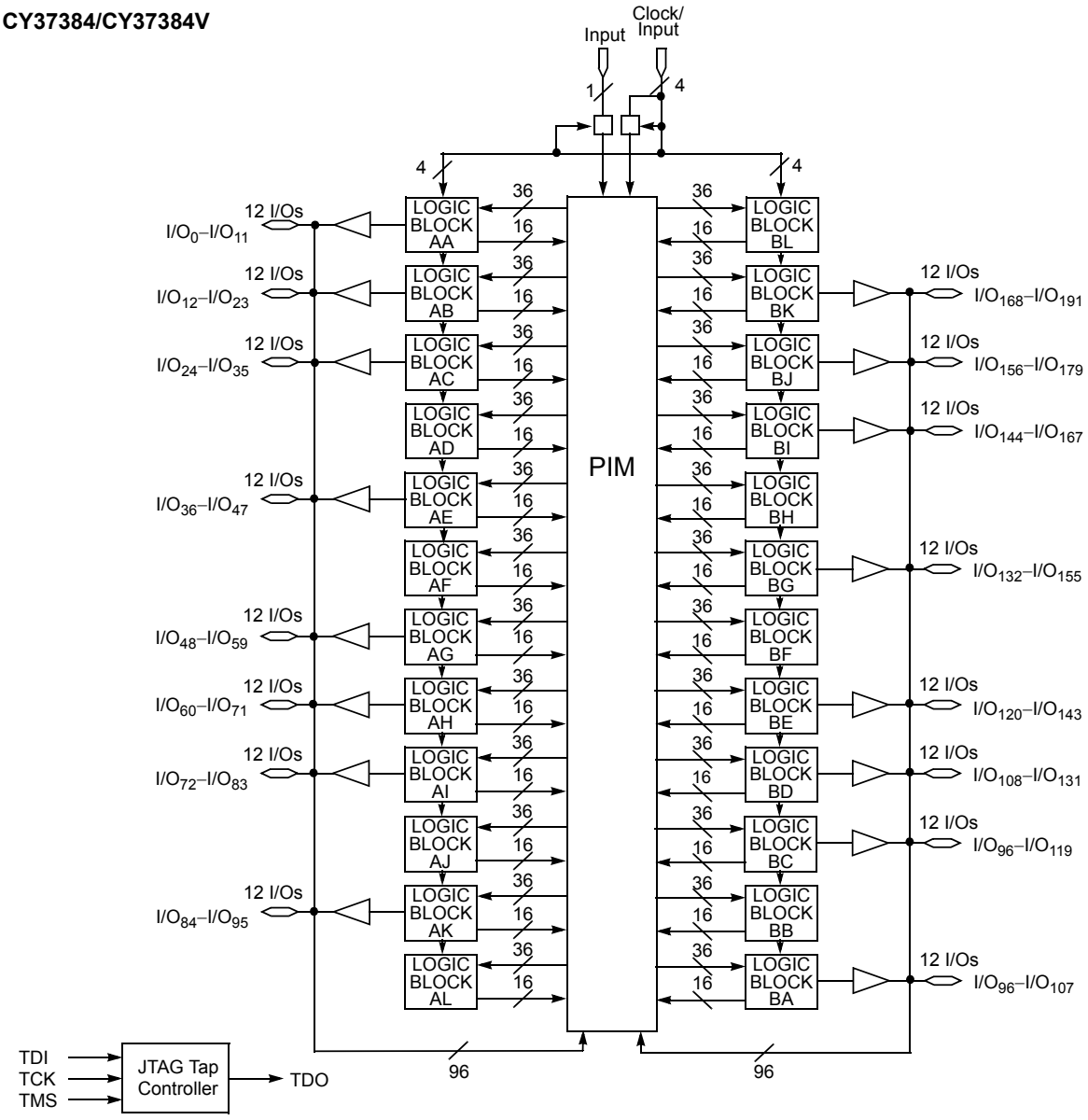
Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

Logic Block Diagrams (continued)

CY37384/CY37384V



Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual-Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

3.3V Device Characteristics Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 3.0 to 3.6V

Current into Outputs ..... 8 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}[10]
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[5, 8]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Notes:
9. Dual pins are I/O with JTAG pins.
10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range: V_{CC} is 3.3V± 0.16V.

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

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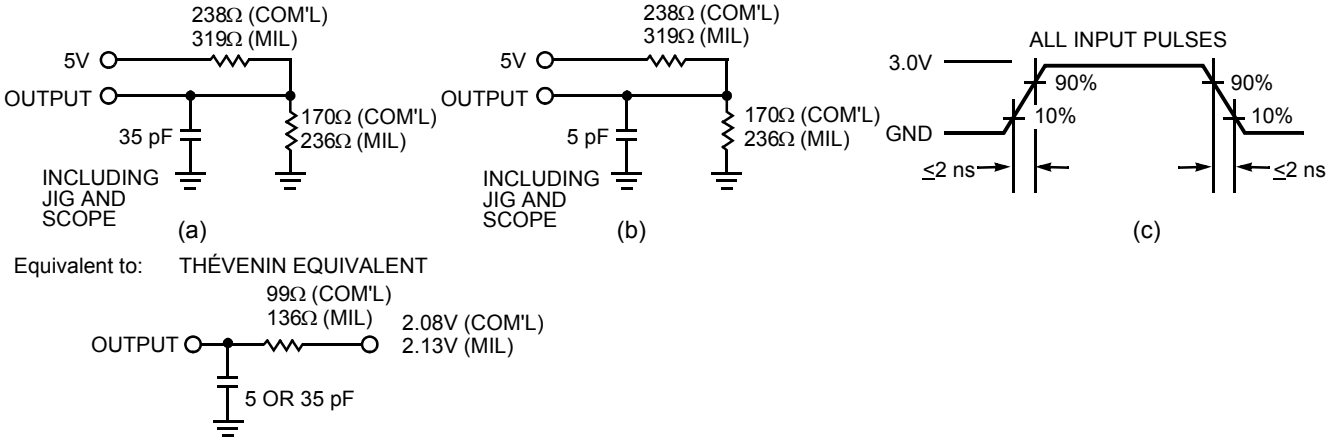
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

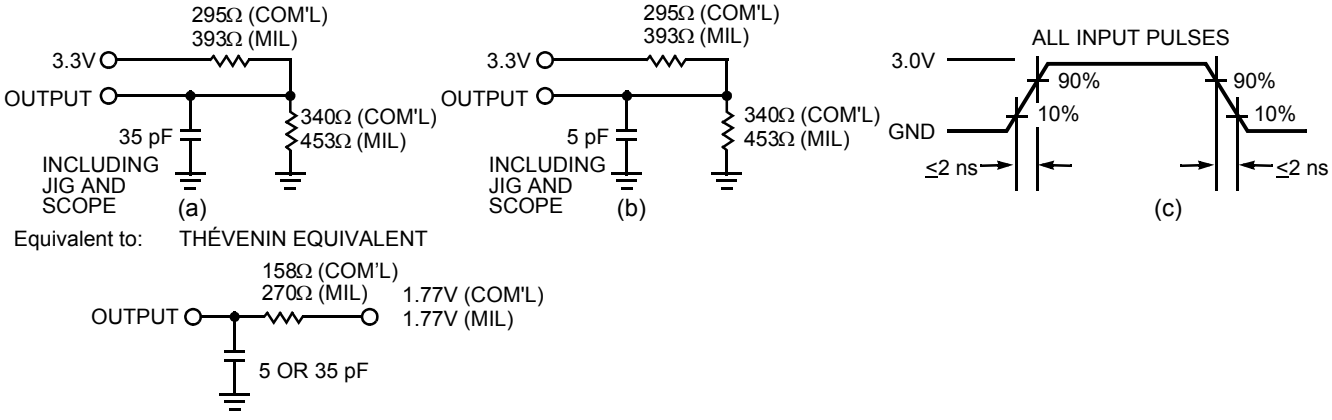
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Characteristics

5.0V AC Test Loads and Waveforms

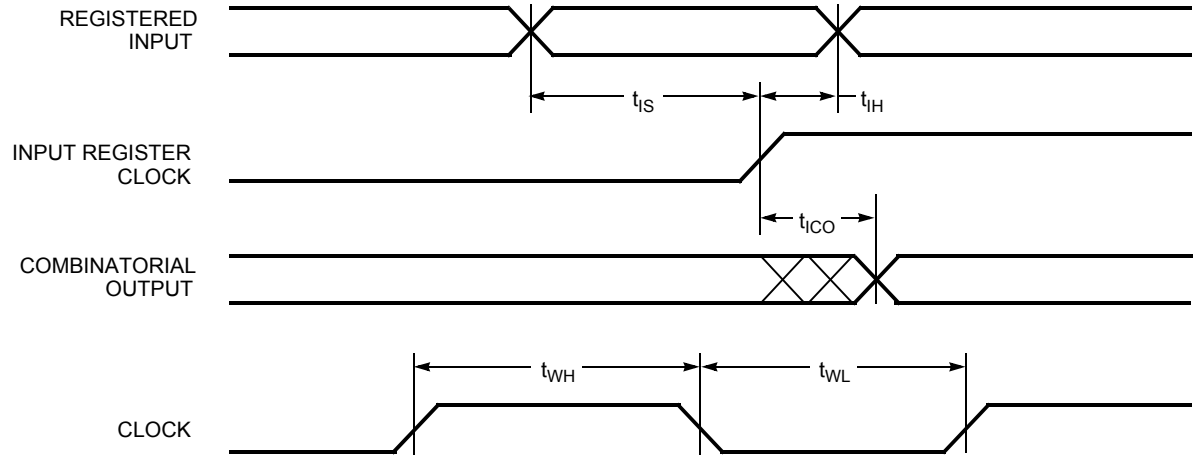


3.3V AC Test Loads and Waveforms

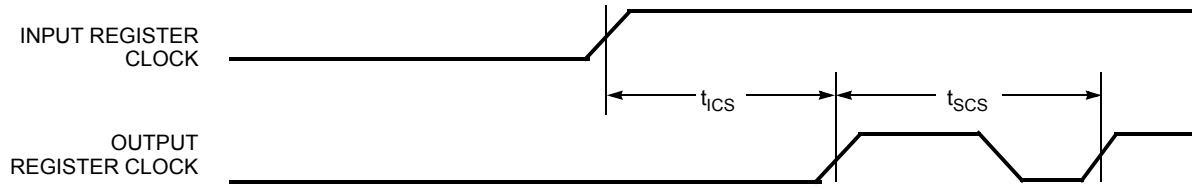


Switching Waveforms (continued)

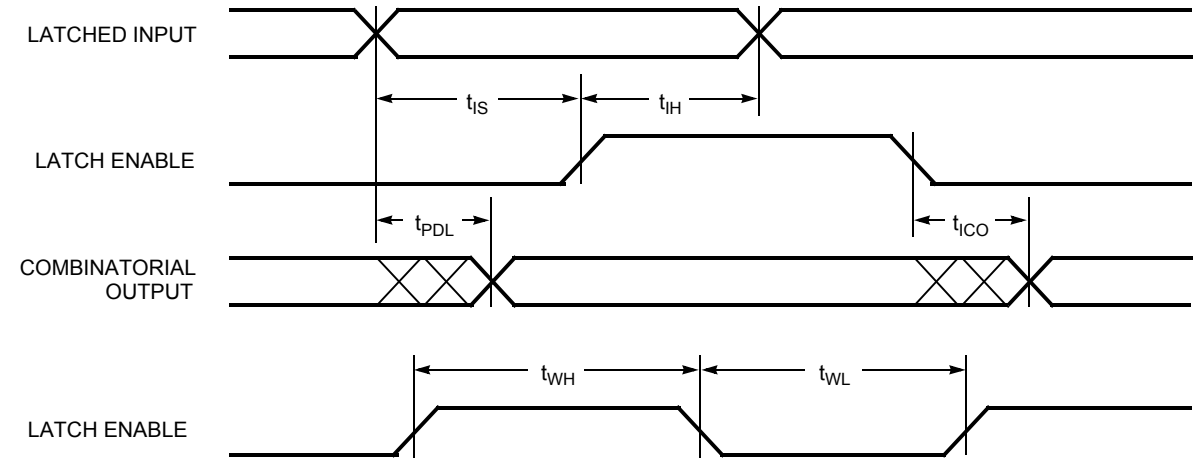
Registered Input



Clock to Clock

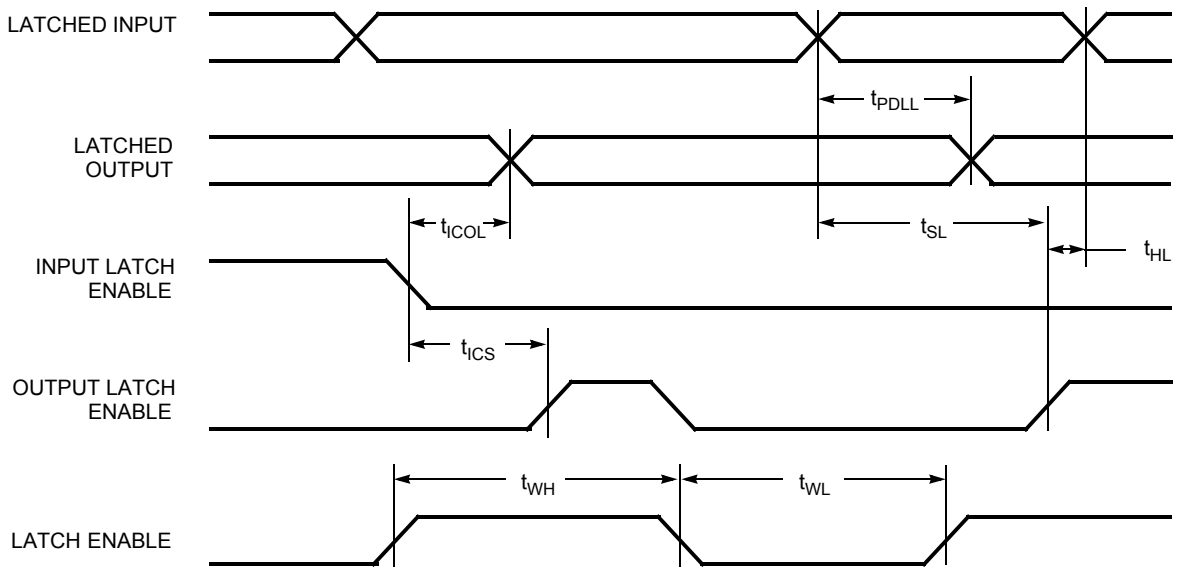


Latched Input

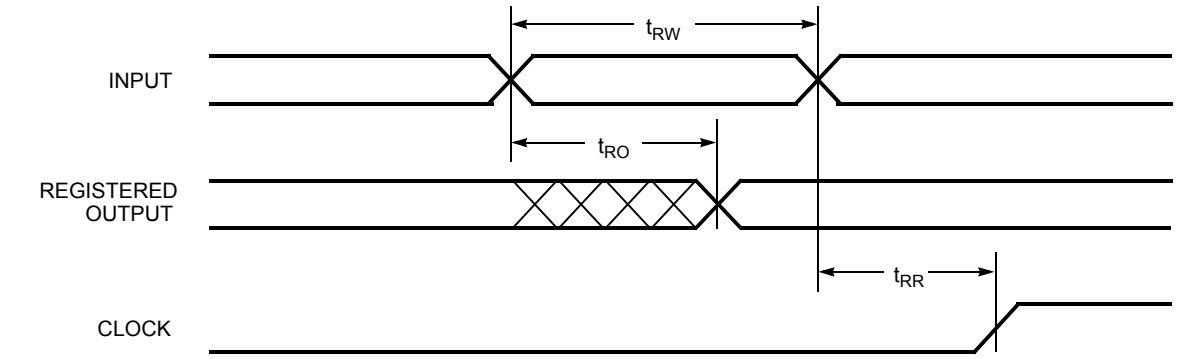


Switching Waveforms (continued)

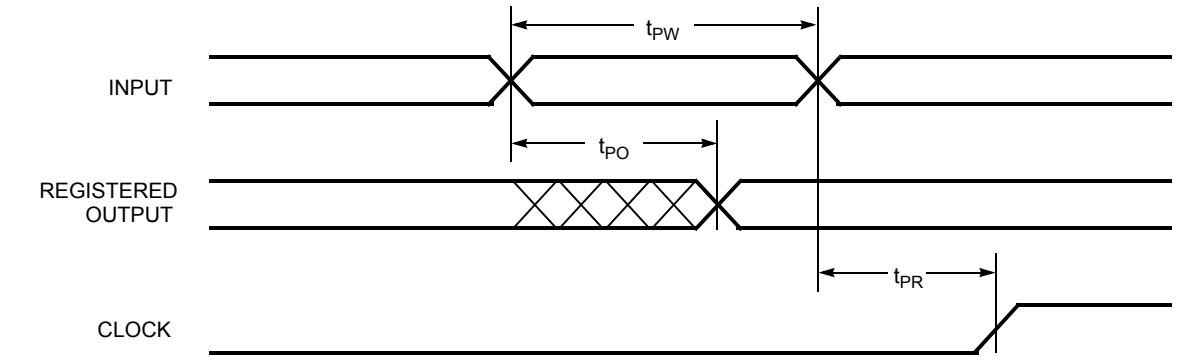
Latched Input and Output



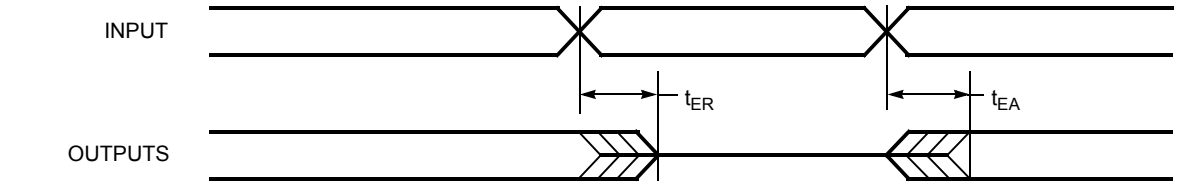
Asynchronous Reset



Asynchronous Preset



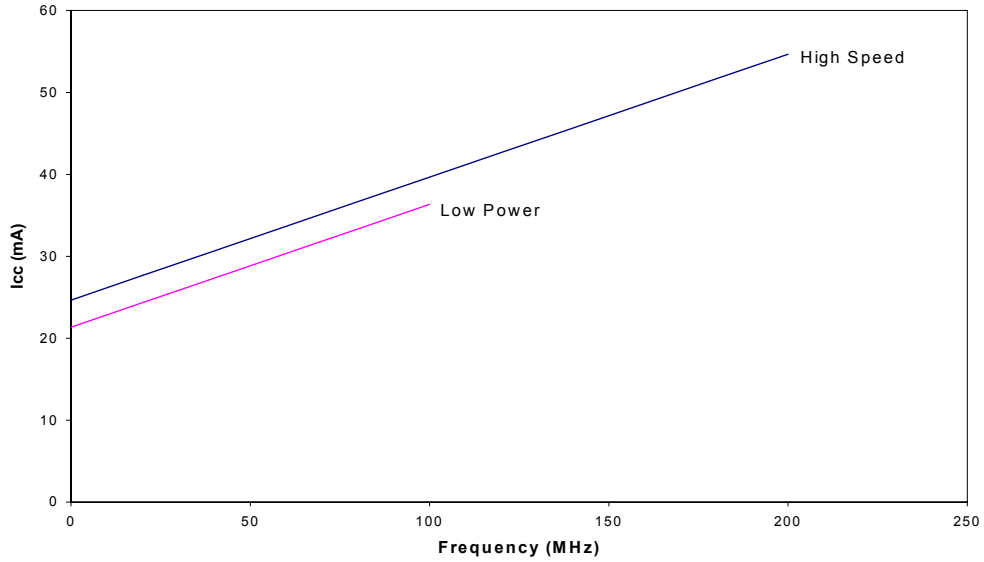
Output Enable/Disable



Power Consumption

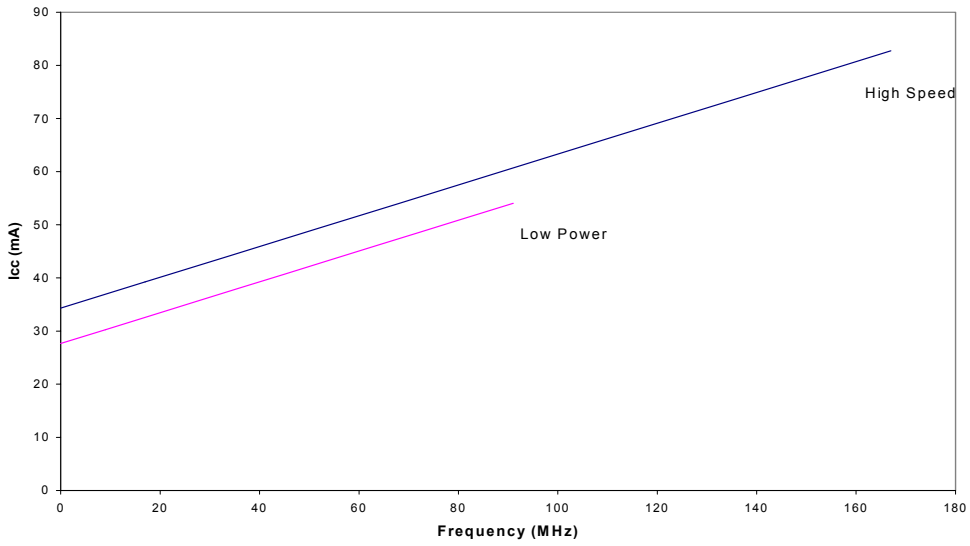
Typical 5.0V Power Consumption

CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

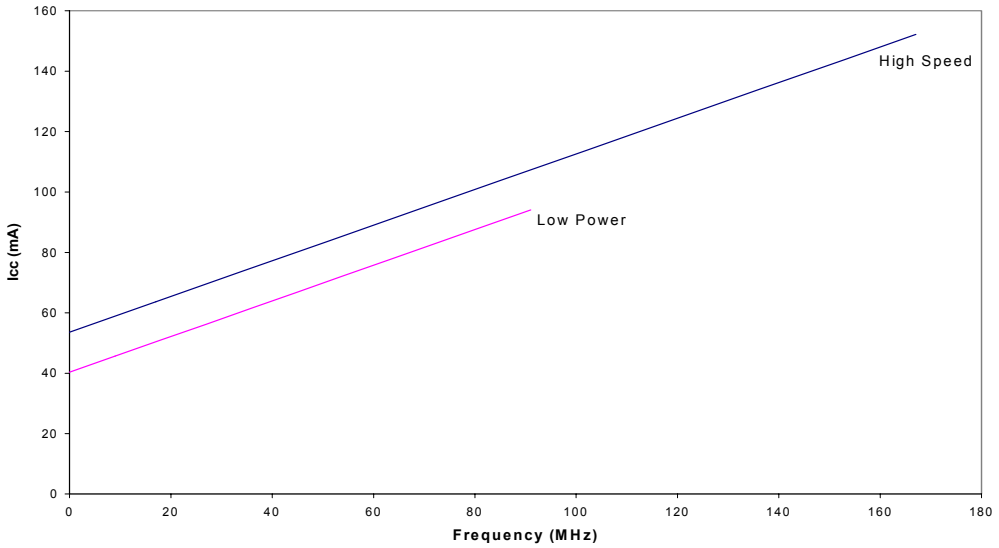
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

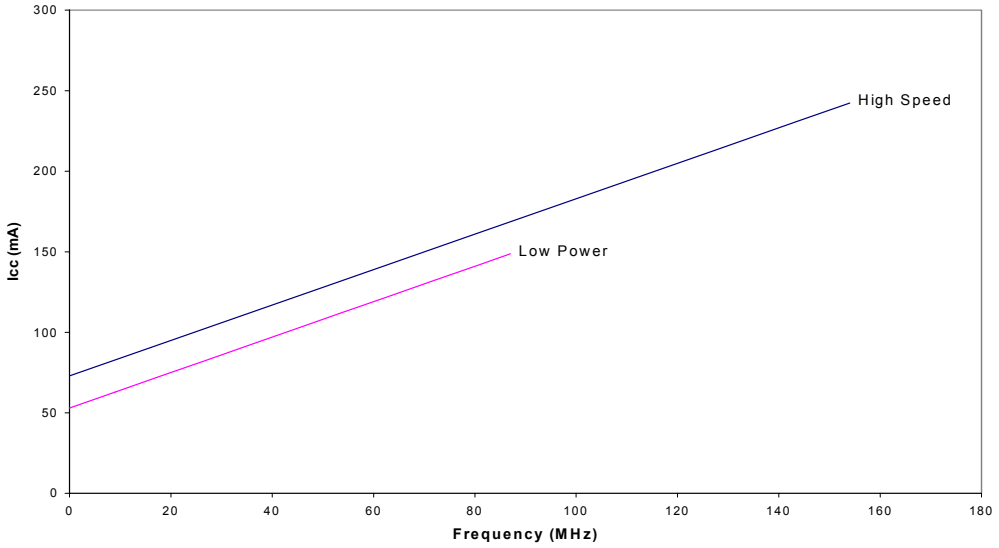
Typical 5.0V Power Consumption (continued)

CY37128



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

CY37192

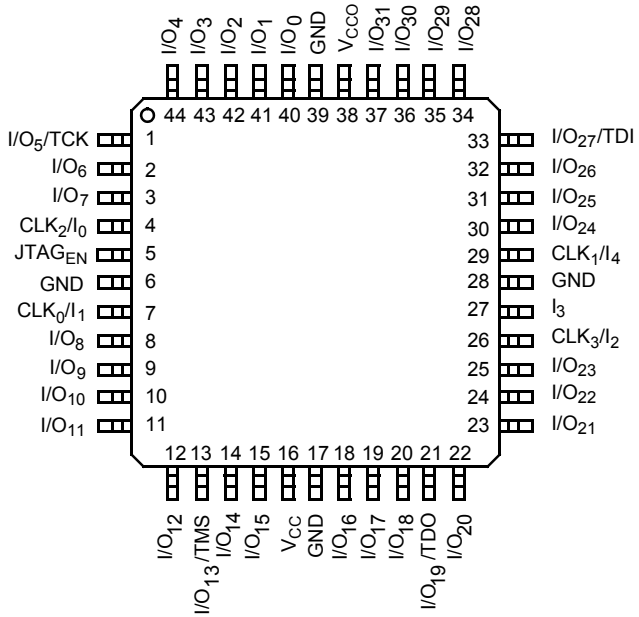


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Pin Configurations[20]

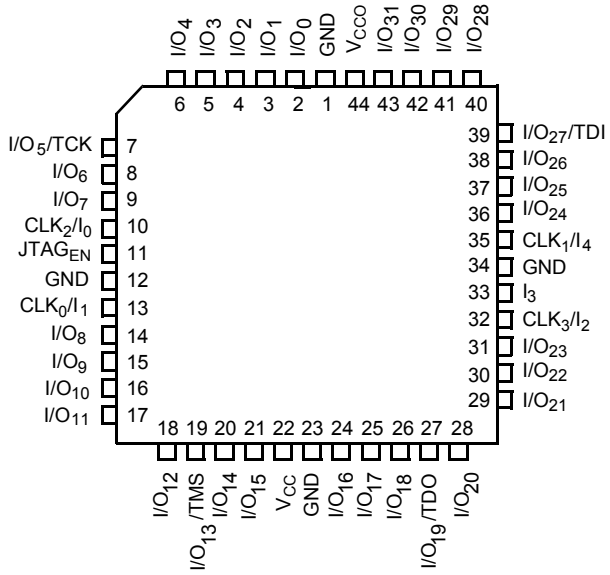
44-pin TQFP (A44)

Top View



44-pin PLCC (J67) / CLCC (Y67)

Top View



Pin Configurations[20] (continued)

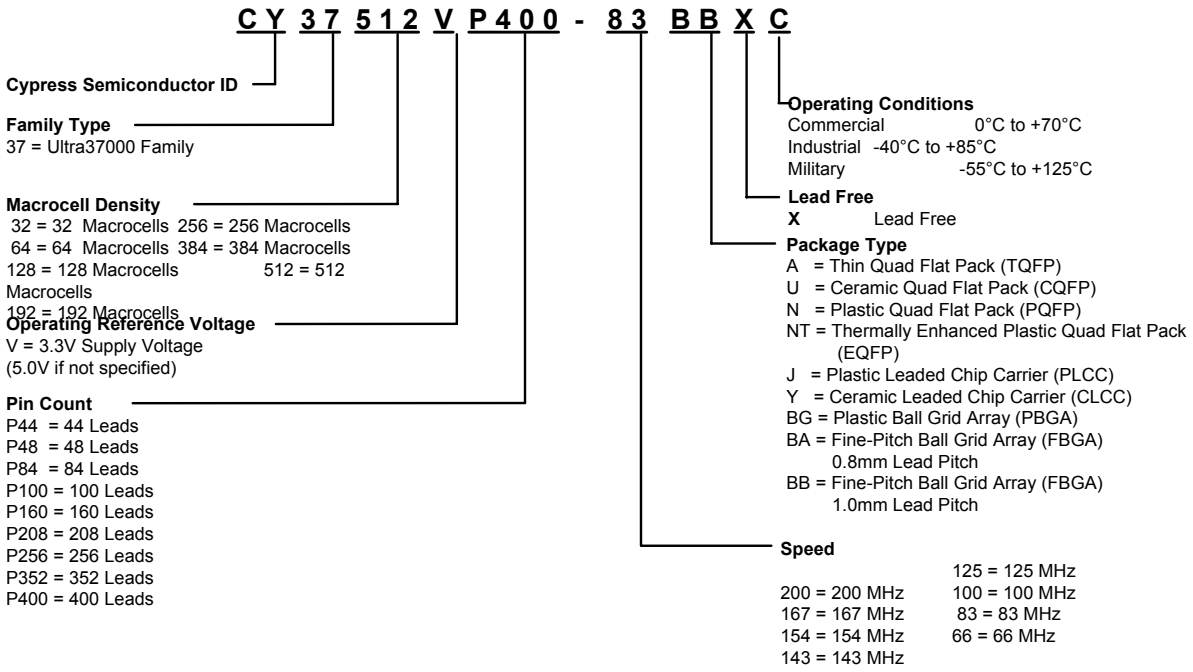
100-ball Fine-Pitch BGA (BB100) for CY37064V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	NC	I/O_7	I/O_5	I/O_2	I/O_{62}	I/O_{60}	I/O_{58}	I/O_{57}	I/O_{56}
B	I/O_9	I/O_8	I/O_6	I/O_4	I/O_1	I/O_{63}	V_{CC}	I/O_{59}	I/O_{55}	NC
C	I/O_{10}	TCK	V_{CC}	I/O_3	NC	NC	I/O_{61}	V_{CC}	TDI	I/O_{54}
D	I/O_{11}	NC	I/O_{12}	I/O_{13}	I/O_0	NC	I/O_{51}	I/O_{52}	CLK_3/I_4	I/O_{53}
E	I/O_{14}	CLK_0/I_0	I/O_{15}	NC	GND	GND	I/O_{48}	I/O_{49}	CLK_2/I_3	I/O_{50}
F	I/O_{17}	NC	NC	I/O_{16}	GND	GND	NC	NC	I_2	I/O_{47}
G	I/O_{22}	CLK_1/I_1	I/O_{21}	I/O_{19}	I/O_{18}	I/O_{46}	I/O_{45}	I/O_{44}	NC	I/O_{43}
H	I/O_{23}	TMS	V_{CC}	I/O_{20}	NC	I/O_{32}	I/O_{42}	V_{CC}	TDO	I/O_{41}
J	NC	I/O_{26}	I/O_{28}	NC	I/O_{31}	I/O_{33}	I/O_{35}	I/O_{37}	I/O_{39}	I/O_{40}
K	I/O_{24}	I/O_{25}	I/O_{27}	I/O_{29}	I/O_{30}	I/O_{34}	I/O_{36}	I/O_{38}	NC	NC

100-ball Fine-Pitch BGA (BB100) for CY37128V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	I/O_9	I/O_8	I/O_6	I/O_3	I/O_{76}	I/O_{74}	I/O_{72}	I/O_{71}	I/O_{70}
B	I/O_{11}	I/O_{10}	I/O_7	I/O_5	I/O_2	I/O_{77}	V_{CC}	I/O_{73}	I/O_{68}	I/O_{69}
C	I/O_{12}	I/O_{13} TCK	V_{CC}	I/O_4	I/O_1	I/O_{78}	I/O_{75}	V_{CC}	I/O_{67} TDI	I/O_{66}
D	I/O_{14}	NC	I/O_{15}	I/O_{16}	I/O_0	I/O_{79}	I/O_{63}	I/O_{64}	CLK_3/I_4	I/O_{65}
E	I/O_{17}	CLK_0/I_0	I/O_{18}	I/O_{19}	GND	GND	I/O_{60}	I/O_{61}	CLK_2/I_3	I/O_{62}
F	I/O_{22}	JTAG EN	I/O_{21}	I/O_{20}	GND	GND	I/O_{59}	I/O_{58}	I_2	I/O_{57}
G	I/O_{27}	CLK_1/I_1	I/O_{26}	I/O_{24}	I/O_{23}	I/O_{56}	I/O_{55}	I/O_{54}	NC	I/O_{53}
H	I/O_{28}	I/O_{33} TMS	V_{CC}	I/O_{25}	I/O_{39}	I/O_{40}	I/O_{52}	V_{CC}	I/O_{47} TDO	I/O_{51}
J	I/O_{29}	I/O_{32}	I/O_{35}	V_{CC}	I/O_{38}	I/O_{41}	I/O_{43}	I/O_{45}	I/O_{48}	I/O_{50}
K	I/O_{30}	I/O_{31}	I/O_{34}	I/O_{36}	I/O_{37}	I/O_{42}	I/O_{44}	I/O_{46}	I/O_{49}	NC

Ordering Information



5.0V Ordering Information

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	200	CY37032P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-200AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-200JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
	154	CY37032P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
	125	CY37032P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37032P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37032P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
64	200	CY37064P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-200AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-200JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-200JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-200AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-200AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	

5.0V Ordering Information (continued)

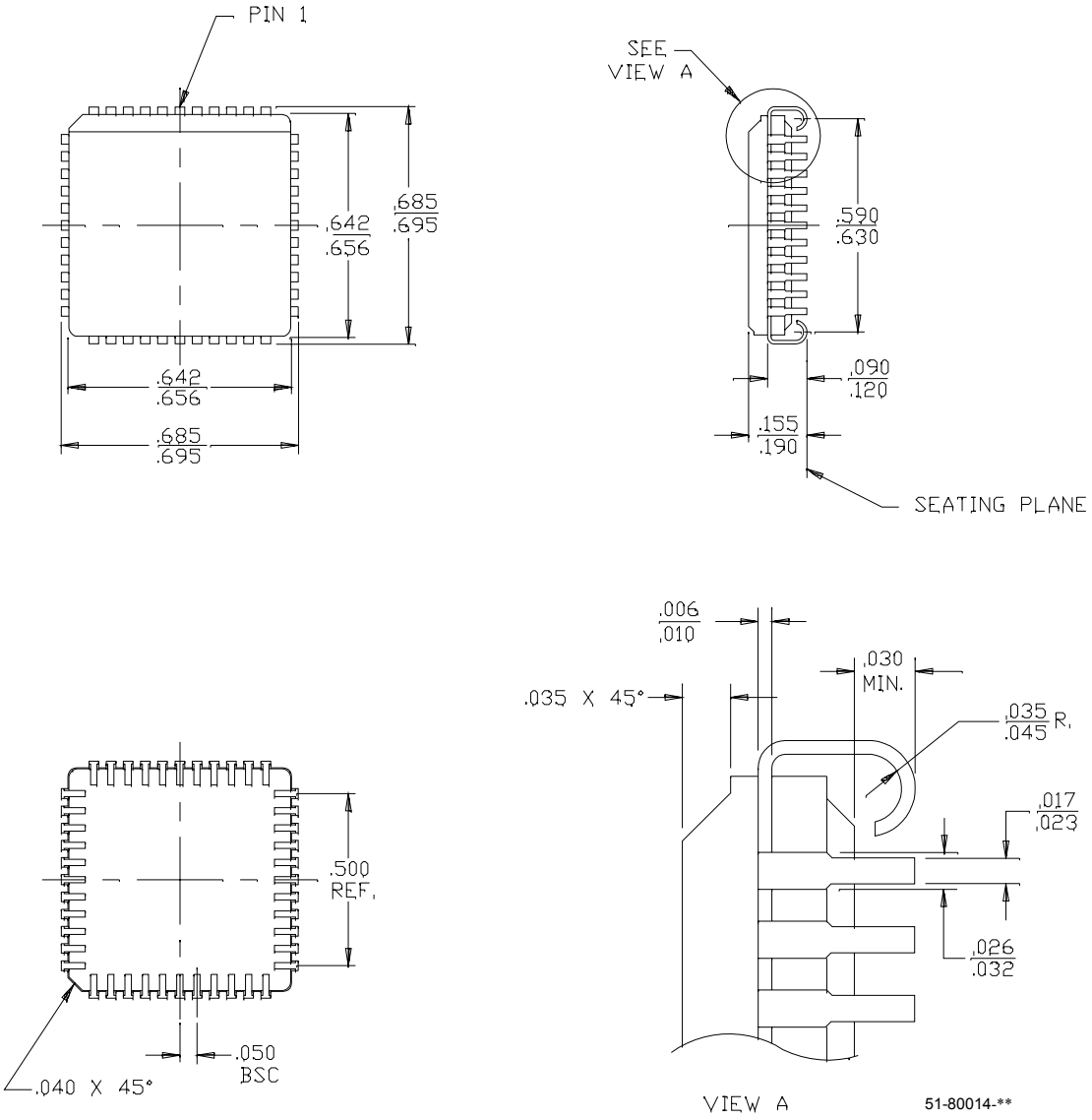
Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-154JXI	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125AXC	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P44-125JXC	J67	44-Lead Lead Free Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXC	A100	100-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125AXI	A44	44-Lead Lead Free Thin Quad Flat Pack	
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37064P100-125AXI	A100	100-Lead Lead Free Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military

3.3V Ordering Information (continued)

Macrocells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-100AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-100AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP160-100AXI	A160	160-Lead Lead Free Thin Quad Flat Pack	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP160-66AXC	A160	160-Lead Lead Free Thin Quad Flat Pack	
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Ball Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Ball Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-83BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGC	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Ball Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG292	292-Ball Plastic Ball Grid Array	
		CY37512VP352-66BGI	BG388	388-Ball Plastic Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Ball Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

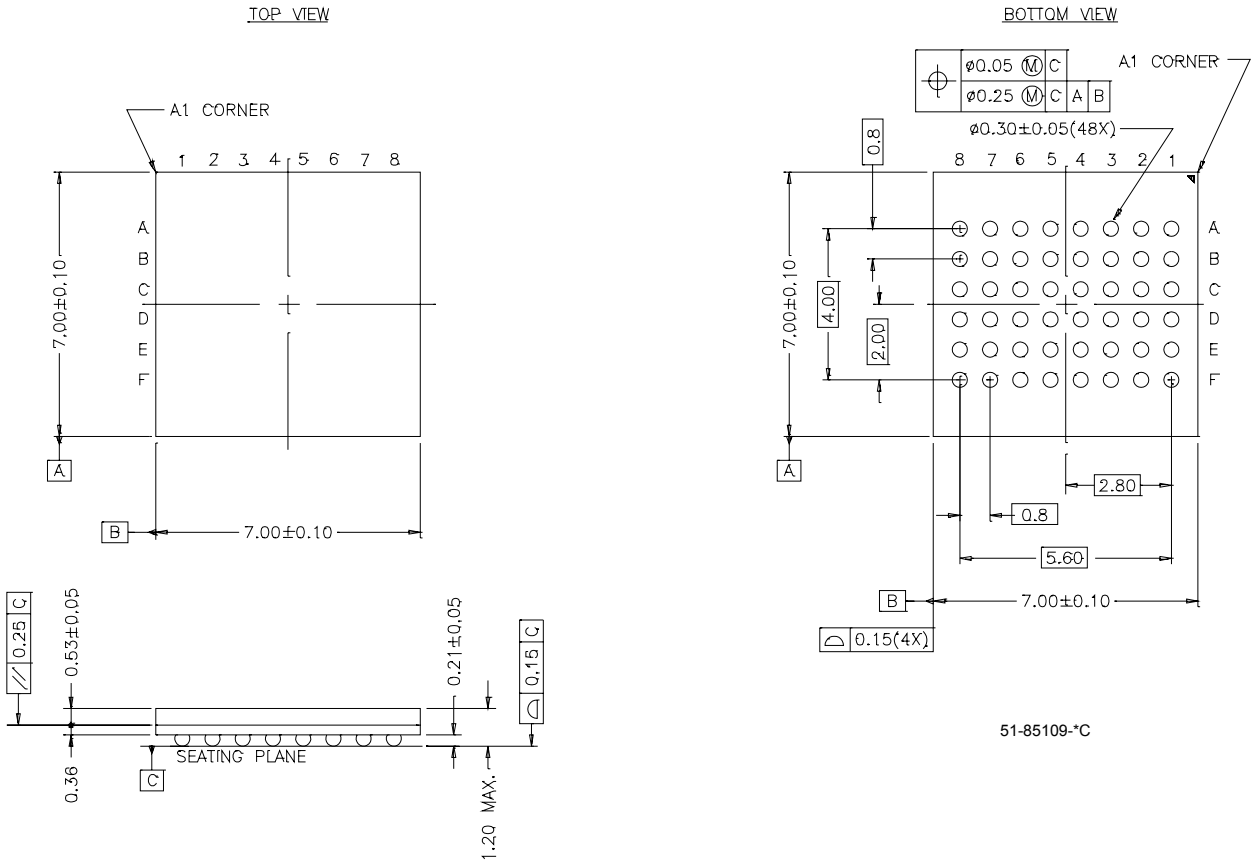
Package Diagrams (continued)

44-Lead Ceramic Leaded Chip Carrier Y67

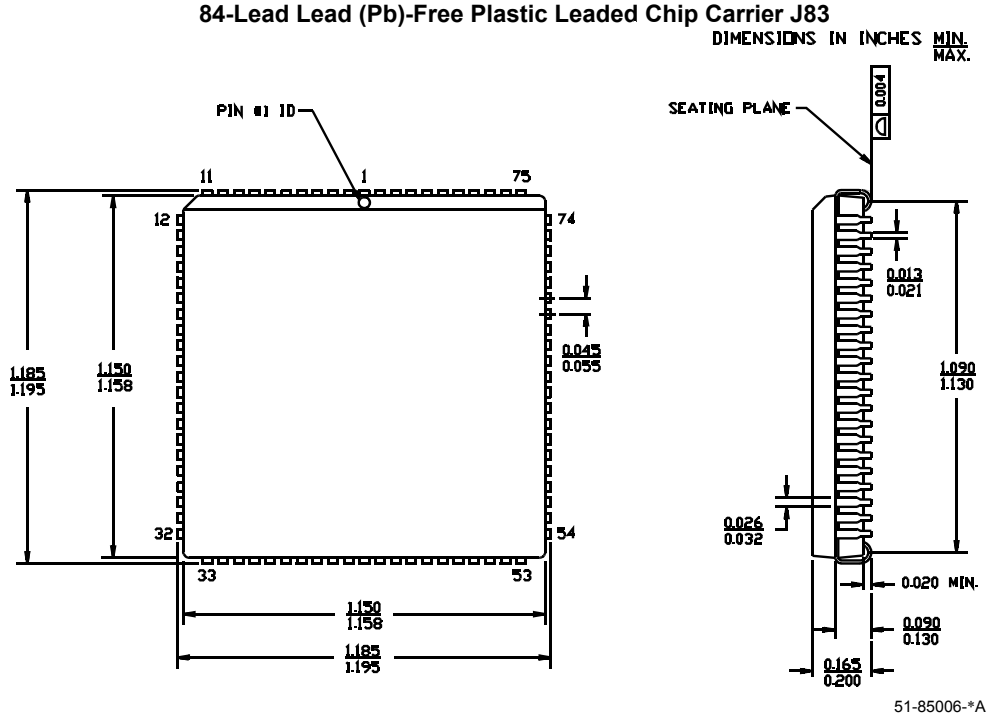


Package Diagrams (continued)

48-Ball (7.0 mm x 7.0 mm x 1.2 mm, 0.80 pitch) Thin BGA BA48D

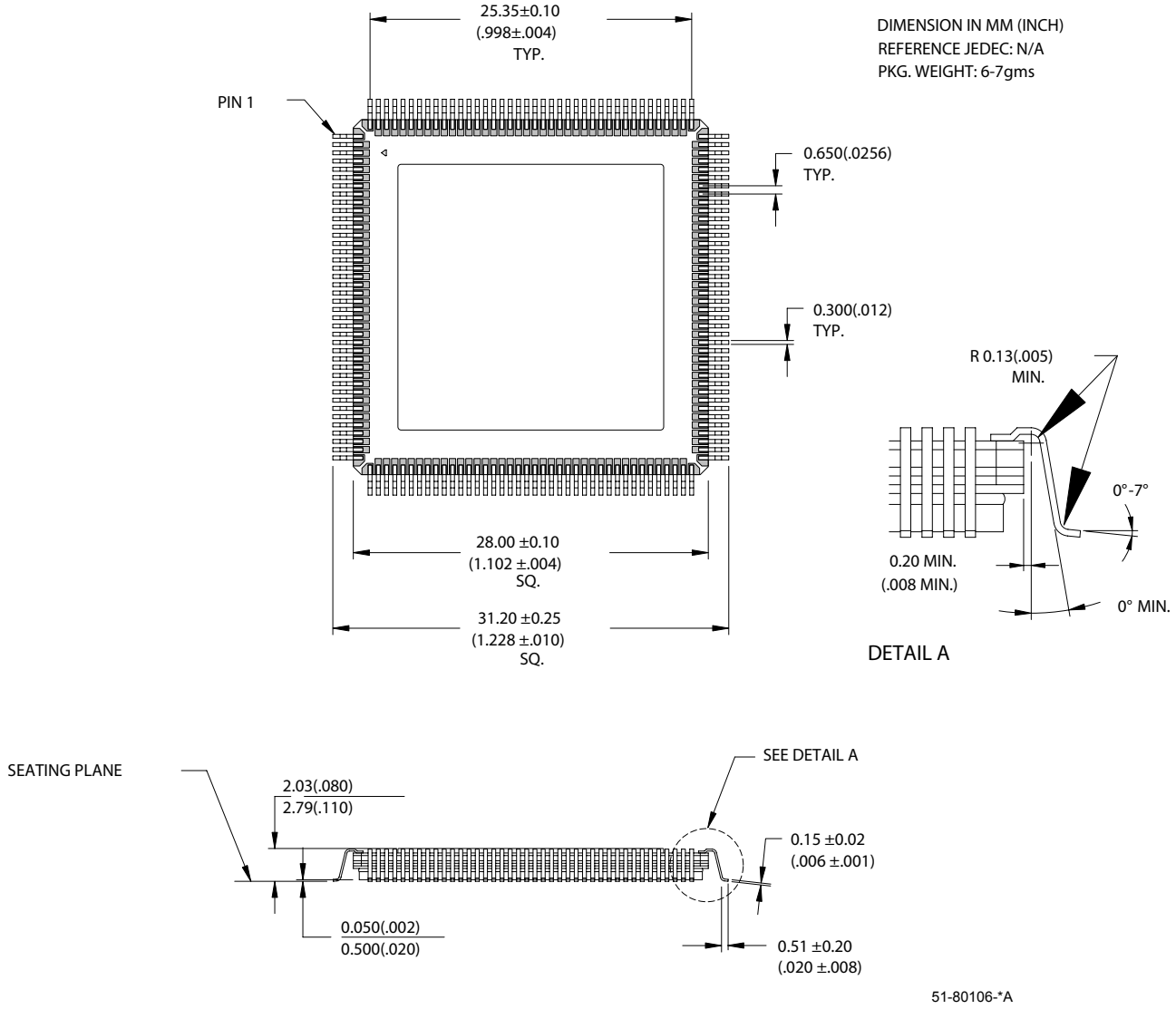


84-Lead Lead (Pb)-Free Plastic Leaded Chip Carrier J83



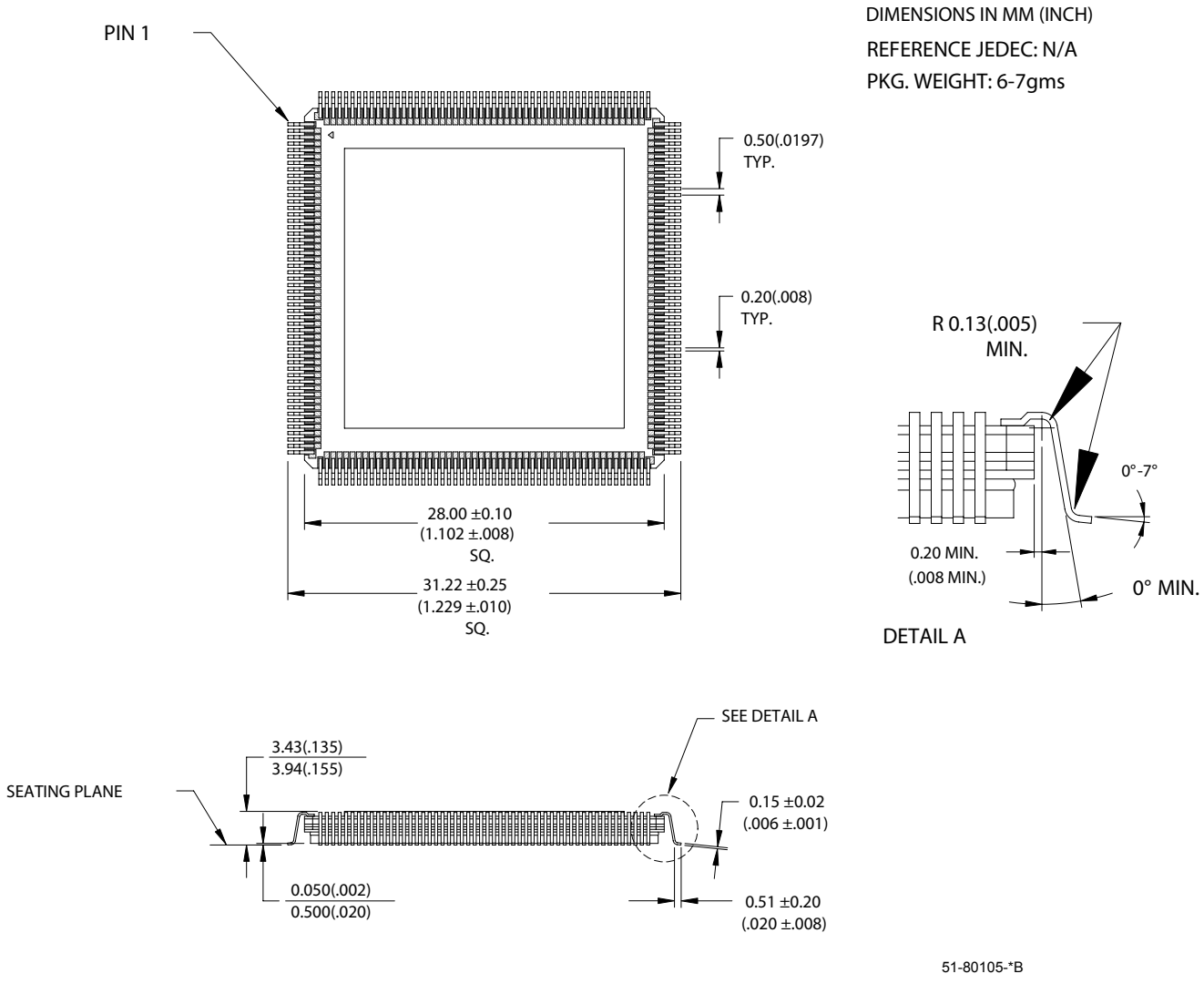
Package Diagrams (continued)

160-Lead Ceramic Quad Flatpack (Cavity Up) U162



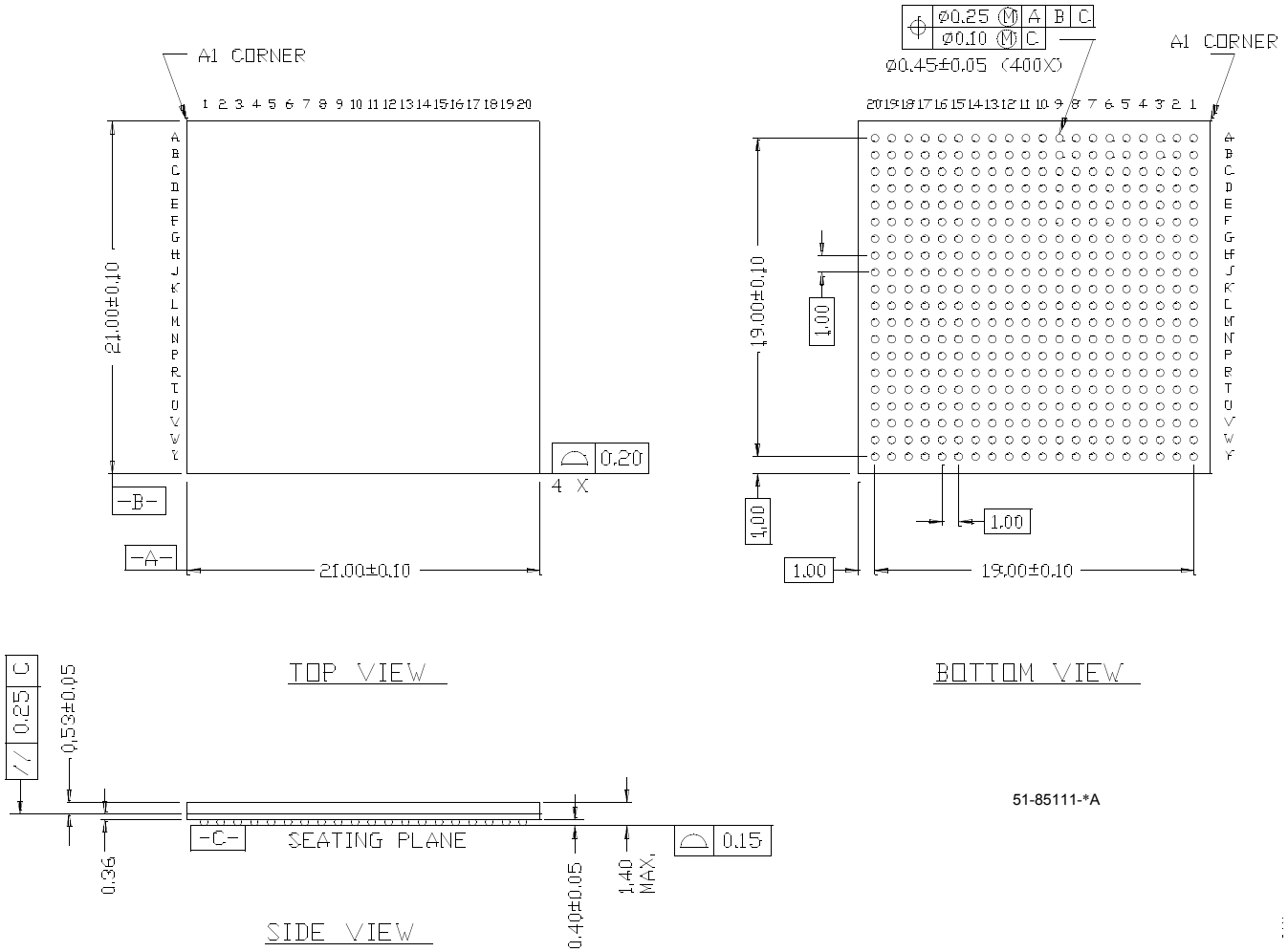
Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208



Package Diagrams (continued)

400-Ball FBGA (21 x 21 x 1.4 mm) BB400



Addendum

3.3V Operating Range

(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.16V

Document History Page

Document Title: Ultra37000 CPLD Family 5V, 3.3V, ISR™ High-Performance CPLDs Document Number: 38-03007				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106272	04/18/01	SZV	Change from Spec number: 38-00475 to 38-03007
*A	124942	03/21/03	OOR	Updated 3.3V V_{CC} requirements for –144 speeds Added an Addendum
*B	126262	05/09/03	TEH	Changed pinout for CY37128V BB100 package
*C	128125	07/16/03	HOM	Obsoleted following 3.3V PLCC packaged devices: CY37032VP44-143JC CY37032VP44-100JC CY37032VP44-100JI CY37064VP44-143JC CY37064VP84-143JC CY37064VP44-100JC CY37064VP84-100JC CY37064VP44-100JI CY37064VP84-100JI CY37128VP84-125JC CY37128VP84-83JC CY37128VP84-83JI
*D	282709	See ECN	YDT	Changed package diagrams and labels for consistency Added Lead (Pb)-free logo on first page, as well as a note in Features Added Lead (Pb)-free package diagram labels Added Lead-free Parts to Ordering Information CY37032P44-200AXC, CY37032P44-200JXC, CY37032P44-154AXI, CY37032P44-154JXI, CY37032P44-125AXC, CY37032P44-125JXC, CY37064P44-200AXC, CY37064P44-200JXC, CY37064P100-200AXC, CY37064P44-154AXI, CY37064P44-154JXI, CY37064P44-125AXC, CY37064P44-125JXC, CY37064P100-125AXC, CY37064P44-125AXI, CY37064P100-125AXI, CY37128P84-167JXC, CY37128P100-167AXC, CY37128P160-167AXC, CY37128P84-125JXC, CY37128P100-125AXC, CY37128P160-125AXC, CY37128P84-125JXI, CY37128P100-125AXI, CY37128P160-125AXI, CY37128P84-100JXC, CY37128P100-100AXC, CY37128P160-100AXC, CY37128P100-100AXI, CY37192P160-154AXC, CY37192P160-125AXC, CY37192P160-125AXI, CY37192P160-83AXC, CY37192P160-83AXI, CY37256P160-154AXC, CY37256P160-125AXC, CY37256P160-125AXI, CY37256P160-83AXC, CY37256P160-83AXI, CY37032VP44-143AXC, CY37032VP44-100AXC, CY37032VP44-100AXI, CY37032VP44-100JXI, CY37064VP44-143AXC, CY37064VP100-143AXC, CY37064VP44-100AXC, CY37064VP100-100AXC, CY37064VP44-100AXI, CY37064VP100-100AXI, CY37128VP100-125AXC, CY37128VP160-125AXC, CY37128VP160-125AXI, CY37128VP100-83AXC, CY37128VP160-83AXC, CY37128VP100-83AXI, CY37128VP160-83AXI, CY37192VP160-100AXC, CY37192VP160-66AXC, CY37256VP160-100AXC, CY37256VP160-100AXI, CY37256VP160-66AXC
*E	321635	See ECN	PCX	Added Package Diagram BG292 Updated all PBGA package type information (BG292 & BG388)