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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	26MHz
Connectivity	I²C, SCI
Peripherals	POR, PWM, WDT
Number of I/O	104
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2551fc26dv

The extended registers (E0 to E7) can be used as 16-bit registers, or as the upper 16-bit segments of 32-bit registers or address registers.

- Instruction Set

  All instructions and addressing modes can be used.

- Exception Vector Table and Memory Indirect Branch Addresses

  In advanced mode, the top area starting at H'00000000 is allocated to the exception vector table in units of 32 bits. In each 32 bits, the upper 8 bits are ignored and a branch address is stored in the lower 24 bits (figure 2.3). For details of the exception vector table, see section 4, Exception Handling.

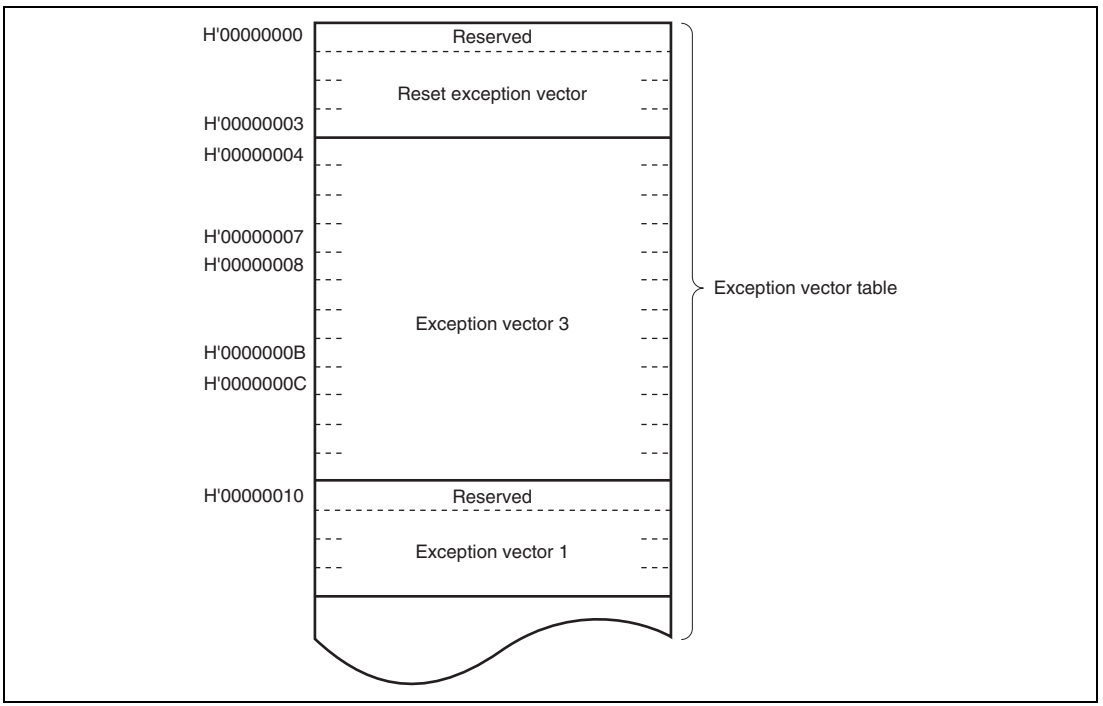


Figure 2.3 Exception Vector Table (Advanced Mode)

The memory indirect addressing mode (@@aa:8) employed in the JMP and JSR instructions uses an 8-bit absolute address included in the instruction code to specify a memory operand that contains a branch address. In advanced mode, the operand is a 32-bit longword operand, providing a 32-bit branch address. The upper 8 bits of these 32 bits is a reserved area that is regarded as H'00. Branch addresses can be stored in the area from H'00000000 to H'000000FF. Note that the first part of this range is also the exception vector table.

Table 4.4 State of CCR and EXR after Trace Exception Handling

	CCR		EXR	
Interrupt Control Mode	**I**	**UI**	**I2 to I0**	**T**
0	Trace exception handling cannot be used.			
2	1	—	—	0

Legend:
1: Set to 1
0: Cleared to 0
—: Retains value prior to execution

4.5 Interrupt Exception Handling

Interrupts are controlled by the interrupt controller. The interrupt controller has two interrupt control modes and can assign interrupts other than NMI to eight priority/mask levels to enable multiplexed interrupt control. For details, see section 5, Interrupt Controller.

Interrupt exception handling is conducted as follows:

1. The values in the program counter (PC), condition code register (CCR), and extended register (EXR) are saved to the stack.
2. The interrupt mask bit is updated and the T bit is cleared to 0.
3. A vector address corresponding to the interrupt source is generated, the start address is loaded from the vector table to the PC, and program execution begins from that address.

4.6 Trap Instruction Exception Handling

Trap instruction exception handling starts when a TRAPA instruction is executed. Trap instruction exception handling can be executed at all times in the program execution state.

Trap instruction exception handling is conducted as follows:

1. The values in the program counter (PC), condition code register (CCR), and extended register (EXR) are saved to the stack.
2. The interrupt mask bit is updated and the T bit is cleared to 0.
3. A vector address corresponding to the interrupt source is generated, the start address is loaded from the vector table to the PC, and program execution starts from that address.

Section 6 PC Break Controller (PBC)

The PC break controller (PBC) provides functions that simplify program debugging. Using these functions, it is easy to create a self-monitoring debugger, enabling programs to be debugged with the chip alone, without using an in-circuit emulator. A block diagram of the PC break controller is shown in figure 6.1.

6.1 Features

- Two break channels (A and B)
- 24-bit break address
  - — Bit masking possible
- Four types of break compare conditions
  - — Instruction fetch
  - — Data read
  - — Data write
  - — Data read/write
- Bus master
  - — Either CPU or CPU/DTC can be selected
- The timing of PC break exception handling after the occurrence of a break condition is as follows:
  - — Immediately before execution of the instruction fetched at the set address (instruction fetch)
  - — Immediately after execution of the instruction that accesses data at the set address (data access)
- Module stop mode can be set

7.5 Basic Timing

The CPU is driven by a system clock, denoted by the symbol ϕ. The period from one rising edge of ϕ to the next is referred to as a "state." The memory cycle or bus cycle consists of one, two, or three states. Different methods are used to access on-chip memory, on-chip peripheral modules, and the external address space.

7.5.1 On-Chip Memory (ROM, RAM) Access Timing

On-chip memory is accessed in one state. The data bus width is 16 bits, enabling both byte and word transfer. Figure 7.4 shows the on-chip memory access cycle. Figure 7.5 shows the pin states.

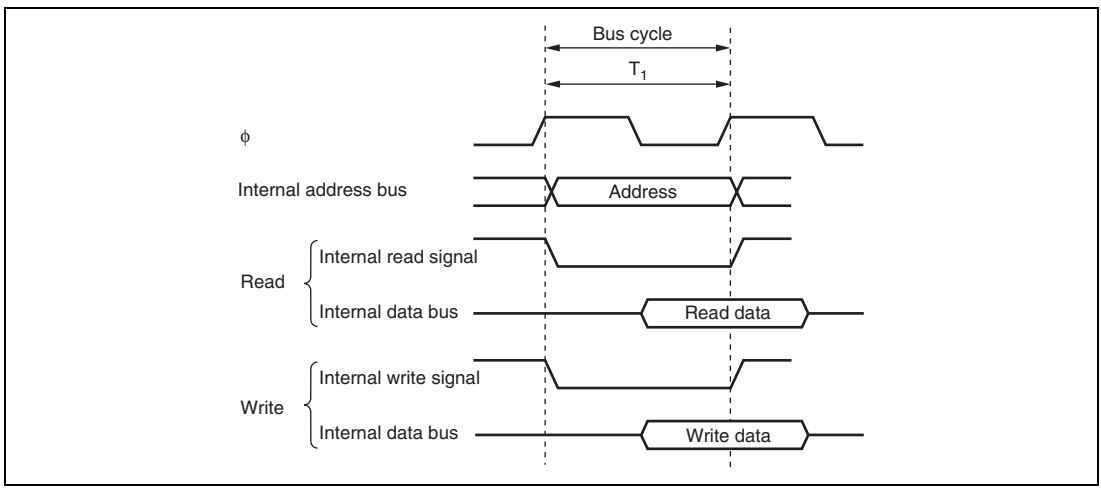


Figure 7.4 On-Chip Memory Access Cycle

9.2.2 Port 2 Data Register (P2DR)

P2DR stores output data for port 2 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P27DR	0	R/W	Output data for a pin is stored when the pin is specified as a general purpose output port.
6	P26DR	0	R/W	
5	P25DR	0	R/W	
4	P24DR	0	R/W	
3	P23DR	0	R/W	
2	P22DR	0	R/W	
1	P21DR	0	R/W	
0	P20DR	0	R/W	

9.2.3 Port 2 Register (PORT2)

PORT2 shows port 2 pin states. This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	P27	—*	R	If a port 2 read is performed while P2DDR bits are set to 1, the P2DR values are read. If a port 2 read is performed while P2DDR bits are cleared to 0, the pin states are read.
6	P26	—*	R	
5	P25	—*	R	
4	P24	—*	R	
3	P23	—*	R	
2	P22	—*	R	
1	P21	—*	R	
0	P20	—*	R	

Note: * Determined by the states of pins P27 to P20.

- P33/TxD1/SCL1

  The pin function is switched as shown below according to the combination of the ICE bit in ICCR1_1 of IIC2_1, the TE bit in SCR_1 of SCI_1, and the P33DDR bit.

ICE	0			1
TE	0		1	—
P33DDR	0	1	—	—
Pin function	P33 input	P33 output*	TxD1 output*	SCL1 input/output

Note: * When P33ODR is set to 1, this pin functions as NMOS open drain output.

- P32/SCK0/SDA1/$\overline{\text{IRQ4}}$

  The pin function is switched as shown below according to the combination of the ICE bit in ICCR1_1 of IIC2_1, the C/$\overline{\text{A}}$ bit in SMR_0 of SCI_0, the CKE0 and CKE1 bits in SCR_0, and the P32DDR bit.

ICE	0					1
CKE1	0				1	—
C/$\overline{\text{A}}$	0			1	—	—
CKE0	0		1	—	—	—
P32DDR	0	1	—	—	—	—
Pin function	P32 input	P32 output*[1]	SCK0 output*[1]	SCK0 output*[1]	SCK0 input	SDA1 input/ output
	$\overline{\text{IRQ4}}$ Input*[2]					

Notes: 1. When P32ODR is set to 1, this pin functions as NMOS open drain output.
2. When this pin is used as an external interrupt pin, do not specify other functions.

- P31/RxD0

  The pin function is switched as shown below according to the combination of the RE bit in SCR_0 of SCI_0 and the P31DDR bit.

RE	0		1
P31DDR	0	1	—
Pin function	P31 input	P31 output*	RxD0 input

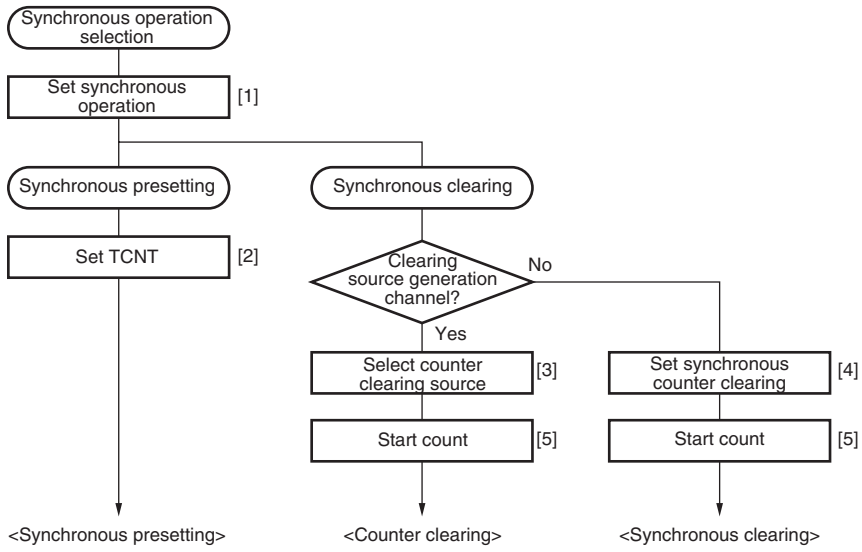
Note: * When P31ODR is set to 1, this pin functions as NMOS open drain output.

Table 10.18 TIOR_4

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_4 Function**	**TIOCB4 Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCB4 pin Input capture at rising edge
			1		Capture input source is TIOCB4 pin Input capture at falling edge
		1	X		Capture input source is TIOCB4 pin Input capture at both edges
	1	X	X		Capture input source is TGRC_3 compare match/input capture Input capture at generation of TGRC_3 compare match/input capture

Legend:

X: Don’t care



[1] Set to 1 the SYNC bits in TSYR corresponding to the channels to be designated for synchronous operation.
[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.
[3] Use the CCLR2 to CCLR0 bits in TCR to specify TCNT clearing by input capture/output compare, etc.
[4] Use the CCLR2 to CCLR0 bits in TCR to designate synchronous clearing for the counter clearing source.
[5] Set to 1 the CST bits in TSTR for the relevant channels, to start the count operation.

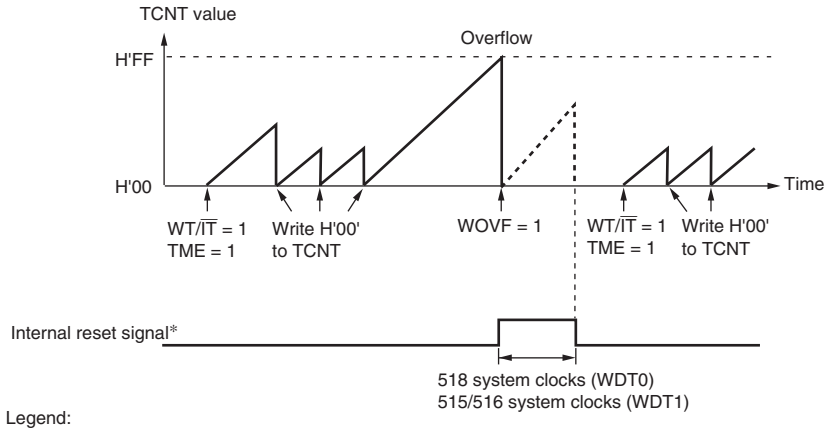
Figure 10.10 Example of Synchronous Operation Setting Procedure

Example of Synchronous Operation: Figure 10.11 shows an example of synchronous operation.

In this example, synchronous operation and PWM mode 1 have been designated for channels 0 to 2, TGRB_0 compare match has been set as the channel 0 counter clearing source, and synchronous clearing has been set for the channel 1 and 2 counter clearing source.

Three-phase PWM waveforms are output from pins TIOCA0, TIOCA1, and TIOCA2. At this time, synchronous presetting, and synchronous clearing by TGRB_0 compare match, are performed for channel 0 to 2 TCNT counters, and the data set in TGRB_0 is used as the PWM cycle.

For details of PWM modes, see section 10.4.5, PWM Modes.



Legend:
WT/$\overline{IT}$: Timer mode select bit
TME: Timer enable bit
WOVF: Overflow flag

Note: * In the case of WDT_0, the internal reset signal is generated only when the RSTE bit is set to 1.
In the case of WDT_1, either the internal reset or the NMI interrupt is generated.

Figure 12.2 Watchdog Timer Mode Operation

12.4.2 Interval Timer Mode

To use the WDT as an internal timer, set the WT/$\overline{IT}$ bit in TCSR to 0 and the TME bit to 1.

When the WDT is used as an interval timer, an interval timer interrupt (WOVI) is generated each time the TCNT overflows. (The NMI interrupt request is not generated.) Therefore, an interrupt can be generated at specified times.

15.2 Input/Output Pins

Table 15.1 summarizes the input pins used by the A/D converter. The 16 analog input pins (AN0 to AN15) are divided into four groups each of which consists of two channels; analog input pins 0 to 7 (AN0 to AN7) comprising channel set 0, analog input pins 8 to 15 (AN8 to AN15) comprising channel set 1, analog input pins 0 to 3, 8 to 11 (AN0 to AN3, AN8 to AN11) comprising group 0, and analog input pins 4 to 7, 12 to 15 (AN4 to AN7, AN12 to AN15) comprising group 1. The AVcc and AVss pins are the power supply pins for the analog block in the A/D converter. The Vref pin is the A/D conversion reference voltage pin.

Table 15.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog block power supply pin
Analog ground pin	AV_{SS}	Input	Analog block ground and reference voltage
Reference voltage pin	Vref	Input	Reference voltage for A/D conversion
Analog input pin 0	AN0	Input	Channel set 0 (CH3 = 0), group 0 analog input pins
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	Channel set 0 (CH3 = 0), group 1 analog input pins
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
Analog input pin 8	AN8	Input	Channel set 1 (CH3 = 1), group 0 analog input pins
Analog input pin 9	AN9	Input	
Analog input pin 10	AN10	Input	
Analog input pin 11	AN11	Input	
Analog input pin 12	AN12	Input	Channel set 1 (CH3 = 1), group 1 analog input pins
Analog input pin 13	AN13	Input	
Analog input pin 14	AN14	Input	
Analog input pin 15	AN15	Input	
A/D external trigger input	$\overline{\text{ADTRG}}$	Input	External trigger input pin for starting A/D conversion

must be enabled. If an error termination interrupt is disabled, no interrupt is generated even if the transmission is terminated by an error.

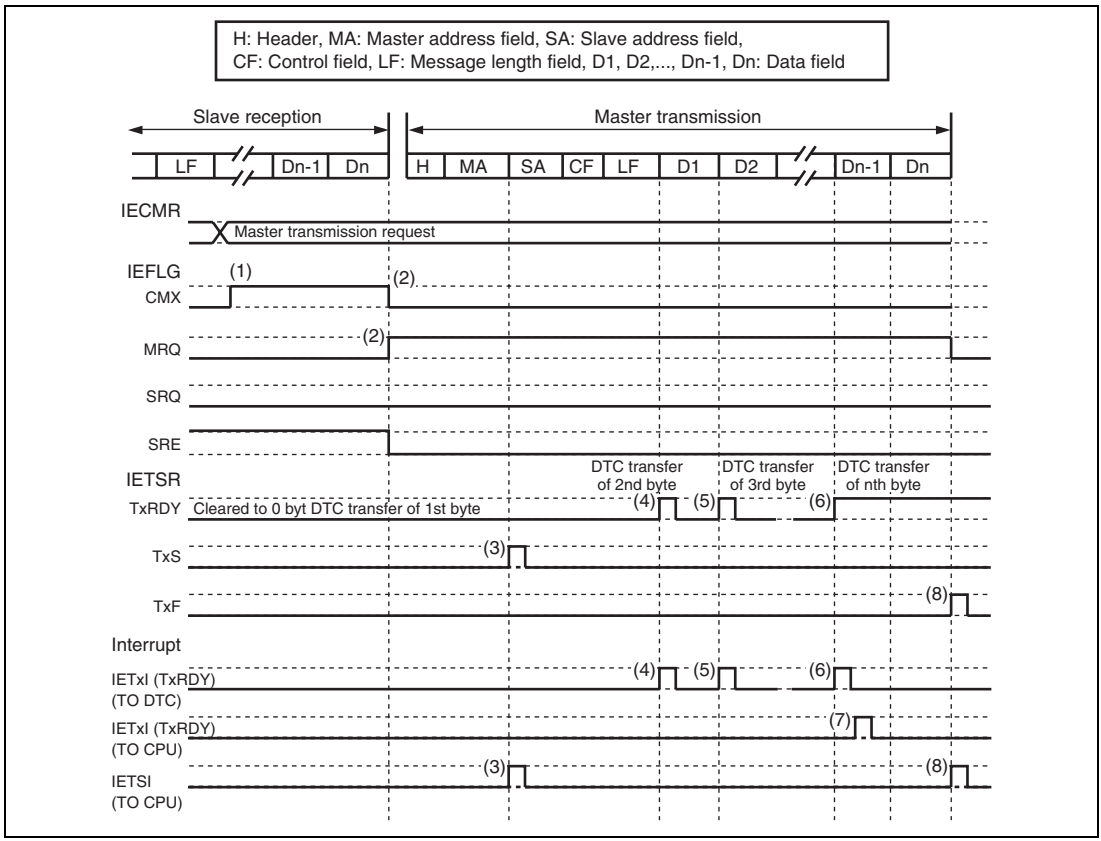


Figure 17.8 Master Transmit Operation Timing

17.4.2 Slave Receive Operation

This section describes an example of performing a slave reception using the DTC.

(1) IEB Initialization

(a) Setting the IEBus Control Register (IECTR)

Enable the IEBus pins, select the signal polarity, and select a clock supplied to the IEB. Set the RE bit to 1 to perform reception. The LUEE bit does not need to be specified.

(b) Setting the IEBus Master Unit Address Registers 1 and 2 (IEAR1 and IEAR2)

18.3.7 Transmit Acknowledge Register (TXACK)

TXACK is a status register that indicates the normal transmission of mailbox (buffer) transmit messages.

Bit	Bit Name	Initial Value	R/W	Description
15	TXACK7	0	R/(W)*	These bits are status flags that indicate error-free transmission of the transmit message in the corresponding mailboxes 1 to 15. When the message in mailbox n (n = 1 to 15) has been transmitted error-free, TXACKn is set to 1. [Setting condition] • Completion of message transmission for corresponding mailbox [Clearing condition] • Writing 1 Bit 8 is reserved. This bit is always read as 0 and the write value should always be 0.
14	TXACK6	0	R/(W)*	
13	TXACK5	0	R/(W)*	
12	TXACK4	0	R/(W)*	
11	TXACK3	0	R/(W)*	
10	TXACK2	0	R/(W)*	
9	TXACK1	0	R/(W)*	
8	—	0	R	
7	TXACK15	0	R/(W)*	
6	TXACK14	0	R/(W)*	
5	TXACK13	0	R/(W)*	
4	TXACK12	0	R/(W)*	
3	TXACK11	0	R/(W)*	
2	TXACK10	0	R/(W)*	
1	TXACK9	0	R/(W)*	
0	TXACK8	0	R/(W)*	

Note: * Only 1 can be written to this bit for clearing the flag.

20.1.4 Flash MAT Configuration

This LSI's flash memory is configured by the 512-kbyte (H8S/2556, H8S/2552, and H8S/2506) or 384-kbyte (H8S/2551 and H8S/2505) user MAT and 8-kbyte user boot MAT.

The start address is allocated to the same address in the user MAT and user boot MAT. Therefore, when the program execution or data access is performed between two MATs, the MAT must be switched by using FMATS register.

The user MAT or user boot MAT can be read in all modes. However, the user boot MAT can be programmed only in boot mode and programmer mode.

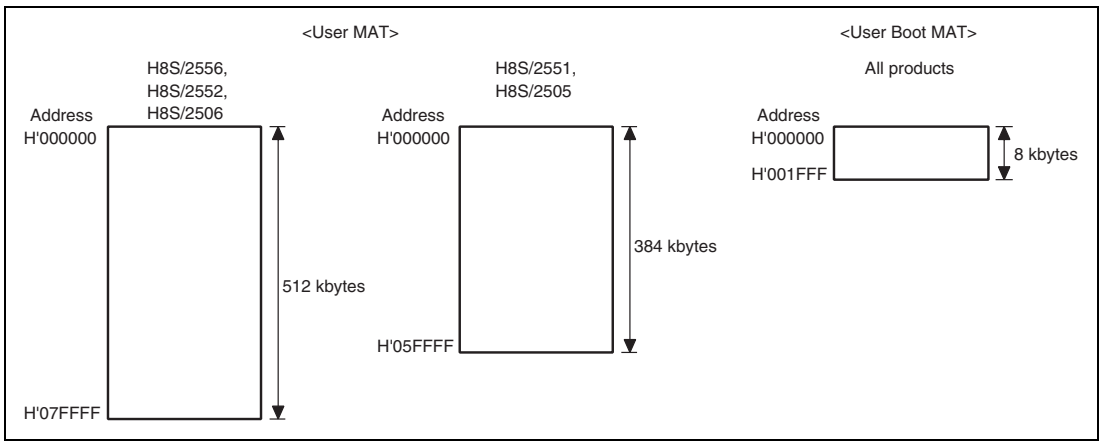


Figure 20.3 Flash Memory Configuration

The size of the user MAT is different from that of the user boot MAT. An address which exceeds the size of the 8-kbyte user boot MAT should not be accessed. If the attempt is made, data is read as undefined value.

Bit	Bit Name	Initial Value	R/W	Description
1	STC1	0	R/W	Multiplication Ratio Setting
0	STC0	0	R/W	Specify multiplication ratio of the PLL circuit. The specified multiplication ratio becomes valid after software standby mode or watch mode is entered. A setting of STC1 = 0 must be used in this LSI. 00: x 1 01: x 2 10: Setting prohibited 11: Setting prohibited

Note: * When watch mode is entered, high-speed mode must be set.

4. The clock pulse generator stops, and the setting for the STC1 and STC0 bits becomes valid.
5. Software standby mode or watch mode is exited, and the transition time set by the STS2 to STS0 bits is ensured.
6. After the set transition time is elapsed, this LSI resumes operation with the changed multiplication ratio.

When the STCS bit is set to 1, after rewriting the STC1 and STC0 bits, this LSI operates with the changed multiplication ratio.

21.4 Medium-Speed Clock Divider

The medium-speed clock divider divides the system clock to generate ϕ/2, ϕ/4, ϕ/8, ϕ/16, and ϕ/32.

21.5 Bus Master Clock Selection Circuit

The bus master clock selection circuit selects the clock supplied to the bus master by setting the SCK2 to SCK0 bits in SCKCR. The bus master clock can be selected from system clock (ϕ), or medium-speed clocks (ϕ/2, ϕ/4, ϕ/8, ϕ/16, and ϕ/32).

21.6 System Clock with IEBus

When using the IEBus*[1], the system clock should be set with one of 12 MHz, 12.58 MHz, 18 MHz, 18.87 MHz, 24 MHz, or 25.16 MHz.

When the IEBus*[1] is not used, any system clock frequency between 8 MHz and 26 MHz*[2] can be used.

Notes: 1. The IEBus is supported only by the H8S/2552 Group.
2. System clock frequency up to 20 MHz is supported by the H8S/2556 Group.

21.7.2 Handling Pins when Subclock Is Not Used

If no subclock is required, connect the OSC1 pin to Vss and leave the OSC2 pin open, as shown in figure 21.10. The SUBSTP bit in LPWRCR must be set to 1.

If the SUBSTP bit is not set to 1, transitions to the power-down mode may not complete normally.

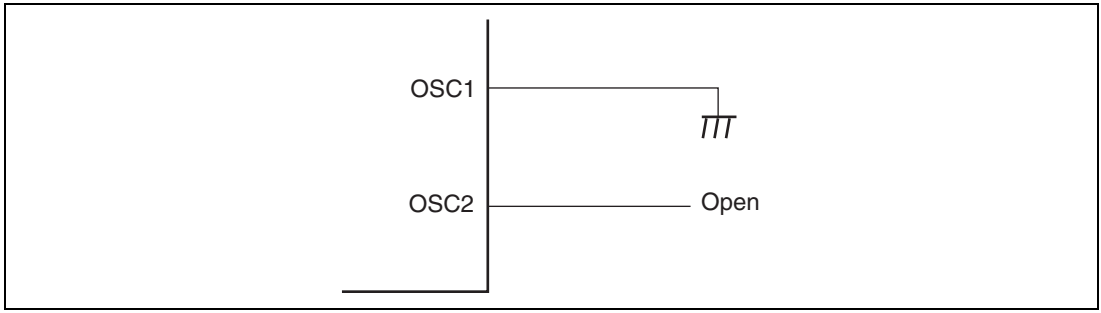


Figure 21.10 Pin Handling when Subclock Is Not Used

21.8 Subclock Waveform Generation Circuit

To eliminate noise from the subclock input from the OSC1 pin, the subclock is sampled using the dividing clock ϕ. The sampling frequency is set using the NESEL bit in LPWRCR. For details, see section 21.1.2, Low-Power Control Register (LPWRCR).

No sampling is performed in watch mode.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
LAFMH	LAFMH7	LAFMH6	LAFMH5	—	—	—	LAFMH1	LAFMH0	HCAN
	LAFMH15	LAFMH14	LAFMH13	LAFMH12	LAFMH11	LAFMH10	LAFMH9	LAFMH8	
MC0[1]	—	—	—	—	DLC3	DLC2	DLC1	DLC0	
MC0[2]	—	—	—	—	—	—	—	—	
MC0[3]	—	—	—	—	—	—	—	—	
MC0[4]	—	—	—	—	—	—	—	—	
MC0[5]	ID-20	ID-19	ID-18	RTR	IDE	—	ID-17	ID-16	
MC0[6]	ID-28	ID-27	ID-26	ID-25	ID-24	ID-23	ID-22	ID-21	
MC0[7]	ID-7	ID-6	ID-5	ID-4	ID-3	ID-2	ID-1	ID-0	
MC0[8]	ID-15	ID-14	ID-13	ID-12	ID-11	ID-10	ID-9	ID-8	
MC1[1]	—	—	—	—	DLC3	DLC2	DLC1	DLC0	
MC1[2]	—	—	—	—	—	—	—	—	
MC1[3]	—	—	—	—	—	—	—	—	
MC1[4]	—	—	—	—	—	—	—	—	
MC1[5]	ID-20	ID-19	ID-18	RTR	IDE	—	ID-17	ID-16	
MC1[6]	ID-28	ID-27	ID-26	ID-25	ID-24	ID-23	ID-22	ID-21	
MC1[7]	ID-7	ID-6	ID-5	ID-4	ID-3	ID-2	ID-1	ID-0	
MC1[8]	ID-15	ID-14	ID-13	ID-12	ID-11	ID-10	ID-9	ID-8	
MC2[1]	—	—	—	—	DLC3	DLC2	DLC1	DLC0	
MC2[2]	—	—	—	—	—	—	—	—	
MC2[3]	—	—	—	—	—	—	—	—	
MC2[4]	—	—	—	—	—	—	—	—	
MC2[5]	ID-20	ID-19	ID-18	RTR	IDE	—	ID-17	ID-16	
MC2[6]	ID-28	ID-27	ID-26	ID-25	ID-24	ID-23	ID-22	ID-21	
MC2[7]	ID-7	ID-6	ID-5	ID-4	ID-3	ID-2	ID-1	ID-0	
MC2[8]	ID-15	ID-14	ID-13	ID-12	ID-11	ID-10	ID-9	ID-8	
MC3[1]	—	—	—	—	DLC3	DLC2	DLC1	DLC0	
MC3[2]	—	—	—	—	—	—	—	—	
MC3[3]	—	—	—	—	—	—	—	—	
MC3[4]	—	—	—	—	—	—	—	—	
MC3[5]	ID-20	ID-19	ID-18	RTR	IDE	—	ID-17	ID-16	

Item	Page	Revision (See Manual for Details)
Table 20.9 (4) Useable Area for Erasure in User Boot Mode	724	Table amended

	Storable/Executable Area		Selected MAT		
Item	On-ChipRAM	User Boot MAT	User MAT	User Boot MAT	Embedded Program Storage Area
Operation for Selection of On-chip Program to be Downloaded	○	○		○	
Operation for Writing H'A5 to FKEY	○	○		○	
Execution of Writing SCO = 1 to FCCS (Download)	○	×			○
Operation for FKEY Clear	○	○		○	
Determination of Download Result	○	○		○	
Operation for Download Error	○	○		○	
Operation for Settings of Initial Parameter	○	○		○	
Execution of Initialization	○	×		○	
Determination of Initialization Result	○	○		○	
Operation for Initialization Error	○	○		○	
NMI Handling Routine	○	×		○	
Operation for Interrupt Inhibit	○	○		○	
Switching MATs by FMATS	○	×	○		
Operation for Writing H'5A to FKEY	○	×	○		

	725	Table amended

	Storable/Executable Area		Selected MAT		
Item	On-Chip RAM	User Boot MAT	User MAT	User Boot MAT	Embedded Program Storage Area
Operation for Settings of Erasure Parameter	○	×	○		
Execution of Erasure	○	×	○		
Determination of Erasure Result	○	×	○		
Operation for Erasure Error	○	×*	○		
Operation for FKEY Clear	○	×	○		
Switching MATs by FMATS	○	×		○	