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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	26MHz
Connectivity	I²C, SCI
Peripherals	POR, PWM, WDT
Number of I/O	104
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2552fc26dv

Contents

1.3.3 Pin Functions

Table 1.2 lists the pins functions in each mode.

Table 1.2 Pin Functions

		Pin No.			
Type	Symbol	FP-144J, FP-144JV	BP-176V※2	I/O	Function
Power supply	Vcc	96	F14	I	Power supply pin. Connect this pin to the system power supply.
	P1Vcc	14, 84	F3, G3, G4, H3, H4, K12	I	Power supply pin for ports indicated that its power is supplied by P1Vcc (see table 1.1).
	P2Vcc	118	C9, C10, D9, D10	I	Pins for connecting a capacitor to stabilize the internal step-down voltage. Power supply pin for ports indicated that its power is supplied by P2Vcc (see table 1.1).
	VCL	88	J13	O	Pin for connecting the on-chip step-down power supply to a capacitor for voltage stabilization. Must not be directly connected to a power supply. A capacitor of 0.47 μF must be connected between this pin and Vss. (Place close to the pin.)
	VSS	12, 54, 86, 94, 117	G2, G1, F2, F1, E1, R7, R6, P8, P7, K15, K14, H15, H14, G14, G13, G12, F13, F12, B10, A14, A13, A12, A11, A10	I	Ground pins. Connect this pin to the system power supply (0V).
Clock	XTAL	93	G15	I	For connection to a crystal resonator. For examples of connecting crystal resonator and external clock input, see section 21, Clock Pulse Generator.
	EXTAL	95	F15	I	For connection to a crystal resonator or a ceramic resonator. This pin can be also used for external clock input. For examples of connecting crystal resonator and external clock input, see section 21, Clock Pulse Generator.

2.9 Usage Notes

2.9.1 TAS Instruction

Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction. The TAS instruction is not generated by the H8S and H8/300 Series C/C++ compilers. If the TAS instruction is used as a user-defined intrinsic function, ensure that only register ER0, ER1, ER4, or ER5 is used.

2.9.2 STM/LDM Instruction

With the STM or LDM instruction, the ER7 register is used as the stack pointer, and thus cannot be used as a register that allows save (STM) or restore (LDM) operation.

With a single STM or LDM instruction, two to four registers can be saved or restored. The available registers are as follows:

For two registers: ER0 and ER1, ER2 and ER3, or ER4 and ER5

For three registers: ER0 to ER2, or ER4 to ER6

For four registers: ER0 to ER3

For the H8S or H8/300 Series C/C++ Compiler, the STM/LDM instruction including ER7 is not created.

2.9.3 Bit Manipulation Instructions

When bit-manipulation is used with registers that include write-only bits, bits to be manipulated may not be manipulated properly or bits unrelated to the bit-manipulation may be changed.

Some values read from write-only bits are fixed and some are undefined. When such bits are the operands of bit-manipulation instructions that use read values in arithmetic operations (BNOT, BTST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD), the desired bit-manipulation will not be executed.

Also, bit-manipulation instructions that write back data according to the results of arithmetic operations (BSET, BCLR, BNOT, BST, BIST) may change bits that are not related to the bit-manipulation. Therefore, special care is necessary when using these instructions with registers that include write-only bits.

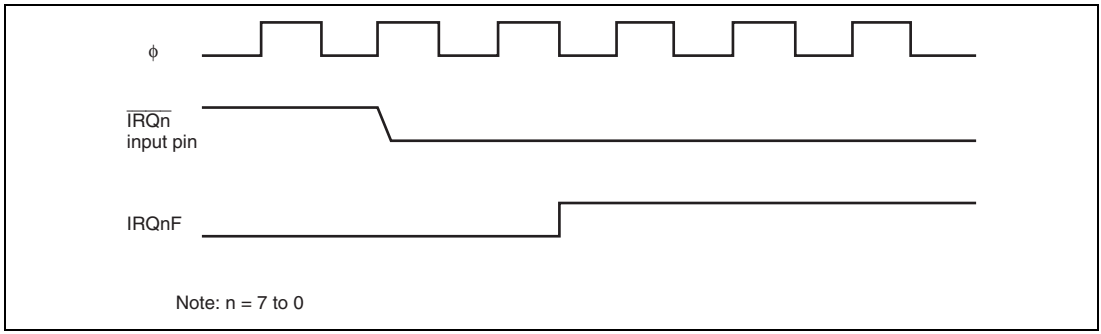

Figure 5.3 Set Timing for IRQ7F to IRQ0F

The detection of IRQ7 to IRQ0 interrupts does not depend on whether the relevant pin has been set for input or output. However, when a pin is used as an external interrupt input pin, do not clear the corresponding DDR to 0 to use the pin as an I/O pin for another function. The IRQ7F to IRQ0F interrupt request flags can be set to 1 when the setting condition is satisfied, regardless of IER settings. Accordingly, refer to only necessary flags.

5.4.2 Internal Interrupts

For each on-chip peripheral module, there are flags that indicate the interrupt request status, and enable bits that select enabling or disabling of these interrupts. If both of these are set to 1 for a particular interrupt source, an interrupt request is sent to the interrupt controller.

5.4.3 Interrupt Exception Handling Vector Table

Table 5.2 shows interrupt exception handling sources, vector addresses, and interrupt priorities. For default priorities, the lower the vector number, the higher the priority.

Priorities among modules can be set by means of the IPR. Modules set at the same priority will conform to their default priorities. Priorities within a module are fixed.

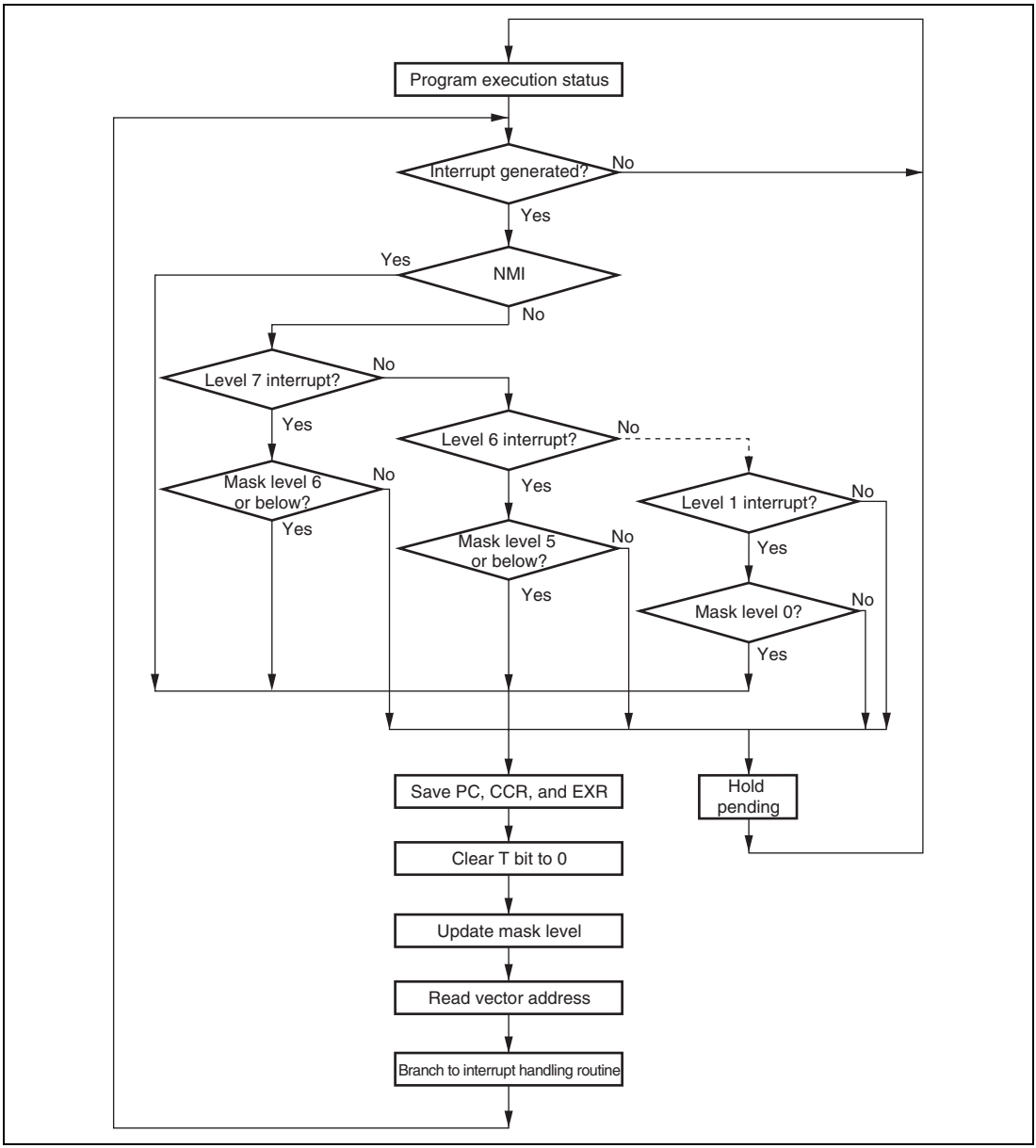

Figure 5.6 Flowchart of Procedure up to Interrupt Acceptance in Interrupt Control Mode 2

9.13.4 Pin Functions

Port F pins also function as bus control I/O pins, interrupt input pins, system clock output pins, A/D trigger input pins, and BUZZ output pins. Port F pin functions are shown below.

- PF7/ϕ

  The pin function is switched as shown below according to the PF7DDR bit.

PF7DDR	0	1
Pin function	PF7 input	ϕ output

- PF6/$\overline{AS}$

  The pin function is switched as shown below according to the combination of the operating mode and the PF6DDR bit.

Operating mode	Mode 6	Mode 7	
PF6DDR	—	0	1
Pin function	$\overline{AS}$ output	PF6 input	PF6 output

- PF5/$\overline{RD}$

  The pin function is switched as shown below according to the combination of the operating mode and the PF5DDR bit.

Operating mode	Mode 6	Mode 7	
PF5DDR	—	0	1
Pin function	$\overline{RD}$ output	PF5 input	PF5 output

- PF4/$\overline{HWR}$

  The pin function is switched as shown below according to the combination of the operating mode and the PF4DDR bit.

Operating mode	Mode 6	Mode 7	
PF4DDR	—	0	1
Pin function	$\overline{HWR}$ output	PF4 input	PF4 output

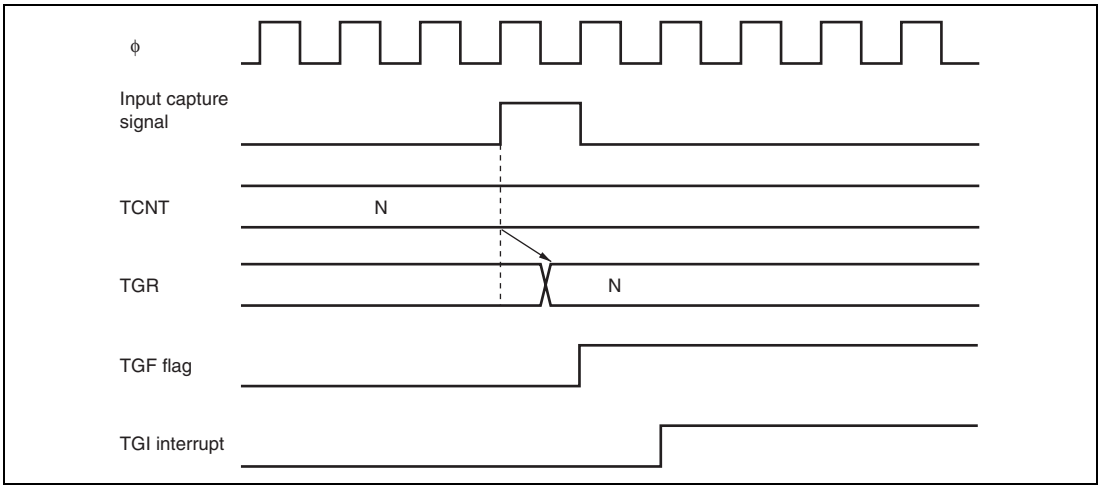

Figure 10.39 TGI Interrupt Timing (Input Capture)

TCFV Flag/TCFU Flag Setting Timing: Figure 10.40 shows the timing for setting of the TCFV flag in TSR on overflow, and TCIV interrupt request signal timing.

Figure 10.41 shows the timing for setting of the TCFU flag in TSR on underflow, and TCIU interrupt request signal timing.

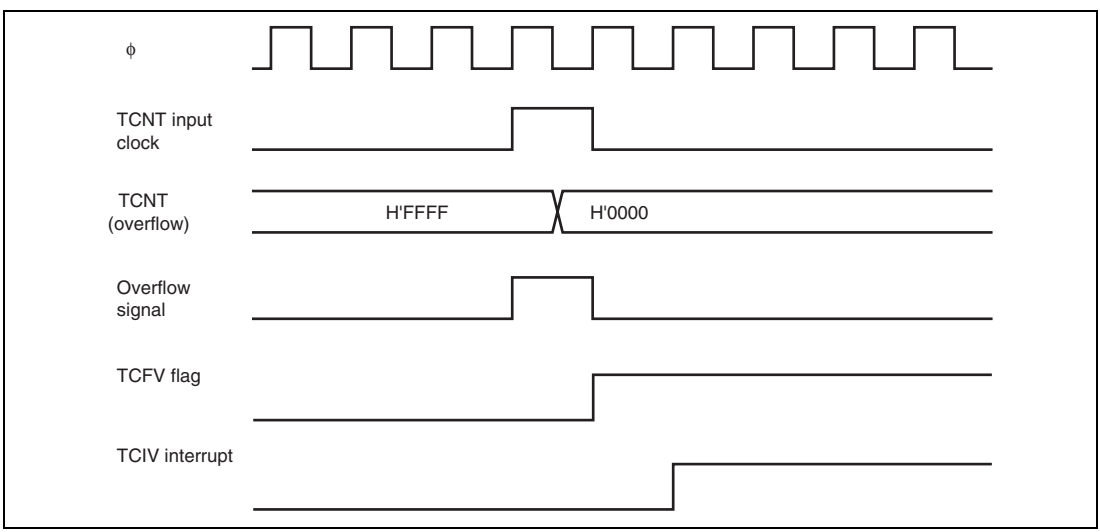

Figure 10.40 TCIV Interrupt Setting Timing

Bit	Bit Name	Initial Value	R/W	Description
5	OVF	0	R/(W)*	Timer Overflow Flag [Setting condition] When TCNT overflows from H'FF to H'00 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
4	—	0	R/W	Reserved This bit is a readable/writable bit, but the write value should always be 0.
3	OS3	0	R/W	Output Select 3 and 2 These bits specify how the timer output level is to be changed by a compare-match B of TCORB and TCNT. 00: No change when compare-match B occurs 01: 0 is output when compare-match B occurs 10: 1 is output when compare-match B occurs 11: Output is inverted when compare-match B occurs (toggle output)
2	OS2	0	R/W	
1	OS1	0	R/W	Output Select 1 and 0 These bits specify how the timer output level is to be changed by a compare-match A of TCORA and TCNT. 00: No change when compare-match A occurs 01: 0 is output when compare-match A occurs 10: 1 is output when compare-match A occurs 11: Output is inverted when compare-match A occurs (toggle output)
0	OS0	0	R/W	

Note: * Only 0 can be written to this bit, to clear the flag.

11.5.6 Timing of Overflow Flag (OVF) Setting

OVF in TCSR is set to 1 when the timer count overflows (changes from H'FF to H'00). Figure 11.9 shows the timing of this operation.

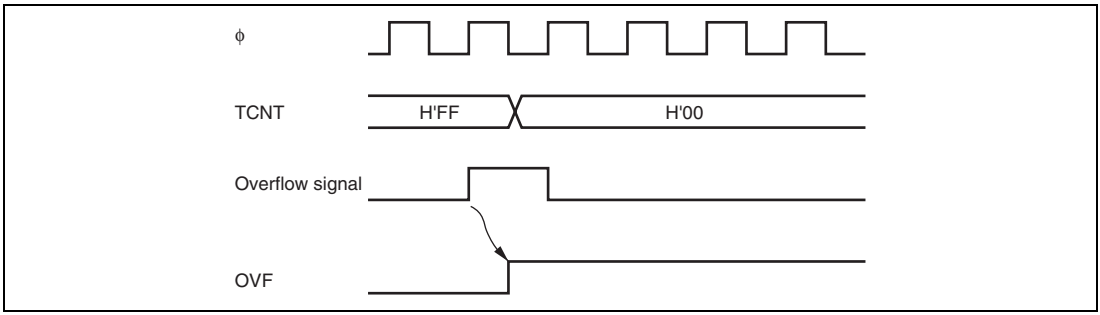

Figure 11.9 Timing of OVF Setting

13.3.6 Serial Control Register (SCR)

SCR is a register that enables or disables SCI transfer operations and interrupt requests, and is also used to selection of the transfer clock source. For details on interrupt requests, see section 13.8, Interrupt Sources. Some bit functions of SCR differ between normal serial communication interface mode and Smart Card interface mode.

- Normal Serial Communication Interface Mode (When SMIF in SCMR Is 0)

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, the TXI interrupt request is enabled. TXI interrupt request cancellation can be performed by reading 1 from the TDRE flag in SSR, then clearing it to 0, or clearing the TIE bit to 0.
6	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrupt requests are enabled. RXI and ERI interrupt request cancellation can be performed by reading 1 from the RDRF, FER, PER, or ORER flag in SSR, then clearing the flag to 0, or clearing the RIE bit to 0.
5	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0. SMR setting must be performed to decide the transfer format before setting the TE bit to 1. When this bit is cleared to 0, the transmission operation is disabled, and the TDRE flag is fixed at 1.

- As with the normal Smart Card interface, the ERS flag indicates the error signal status, but since error signal transfer is not performed, this flag is always cleared to 0.

Note: etu: Elementary time unit (time for transfer of 1 bit)

13.7.4 Receive Data Sampling Timing and Reception Margin

In Smart Card interface mode an internal clock generated by the on-chip baud rate generator can only be used as a transmission/reception clock. In this mode, the SCI operates on a basic clock with a frequency of 32, 64, 372, or 256 times the transfer rate (fixed to 16 times in normal asynchronous mode) as determined by bits BCP1 and BCP0. In reception, the SCI samples the falling edge of the start bit using the basic clock, and performs internal synchronization. As shown in figure 13.25, by sampling receive data at the rising-edge of the 16th, 32nd, 186th, or 128th pulse of the basic clock, data can be latched at the middle of the bit. The reception margin is given by the following formula.

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\,F - \frac{|D - 0.5|}{N}(1 + F) \right| \times 100\%$$

Where M: Reception margin (%)
N: Ratio of bit rate to clock (N = 32, 64, 372, and 256)
D: Clock duty (D = 0 to 1.0)
L: Frame length (L = 10)
F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5 and N = 372 in the above formula, the reception margin formula is as follows.

$$M = (0.5 - 1/2 \times 372) \times 100\%$$
$$= 49.866\%$$

14.4 Operation

The I²C bus interface can communicate either in I²C bus mode or clocked synchronous serial mode by setting FS in SAR.

14.4.1 I²C Bus Format

Figure 14.3 shows the I²C bus formats. Figure 14.4 shows the I²C bus timing. The first frame following a start condition always consists of 8 bits.

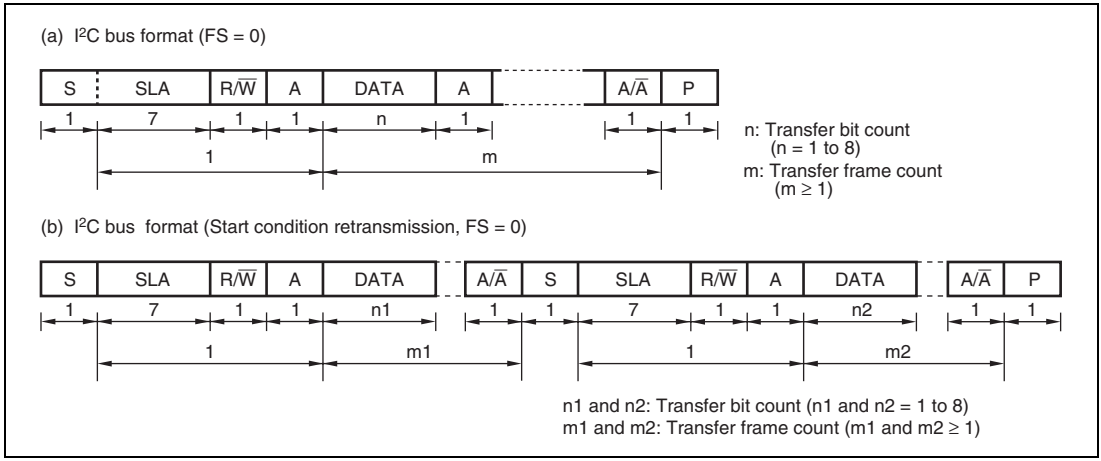

Figure 14.3 I²C Bus Formats

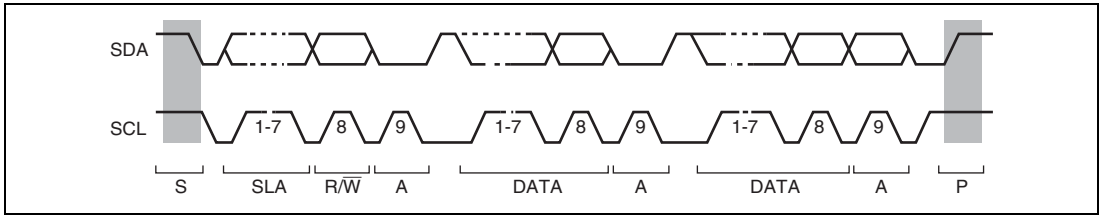

Figure 14.4 I²C Bus Timing

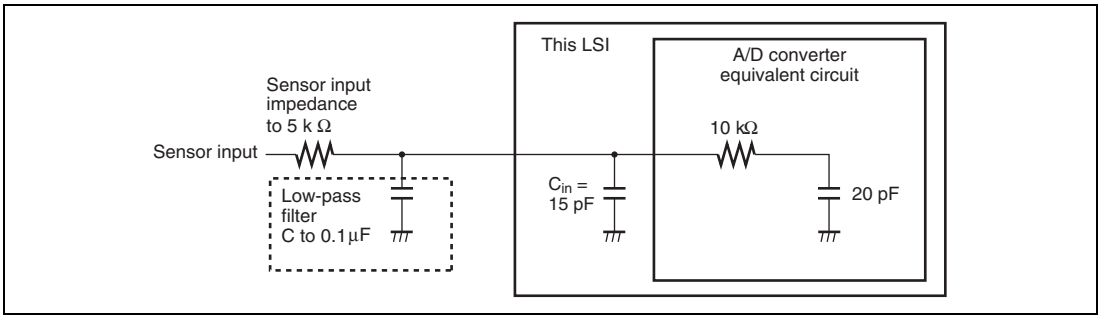

Figure 15.9 Example of Analog Input Circuit

15.8.4 Range of Analog Power Supply and Other Pin Settings

If the conditions below are not met, the reliability of the device may be adversely affected.

- Analog input voltage range
  The voltage applied to analog input pin ANn during A/D conversion should be in the range AVss ≤ ANn ≤ AVcc.
- Relationship between AVcc, AVss and Vcc, Vss
  Set AVss = Vss as the relationship between AVcc, AVss and Vcc, Vss. If the A/D converter is not used, the AVcc and AVss pins must not be left open.
- Vref range
  The reference voltage input from the Vref pin should be set to AVcc or less.

15.8.5 Notes on Board Design

In board design, digital circuitry and analog circuitry should be as mutually isolated as possible, and layout in which digital circuit signal lines and analog circuit signal lines cross or are in close proximity should be avoided as far as possible. Failure to do so may result in incorrect operation of the analog circuitry due to inductance, adversely affecting A/D conversion values. Also, digital circuitry must be isolated from the analog input signals (AN0 to AN15), and analog power supply (AVcc) by the analog ground (AVss). Also, the analog ground (AVss) should be connected at one point to a stable digital ground (Vss) on the board.

15.8.6 Notes on Noise Countermeasures

A protection circuit should be connected in order to prevent damage due to abnormal voltage, such as an excessive surge at the analog input pins (AN0 to AN15), between AVcc and AVss, as shown

Figure 17.1 shows an IEB block diagram.

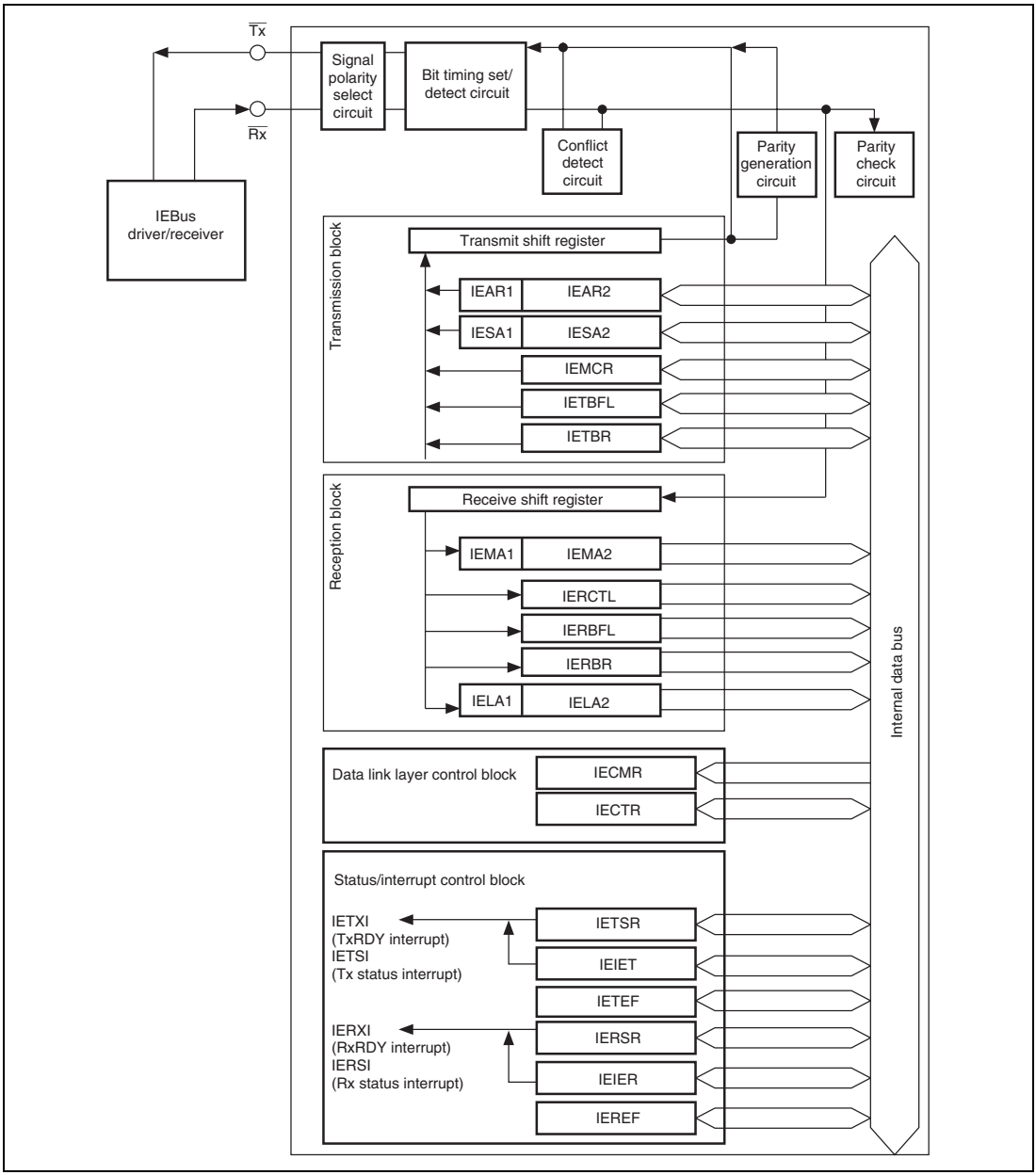

Figure 17.1 Block Diagram of IEB

17.3.13 IEBus Receive Message Length Register (IERBFL)

IERBFL indicates the message length field in slave/broadcast reception. This register is enabled when slave/broadcast receive starts, and the contents are changed at the timing of setting the RxS flag in IERSR.

This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	RBFL7	0	R	IEBus Receive Message Length
6	RBFL6	0	R	Indicates the contents of message length field in slave/broadcast reception.
5	RBFL5	0	R	
4	RBFL4	0	R	
3	RBFL3	0	R	
2	RBFL2	0	R	
1	RBFL1	0	R	
0	RBFL0	0	R	

(3) Slave Transmission Flow

Figure 17.12 shows the slave transmission flow. Numbers in the following description correspond to the numbers in Figure 17.12.

1. After the IEB and DTC have been initialized, a slave communications request command is issued from IECMR. During slave reception, the command execution status flag (CMX) in IEFLG is set and the slave communications request will not be issued.
2. The CMX flag is cleared when the slave reception is completed, the slave communications command is executed, and the SRQ flag is set.
3. If data up to the control field has been received correctly and if the contents of the control bits is H'3 or H'7, the transmit start detection flag (TxS) in IETSR register is set to 1. In this case, the TxS flag is cleared in the TxS interrupt handling routine.
4. The slave then transmits the message length field, and the IEB loads the transmit data in the data field from IETBR when the ACK is received. Then the TxRDY flag is set to 1. A DTC transfer request by IETxI is generated and the second byte data is written to the transmit buffer.
5. Similarly, the above data field load and transmission operations are repeated.
6. The DTC completes the data transfer for the number of specified bytes when data to be transmitted in the last byte is written to. At this time, the DTC does not clear the TxRDY flag. It, however, clears bit DTCEG5 in the DTC enable register G (DTCERG) not to generate more DTC transfer request.
7. A TxRDY interrupt (IETxI) is issued to the CPU when the DTC transfer is completed. In this interrupt handling routine, the TxRDY flag can be cleared. However, since the TxRDY interrupt will be generated again after the last byte transfer, the TxRDY flag remains set. (Note that the LUEE bit should be cleared to 0 because an underrun error occurs to terminate the transfer if the LUEE bit in IECTR is set to 1.) Note, however, that the TxRDY interrupt should be disabled because the TxRDY interrupt is always generated.
8. After the last data transfer has been completed, a transmit normal completion (TxF) interrupt occurs. In this case, the CPU clears the TxF flag and completes the normal completion interrupt and clears the SRQ flag to 0.

Notes: 1. As a transmit status interrupt (IETSI), a transmit error termination (TxE) interrupt as well as the transmit start detection (TxS) and transmit normal completion (TxF) interrupts must be enabled. If a transmit error completion interrupt is disabled, no interrupt is generated even if the transfer is terminated by an error.

2. If the control bits sent from the master unit is H'0, H'4, H'5, or H'6 in slave transmission, the IEB automatically performs processing and the TxS and TxF flags are not set.

Time quantum (TQ) is an integer multiple of the number of system clocks, and is determined by the baud rate prescaler (BRP) as follows. f_{CLK} is the system clock frequency.

$TQ = 2 \times (BRP\ setting + 1)/f_{CLK}$

The following formula is used to calculate the 1-bit time and bit rate.

1-bit time = $TQ \times (3 + TSEG1 + TSEG2)$

Bit rate = 1/Bit time

$= f_{CLK}/\{2 \times (BRP\ setting + 1) \times (3 + TSEG1 + TSEG2)\}$

Note: $f_{CLK} = \phi$ (system clock)
BCR value is used for BRP, TSEG1, and TSEG2.

Example: With a system clock of 20 MHz, a BRP setting of B'000000, a TSEG1 setting of B'0100, and a TSEG2 setting of B'011:

Bit rate = $20/\{2 \times (0 + 1) \times (3 + 4 + 3)\} = 1$ Mbps

Response	H'06

- Response, H'06, (one byte): Response to the blank check for user boot MATs
  If the contents of all user MATs are blank (H'FF), the boot program will return ACK.

Error Response	H'CD	H'52

- Error Response, H'CD, (one byte): Error response to the blank check of user MATs.
- Error code, H'52, (one byte): Erasure has not been completed.

(17) Boot Program State Inquiry

The boot program will return indications of its present state and error condition. This inquiry can be made in the inquiry/selection state or the programming/erasing state.

Command	H'4F

- Command, H'4F, (one byte): Inquiry regarding boot program's state

Response	H'5F	Size	Status	ERROR	SUM

- Response, H'5F, (one byte): Response to boot program state inquiry
- Size (one byte): The number of bytes. This is fixed to 2.
- Status (one byte): State of the boot program
- ERROR (one byte): Error state
  ERROR = 0 indicates normal operation.
  ERROR other than 0 indicates abnormal.
- SUM (one byte): Checksum
  This command can be accepted during programming/erasing operation, however, response time will be longer.

21.9 Usage Notes

21.9.1 Note on Crystal Resonator

As various characteristics related to the crystal resonator are closely linked to the user's board design, thorough evaluation is necessary on the user's part, using the resonator connection examples shown in this section as a guide. As the resonator circuit ratings will depend on the floating capacitance of the resonator and the mounting circuit, the ratings should be determined in consultation with the resonator manufacturer. The design must ensure that a voltage exceeding the maximum rating is not applied to the oscillator pin.

21.9.2 Note on Board Design

When designing the board, place the crystal resonator and its load capacitors as close as possible to the XTAL, EXTAL, OSC1, and OSC2 pins. Make wires as short as possible. Other signal lines should be routed away from the oscillator circuit, as shown in figure 21.11. This is to prevent induction from interfering with correct oscillation.

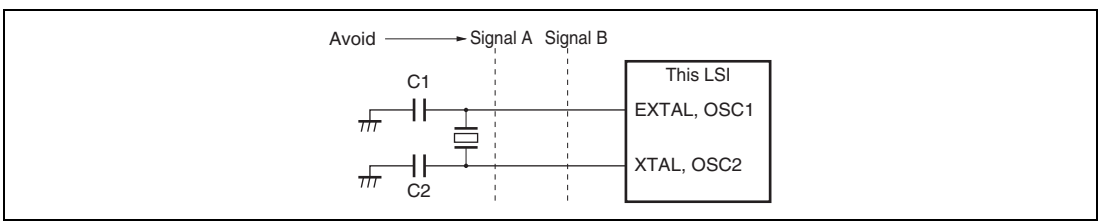

Figure 21.11 Note on Board Design of Oscillator Circuit

Figure 21.12 shows the recommended connection circuit between the power supply pins and Vss pin. The CB which is a capacitor for stabilization should be inserted near the pin between the power supply pins (V_{CC}, V_{CL}, $P1V_{CC}$, and $P2V_{CC}$) and Vss pin. Two CBs should be placed for the $P1V_{CC}$ line. Other signal lines should not be crossed.