Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, SCI
Peripherals	POR, PWM, WDT
Number of I/O	104
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BFQFP
Supplier Device Package	144-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2556fc20dv

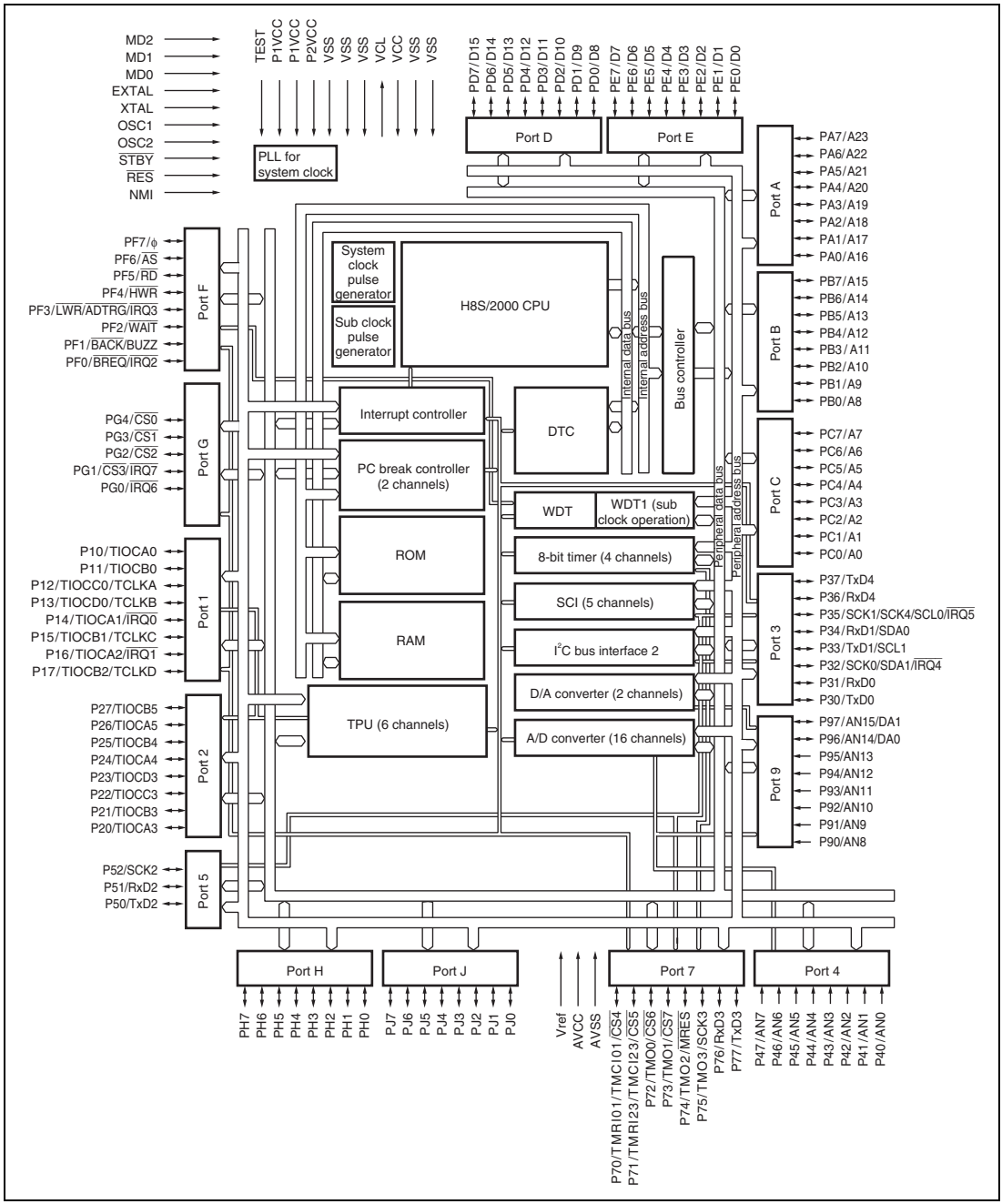


Figure 1.3 Internal Block Diagram of H8S/2506 Group

Table 2.4 Arithmetic Operations Instructions (2)

Instruction	Size*[1]	Function
DIVXS	B/W	Rd ÷ Rs → Rd Performs signed division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.
CMP	B/W/L	Rd – Rs, Rd – #IMM Compares data in a general register with data in another general register or with immediate data, and sets CCR bits according to the result.
NEG	B/W/L	0 – Rd → Rd Takes the two's complement (arithmetic complement) of data in a general register.
EXTU	W/L	Rd (zero extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the lower 16 bits of a 32-bit register to longword size, by padding with zeros on the left.
EXTS	W/L	Rd (sign extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the lower 16 bits of a 32-bit register to longword size, by extending the sign bit.
TAS*[2]	B	@ERd – 0, 1 → (<bit 7> of @ERd) Tests memory contents, and sets the most significant bit (bit 7) to 1.

Notes: 1. Refers to the operand size.
B: Byte
W: Word
L: Longword
2. Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction.

5.3.2 IRQ Enable Register (IER)

IER controls the enabling and disabling of interrupt requests IRQ7 to IRQ0.

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ7E	0	R/W	IRQ7 Enable The IRQ7 interrupt request is enabled when this bit is 1.
6	IRQ6E	0	R/W	IRQ6 Enable The IRQ6 interrupt request is enabled when this bit is 1.
5	IRQ5E	0	R/W	IRQ5 Enable The IRQ5 interrupt request is enabled when this bit is 1.
4	IRQ4E	0	R/W	IRQ4 Enable The IRQ4 interrupt request is enabled when this bit is 1.
3	IRQ3E	0	R/W	IRQ3 Enable The IRQ3 interrupt request is enabled when this bit is 1.
2	IRQ2E	0	R/W	IRQ2 Enable The IRQ2 interrupt request is enabled when this bit is 1.
1	IRQ1E	0	R/W	IRQ1 Enable The IRQ1 interrupt request is enabled when this bit is 1.
0	IRQ0E	0	R/W	IRQ0 Enable The IRQ0 interrupt request is enabled when this bit is 1.

7.6.3 Basic Timing

8-Bit 2-State Access Space: Figure 7.16 shows the bus timing for an 8-bit 2-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used.

Wait states cannot be inserted.

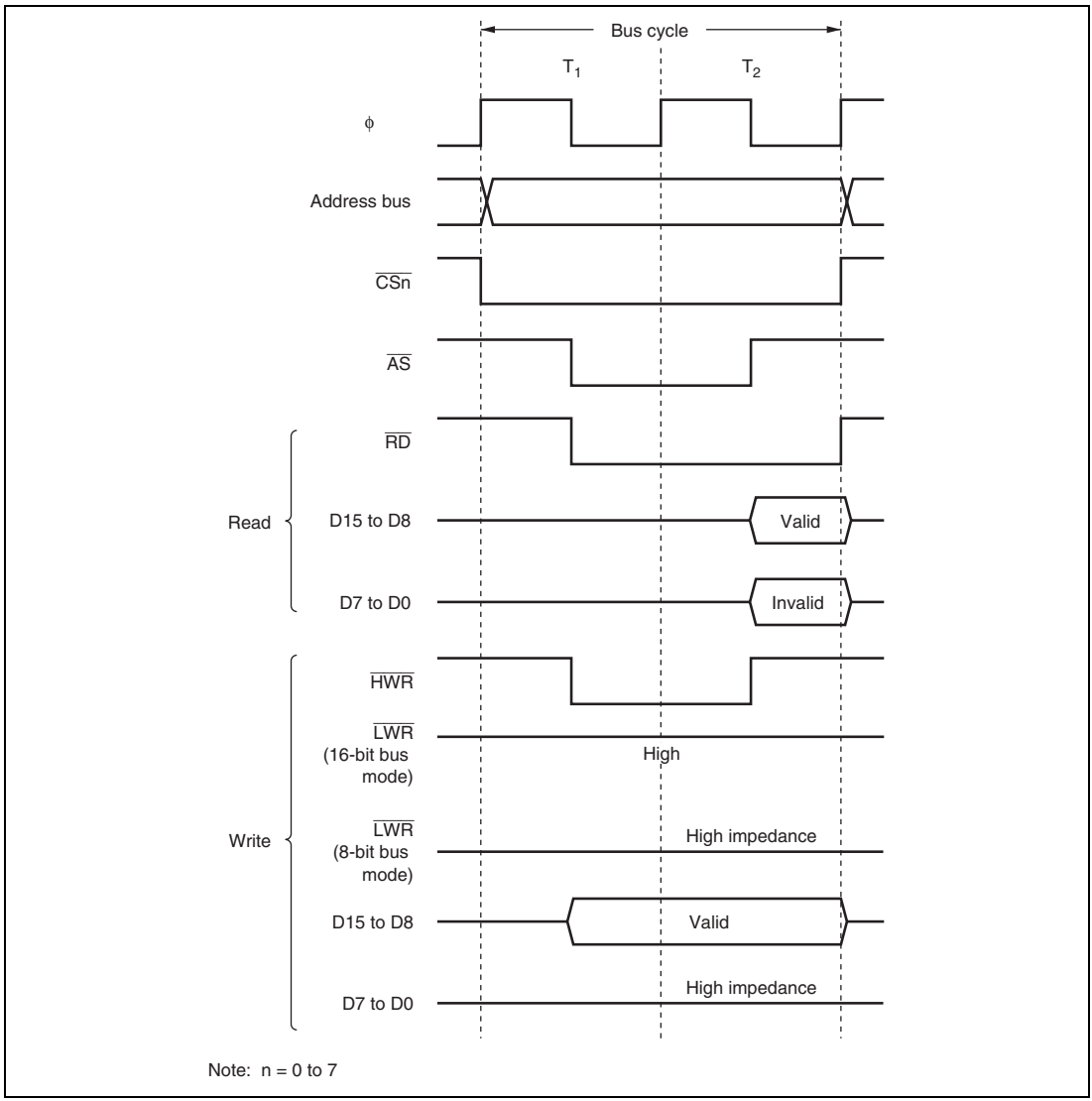


Figure 7.16 Bus Timing for 8-Bit 2-State Access Space

7.9 Bus Release

This LSI can release the external bus in response to a bus mastership request from an external device. In the external bus mastership released state, the internal bus master continues to operate as long as there is no external access.

In external extended mode, the bus mastership can be released to an external device by setting the BRLE bit in BCRL to 1. Driving the $\overline{\text{BREQ}}$ pin low issues an external bus mastership request to this LSI. When the $\overline{\text{BREQ}}$ pin is sampled, the $\overline{\text{BACK}}$ pin is driven low at the prescribed timing, and the address bus, data bus, and bus control signals are placed in the high-impedance state, establishing the external bus mastership released state.

In the external bus mastership released state, an internal bus master can perform accesses using the internal bus. When an internal bus master wants to make an external access, it temporarily defers activation of the bus cycle, and waits for the bus mastership request from the external bus master to be dropped.

When the $\overline{\text{BREQ}}$ pin is driven high, the $\overline{\text{BACK}}$ pin is driven high at the prescribed timing and the external bus mastership released state is terminated.

In the event of simultaneous external bus mastership release request and external access request generation, the order of priority is as follows:

(High) External bus mastership release > Internal bus master external access (Low)

Table 7.5 shows the pin states in the external bus mastership released state.

Table 7.5 Pin States in Bus Mastership Released State

Pins	Pin State
A23 to A0	High impedance
D15 to D0	High impedance
$\overline{\text{CSn}}$	High impedance
$\overline{\text{AS}}$	High impedance
$\overline{\text{RD}}$	High impedance
$\overline{\text{HWR}}$	High impedance
$\overline{\text{LWR}}$	High impedance

7.10 Bus Arbitration

This LSI has a bus arbiter that arbitrates bus master operations.

There are two bus masters, the CPU and DTC, which perform read/write operations when they have possession of the bus. Each bus master requests the bus mastership by means of a bus request signal. The bus arbiter determines priorities at the prescribed timing, and permits use of the bus by means of a bus mastership request acknowledge signal. The selected bus master then takes possession of the bus mastership and begins its operation.

7.10.1 Operation

The bus arbiter detects the bus masters' bus mastership request signals, and if the bus mastership is requested, sends a bus mastership request acknowledge signal to the bus master. If there are bus mastership requests from more than one bus master, the bus mastership request acknowledge signal is sent to the one with the highest priority. When a bus master receives the bus mastership request acknowledge signal, it takes possession of the bus until that signal is canceled.

The order of priority of the bus masters is as follows:

(High) DTC > CPU (Low)

An internal bus access by an internal bus master, and external bus mastership release, can be executed in parallel.

In the event of simultaneous external bus mastership release request, and internal bus master external access request generation, the order of priority is as follows:

(High) External bus mastership release > Internal bus master external access (Low)

7.10.2 Bus Mastership Transfer Timing

Even if a bus mastership request is received from a bus master with a higher priority than that of the bus master that has acquired the bus and is currently operating, the bus mastership is not necessarily transferred immediately. There are specific times at which each bus master can relinquish the bus mastership.

CPU: The CPU is the lowest-priority bus master, and if a bus mastership request is received from the DTC, the bus arbiter transfers the bus mastership to the bus master that issued the request. The timing for transfer of the bus mastership is as follows:

9.8.4 Port A Pull-Up MOS Control Register (PAPCR)

PAPCR controls on/off state of the input pull-up MOS for port A pins.

Bit	Bit Name	Initial Value	R/W	Description
7	PA7PCR	0	R/W	When a pin is specified as an input port, setting the corresponding bit to 1 turns on the input pull-up MOS for that pin.
6	PA6PCR	0	R/W	
5	PA5PCR	0	R/W	
4	PA4PCR	0	R/W	
3	PA3PCR	0	R/W	
2	PA2PCR	0	R/W	
1	PA1PCR	0	R/W	
0	PA0PCR	0	R/W	

9.8.5 Port A Open Drain Control Register (PAODR)

PAODR selects the output type for port A pins.

Bit	Bit Name	Initial Value	R/W	Description
7	PA7ODR	0	R/W	When these bits are set to 1, the corresponding pins function as NMOS open drain outputs. When cleared to 0, the corresponding pins function as CMOS outputs.
6	PA6ODR	0	R/W	
5	PA5ODR	0	R/W	
4	PA4ODR	0	R/W	
3	PA3ODR	0	R/W	
2	PA2ODR	0	R/W	
1	PA1ODR	0	R/W	
0	PA0ODR	0	R/W	

Table 10.7 TPSC0 to TPSC2 (channels 2)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
2	0	0	0	Internal clock: counts on ϕ/1
			1	Internal clock: counts on ϕ/4
		1	0	Internal clock: counts on ϕ/16
			1	Internal clock: counts on ϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	External clock: counts on TCLKC pin input
			1	Internal clock: counts on ϕ/1024

Note: This setting is ignored when channel 2 is in phase counting mode.

Table 10.8 TPSC0 to TPSC2 (channel 3)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
3	0	0	0	Internal clock: counts on ϕ/1
			1	Internal clock: counts on ϕ/4
		1	0	Internal clock: counts on ϕ/16
			1	Internal clock: counts on ϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	Internal clock: counts on ϕ/1024
		1	0	Internal clock: counts on ϕ/256
			1	Internal clock: counts on ϕ/4096

Figure 10.23 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

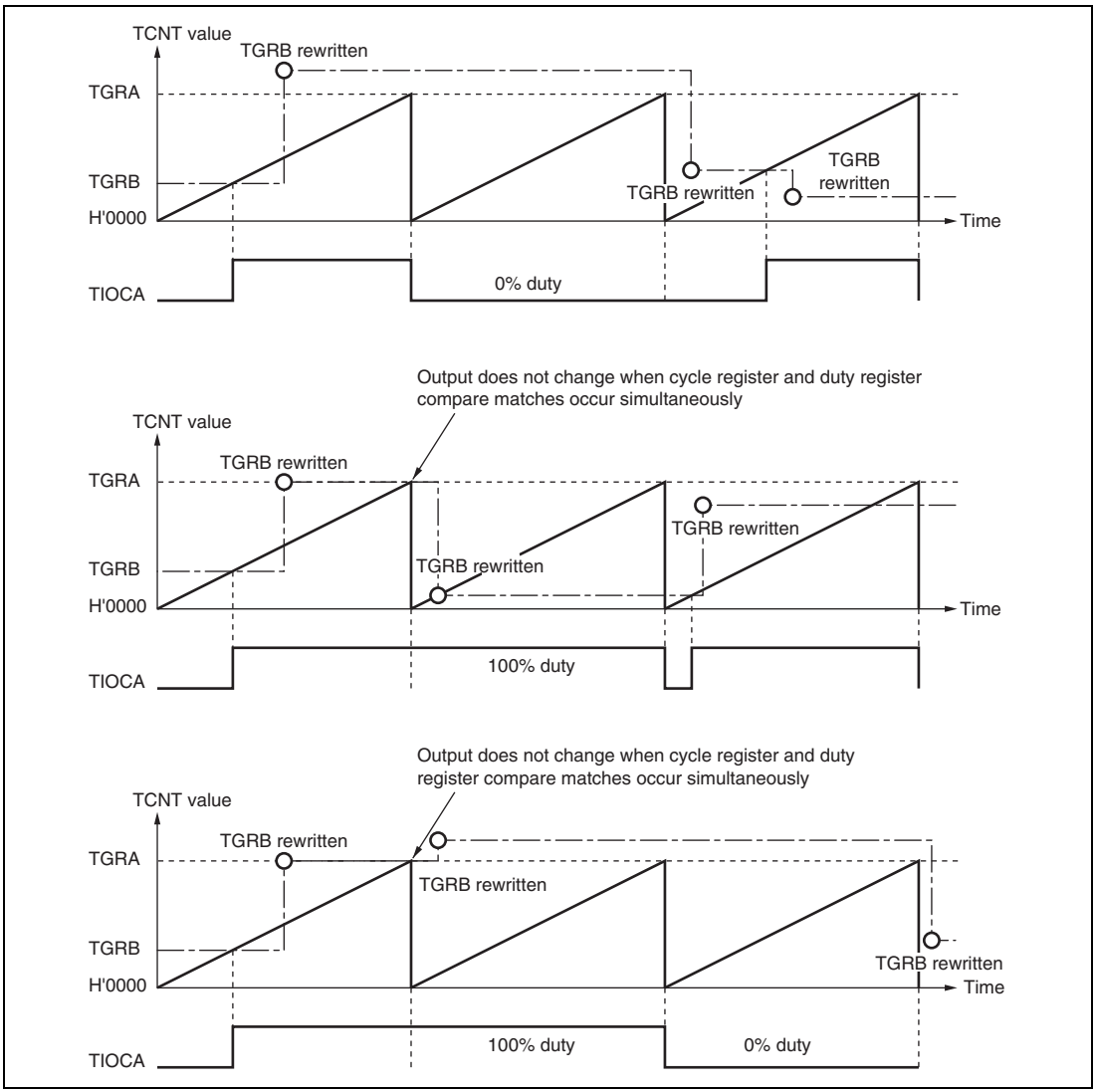


Figure 10.23 Example of PWM Mode Operation (3)

Output Compare Output Timing: A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the output value set in TIOR is output at the output compare output pin. After a match between TCNT and TGR, the compare match signal is not generated until the TCNT input clock is generated.

Figure 10.32 shows output compare output timing.

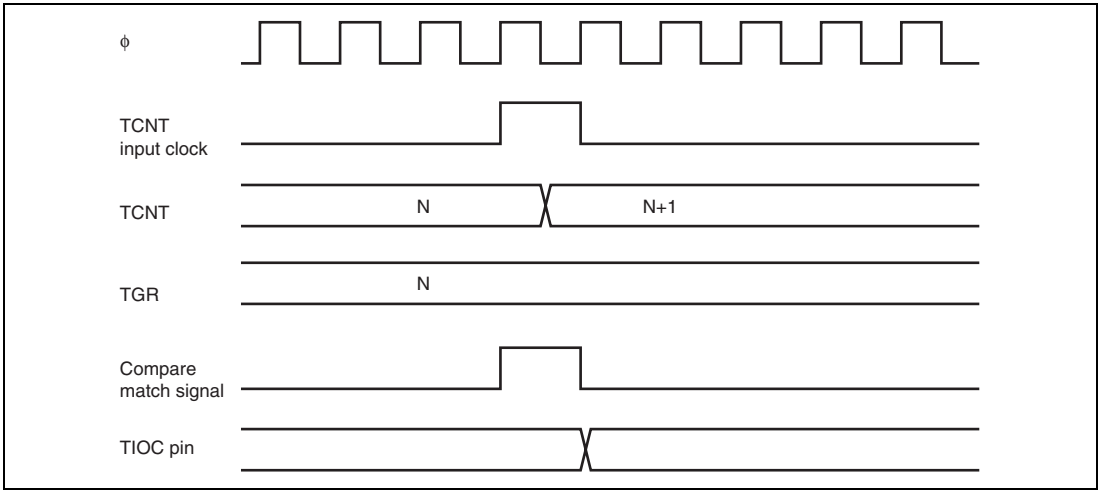


Figure 10.32 Output Compare Output Timing

Input Capture Signal Timing: Figure 10.33 shows input capture signal timing.

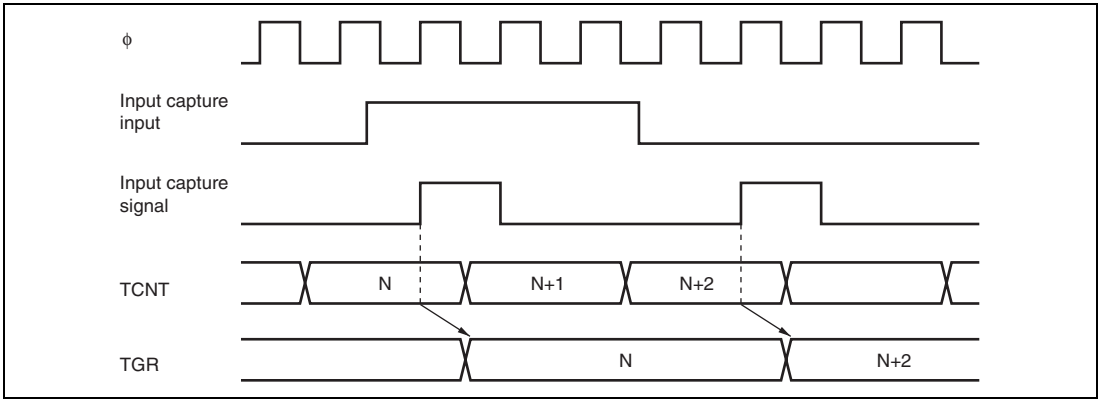


Figure 10.33 Input Capture Input Signal Timing

11.5.2 Timing of CMFA and CMFB Setting When a Compare-Match Occurs

The CMFA and CMFB flags in TCSR are set to 1 by a compare-match signal generated when the TCOR and TCNT values match. The compare-match signal is generated at the last state in which the match is true, just before the timer counter is updated. Therefore, when TCOR and TCNT match, the compare-match signal is not generated until the next incrementation clock input. Figure 11.5 shows the timing of CMF flag setting.

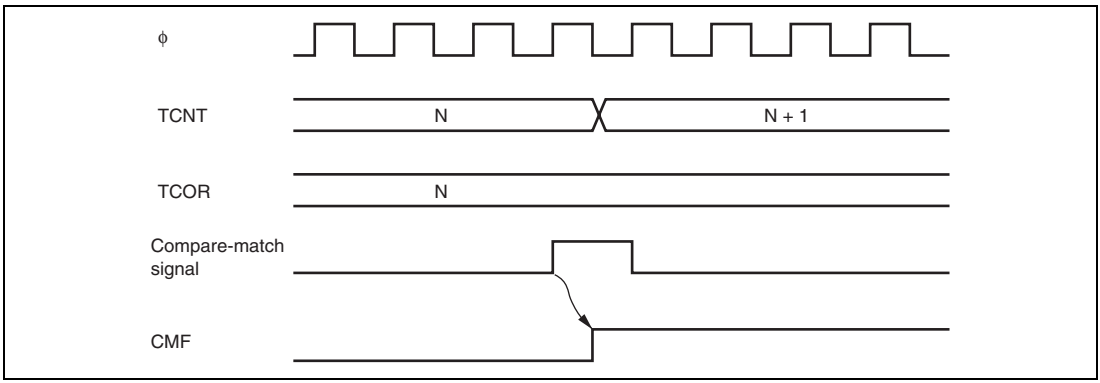


Figure 11.5 Timing of CMF Flag Setting

11.5.3 Timing of Timer Output When a Compare-Match Occurs

When a compare-match occurs, the timer output changes as specified by the output select bits, OS3 to OS0, in TCSR. Figure 11.6 shows the timing when the output is set to toggle at compare-match A.

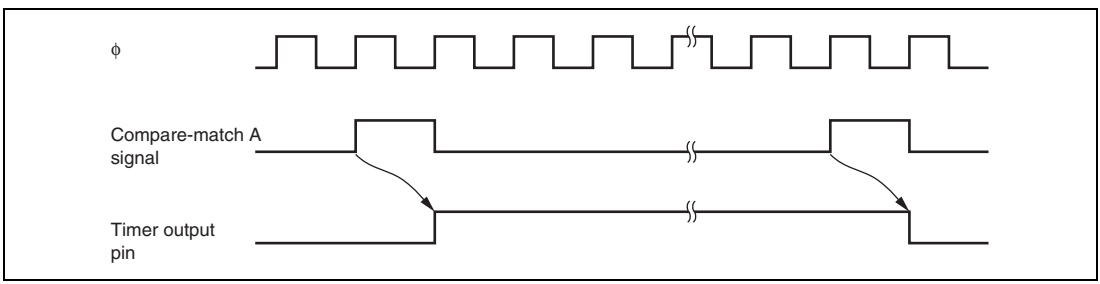
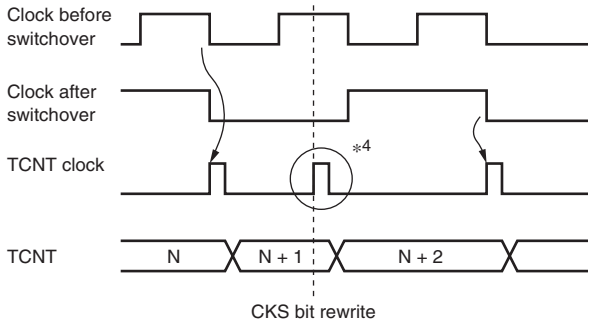
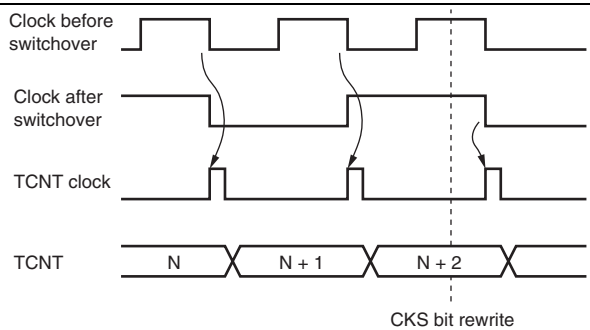


Figure 11.6 Timing of Timer Output

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	TCNT Clock Operation
3	Switching from high to low*3	
4	Switching from high to high	

Notes: 1. Includes switching from low to stop, and from stop to low.
2. Includes switching from stop to high.
3. Includes switching from high to stop.
4. Generated on the assumption that the switchover is a falling edge; TCNT is incremented.

Table 13.7 Maximum Bit Rate with External Clock Input (Clocked Synchronous Mode)

φ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bps)
8	1.3333	1333333.3
10	1.6667	1666666.7
12	2.0000	2000000.0
14	2.3333	2333333.3
16	2.6667	2666666.7
18	3.0000	3000000.0
20	3.3333	3333333.3
25	4.1667	4166666.7

Table 13.8 Examples of Bit Rate for Various BRR Settings (Smart Card Interface Mode) (When n = 0 and S = 372)

	Operating Frequency φ (MHz)							
Bit Rate	10.00		10.7136		13.00		14.2848	
(bps)	N	Error (%)	N	Error (%)	N	Error (%)	N	Error (%)
9600	1	30.00	1	25.00	1	8.99	1	0.00

	Operating Frequency φ (MHz)							
Bit Rate	16.00		18.00		20.00		25.00	
(bps)	N	Error (%)	N	Error (%)	N	Error (%)	N	Error (%)
9600	1	12.01	2	15.99	2	6.66	3	12.49

16.3.2 D/A Control Register (DACR)

DACR controls D/A converter operation.

Bit	Bit Name	Initial Value	R/W	Description
7	DAOE1	0	R/W	D/A Output Enable 1 Controls D/A conversion and analog output 0: Analog output DA1 is disabled 1: D/A conversion for channel 1 and analog output DA1 are enabled
6	DAOE0	0	R/W	D/A Output Enable 0 Controls D/A conversion and analog output 0: Analog output DA0 is disabled 1: D/A conversion for channel 0 and analog output DA0 are enabled
5	DAE	0	R/W	D/A Enable Controls D/A conversion in conjunction with the DAOE0 and DAOE1 bits. When the DAE bit is cleared to 0, D/A conversion for channels 0 and 1 are controlled individually. When DAE is set to 1, D/A conversion for channels 0 and 1 are controlled as one. Conversion result output is controlled by the DAOE0 and DAOE1 bits. For details, see table 16.2.
4 to 0	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.

When more than one unit starts transfer of communications frame at the same timing, broadcast communications has priority over normal communications, and arbitration occurs.

(2) Master Address Field

The master address field is a field for transmitting the unit address (master address) to other units. The master address field is comprised of master address bits and a parity bit.

The master address has 12 bits and are output MSB first.

When more than one unit starts transfer of the broadcast bit having the same value at the same timing, arbitration is decided by the master address field.

In the master address field, self-output data and data on the bus are compared for every one-bit transfer. If the self-output master address and data on the bus are different, the unit that loses arbitration, stops transfer, and enters the receive state.

Since the IEBus is configured with wired AND, a unit having the smallest master address of the units in arbitration (arbitration master) wins in arbitration.

Finally, only a single unit remains in the transfer state as a master unit after outputting 12-bit master address.

Next, this master unit outputs a parity bit*, defines the master address to other units, and then enters the slave address field output state.

Note: Since even parity is used, when the number of one bits in the master address is odd, the parity bit is 1.

(3) Slave Address Field

The slave address field is a field to transmit an address (slave address) of a unit (slave unit) to which a master transmit data. The slave address field is comprised of slave address bits, a parity bit, and an acknowledge bit.

The slave address has 12 bits and is output MSB first. The parity bit is output after the 12-bit slave address is transmitted in order to avoid receiving the slave address accidentally. The master unit then detects the acknowledgement from the slave unit in order to confirm that the slave unit exists on the bus. When the acknowledgement is detected, the master unit enters the control field output state. However, the master unit enters the control field output state without detecting the acknowledgement in broadcast communications.

17.3.5 IEBus Master Unit Address Register 2 (IEAR2)

IEAR2 sets the upper 8 bits of the master unit address. In master communications, this register becomes the master address field value. In slave communications, this register is compared with the received slave address field.

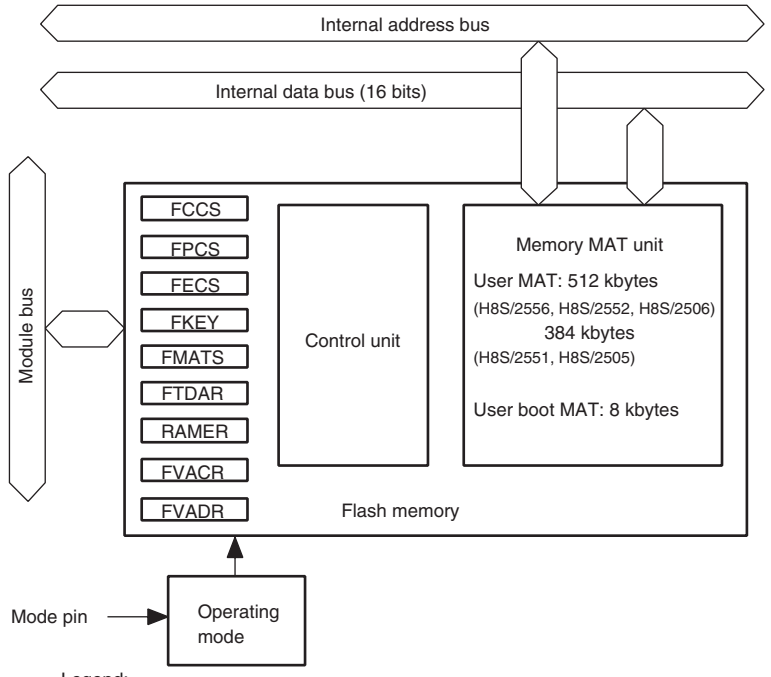
Bit	Bit Name	Initial Value	R/W	Description
7	IAR11	0	R/W	Upper 8 Bits of IEBus Master Unit Address
6	IAR10	0	R/W	Set the upper 8 bits of the master unit address.
5	IAR9	0	R/W	
4	IAR8	0	R/W	
3	IAR7	0	R/W	
2	IAR6	0	R/W	
1	IAR5	0	R/W	
0	IAR4	0	R/W	

17.3.6 IEBus Slave Address Setting Register 1 (IESA1)

IESA1 sets the lower 4 bits of the communications destination slave unit address. For slave communications, it is not necessary to set this register.

Bit	Bit Name	Initial Value	R/W	Description
7	ISA3	0	R/W	Lower 4 Bits of IEBus Slave Address
6	ISA2	0	R/W	These bits set the lower 4 bits of the communications destination slave unit address
5	ISA1	0	R/W	
4	ISA0	0	R/W	
3 to 0	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.

20.1.1 Block Diagram



Legend:
FCCS: Flash code control status register
FPCS: Flash program code select register
FECS: Flash erase code select register
FKEY: Flash key code register
FMATS: Flash MAT select register
FTDAR: Flash transfer destination address register
RAMER: RAM emulation register
FVACR: Flash vector address control register
FVADR: Flash vector address data register

Note: To read from or write to the above registers except RAMER, the FLSHE bit in the system control register 2 (SYSCR2) must be set to 1. When FLSHE is 1, some TPU control registers (H'FFFE80 to H'FFFEB1) cannot be accessed. The FLSHE bit should be cleared before the TPU registers are accessed.

Figure 20.1 Block Diagram of Flash Memory

- Area (1 byte)
  H'00: User boot MAT
  H'01: User MAT
  An address error occurs when the area setting is incorrect.
- Read address (4 bytes): Start address to be read from
- Read size (4 bytes): Size of data to be read
- SUM (1 byte): Checksum

Response	H'52	Read size						
	Data	···						
	SUM							

- Response: H'52 (1 byte): Response to memory read
- Read size (4 bytes): Size of data to be read
- Data (n bytes): Data for the read size from the read address
- SUM (1 byte): Checksum

Error Response	H'D2	ERROR

- Error response: H'D2 (1 byte): Error response to memory read
- ERROR: (1 byte): Error code
  H'11: Sum check error
  H'2A: Address error
  The read address is not in the MAT.
  H'2B: Size error
  The read size exceeds the MAT.

(13) User-Boot Program Sum Check

The boot program will return the byte-by-byte total of the contents of the bytes of the user-boot program, as a four-byte value.

Command	H'4A

- Command, H'4A, (one byte): Sum check for user-boot program

Response	H'5A	Size	Checksum of user boot program	SUM

- Response, H'5A, (one byte): Response to the sum check of user-boot program
- Size (one byte): The number of bytes that represents the checksum
  This is fixed to 4.
- Checksum of user boot program (four bytes): Checksum of user boot MATs
  The total of the data is obtained in byte units.

24.4.2 Clock Timing

Table 24.6 lists the clock timing.

Table 24.6 Clock Timing (1)

Conditions (for H8S/2552 Group, H8S/2506 Group):
V_{CC} = P1V_{CC} = P2V_{CC} = 5.0 V ± 0.5 V (BUFGC1 and BUFGC2 in ICPCR are 0)/ 3.3 V ± 0.3 V (BUFGC1 and BUFGC2 in ICPCR are 1),
AV_{CC} = 3.0 V to 5.5 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ= 32.768 kHz,
8 to 26 MHz, T_a = –20°C to +75°C (regular specifications)*, T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min.	Max.	Unit	Test Conditions
Clock cycle time		t_{cyc}	38	125	ns	Figure 24.5
Clock high pulse width		t_{CH}	12	—	ns	
Clock low pulse width		t_{CL}	12	—	ns	
Clock rise time		t_{Cr}	—	5	ns	
Clock fall time		t_{Cf}	—	5	ns	
EXTAL clock input frequency	PLL1 multiplication	f_{EX}	8	26	MHz	Figure 21.5
	PLL2 multiplication		8	13		
Clock oscillator settling time at reset (crystal)		t_{OSC1}	20	—	ms	Figure 24.6
Clock oscillator settling time at reset (external clock)			20	—	ms	
Clock oscillator settling time in software standby (crystal)		t_{OSC2}	8	—	ms	Figure 22.3
External clock settling delay time		t_{DEXT}	8	—	ms	Figure 24.6
Subclock oscillator settling time		t_{OSC3}	2	—	s	
Subclock oscillator frequency		f_{SUB}		32.768	kHz	
Subclock (ϕ_{SUB}) cycle time		t_{SUB}		30.5	µs	

Note: * The regular specifications are supported in the H8S/2506 Group only.