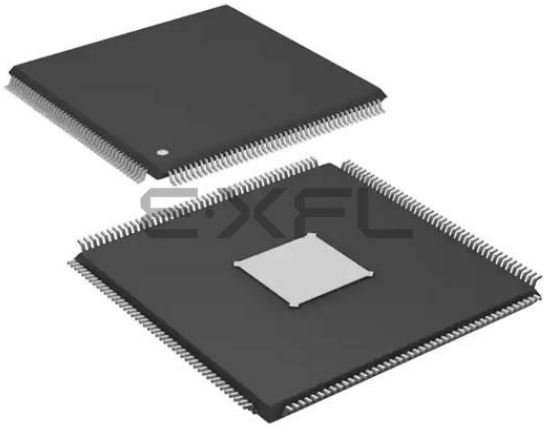

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	No
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-HLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf311r3k1cku2

Table of Contents

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

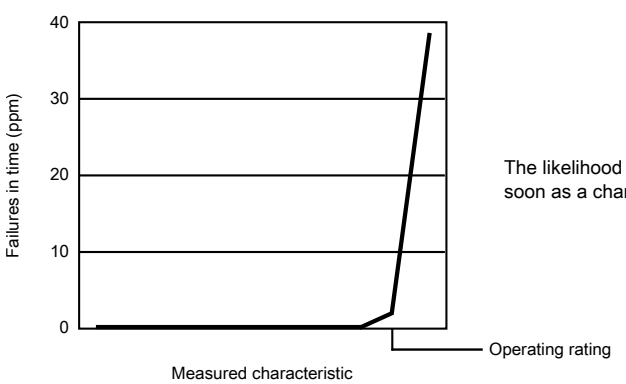
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

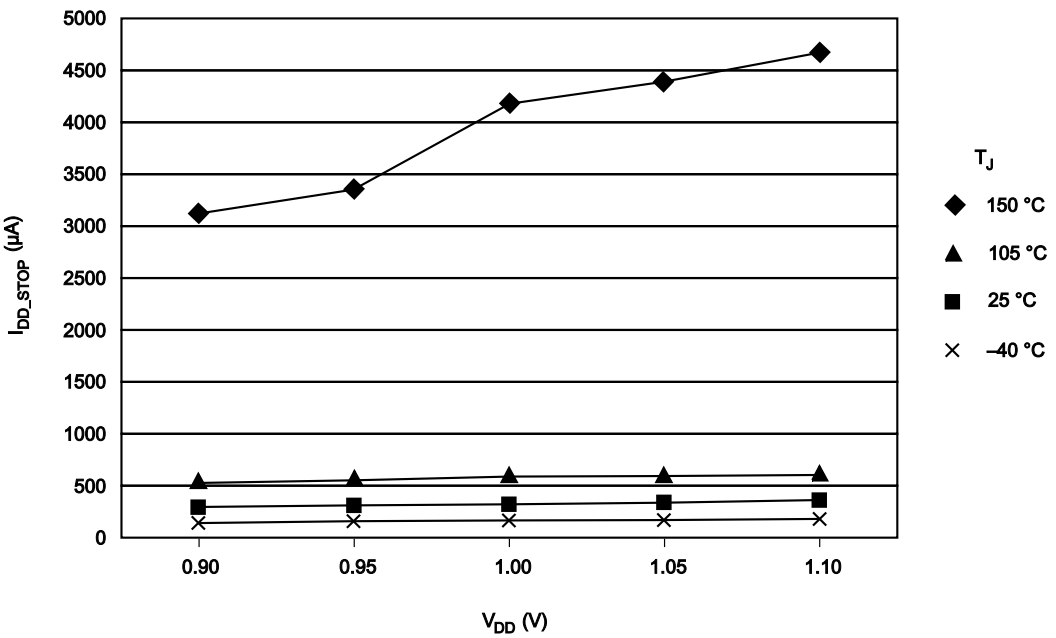
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Handling ratings

4.1 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I_{LAT}	Latch-up Current at ambient temperature of 85 °C	-100	100	mA	

1. Determined according to the AEC spec AEC-Q100-002 for HBM
2. Determined according to AEC spec AEC-Q100-011

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

8.4 Recommended operating conditions

Table 30. Recommended operating conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
USB0_VBUS	VBUS supply for USB w.r.t USB0_GND		4.4	5	5.25	V
USB1_VBUS	VBUS supply for USB w.r.t USB1_GND		4.4	5	5.25	V
USB_DCAP	USB LDO 5V->3 V Output	External DCAP (10uF termination for USBREG)		3		V
VBAT	Battery supply in case of LDOIN fails	External CAP 0.1uF	2.4	3.3	3.6	V
VDD33_LDOIN	LDO input supply		3	3.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	Recommended External DCAP: 1uF(Min) 10uF (Max)		1.1		V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR pre-driver, EFUSE	Recommended External DCAP: 1uF(Min) 10uF (Max)		2.5		V
VDD33	GPIO 3.3V IO supply	External CAP (10uF)	3	3.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	External CAP (10uF)	3	3.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	External CAP (10uF)	3	3.3	3.6	V
VREFH_ADC	High reference voltage for ADC and DAC	Relation with VDDDA33_ADC (1uF)	2.5	3.3	VDDA33_ADC	V
VREFL_ADC	Low reference voltage for ADC and DAC	External CAP (10uF)		0		V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	External CAP 10uF	3	3.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)		1.16	1.23	1.26	V
FA_VDD	For testing purpose only should be shorted to VDD on board.		1.16	1.23	1.26	V
VDD[1]	1.2V core supply	4.7uF with a low ESR value (100 milliohms)	1.16	1.23	1.26	V
USB0_GND	Ground supply for USB			0		V
USB1_GND	Ground supply for USB			0		V
VSS_KEL0	USB LDO ground output			0		V
VSS	VSS ground			0		V
VSSA33_ADC	Ground supply for ADC, DAC and IO segment			0		V

Table continues on the next page...

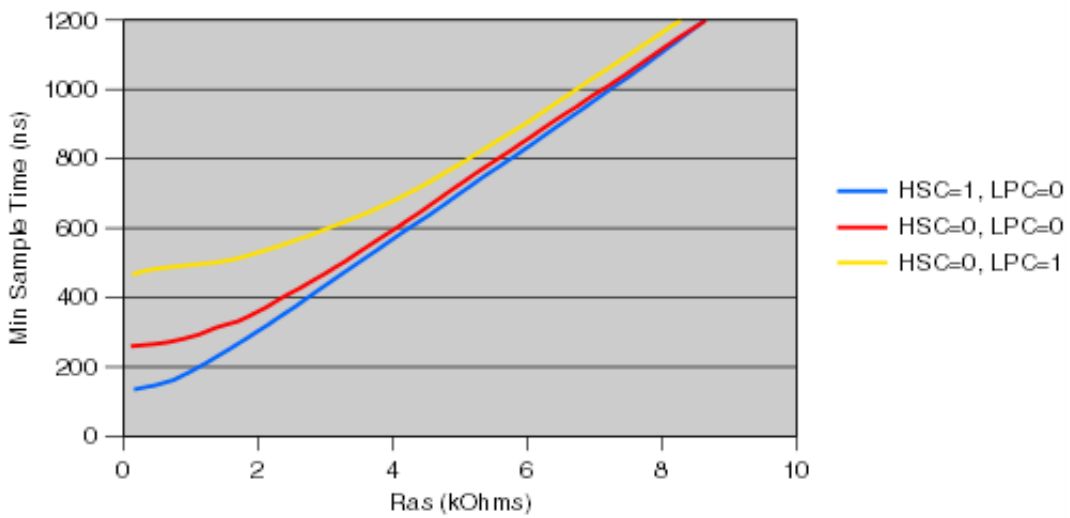


Figure 8. Minimum Sample Time Vs Ras (Cas = 10pF)

9.1.2 12-bit DAC electrical characteristics

9.1.2.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Typ	Max.	Unit	Notes
VDDA33_ADC	Supply voltage	3.0	3.3	3.6	V	
VREFH_ADC	Reference voltage	2.5	3.3	VDDA33_ADC	V	1
C_L	Output load capacitance	—		100	pF	2
I_L	Output load current	—		1	mA	

1. User will need to set up DACx_STATCTRL [DACRFS]=1 to select the valid VREFH_ADC reference. When DACx_STATCTRL [DACRFS]=0, the DAC reference is connected to an internal ground node and is not a valid voltage reference. Note that the DAC and ADC share the VREFH_ADC reference simultaneously.)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

9.1.2.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	100	μA	
I_{DDA_DACHP}	Supply current — high-power mode	—	—	500	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	10	15	μs	

Table continues on the next page...

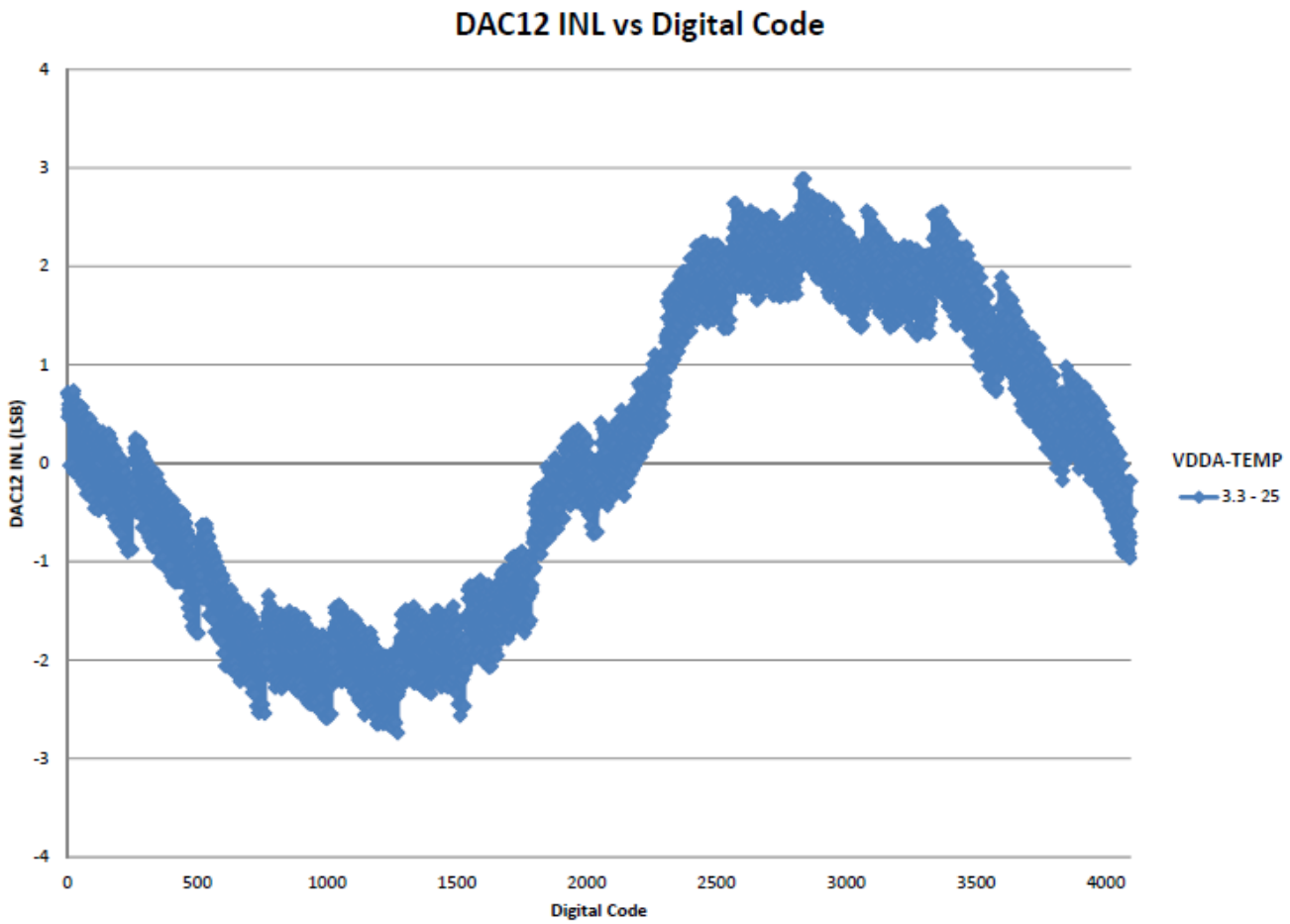


Figure 9. INL error vs. digital code

NOTE

VideoADC 3.3V and 1.2V power supply pins should be decoupled to their respective grounds using low-ESR 100nF capacitors

NOTE

If possible, avoid using switched voltage regulators for the AFE power domains. Use linear voltage regulators instead.

NOTE

The 3.3V and 1.2V power domains should be separated from other circuitry on the board by inductors/beads to filter out high frequency noise.

9.2 Display and Video interfaces

9.2.1 DCU Switching Specifications

9.2.1.1 Interface to TFT panels (DCU0/1)

This section provides the LCD interface timing for a generic active matrix color TFT panel. In the figure below, signals are shown with positive polarity. The sequence of events for active matrix interface timing:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 66 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

Figure 14. TFT LCD interface timing overview[1]

1. In the figure, LD[23:0]" signal is "line data," an aggregation of the DCU's RGB signals—R[0:7], G[0:7] and B[0:7].

Table 52. NFC specifications

Num	Description	Min.	Max.	Unit
t_{CLS}	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
t_{CLH}	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
t_{CS}	$\overline{\text{NFC\_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
t_{CH}	$\overline{\text{NFC\_CEn}}$ hold time	$T_H + T_L$	—	ns
t_{WP}	$\overline{\text{NFC\_WP}}$ pulse width	$T_L - 1$	—	ns
t_{ALS}	NFC_ALE setup time	$2T_H + T_L$	—	ns
t_{ALH}	NFC_ALE hold time	$T_H + T_L$	—	ns
t_{DS}	Data setup time	$T_L - 1$	—	ns
t_{DH}	Data hold time	$T_H - 1$	—	ns
t_{WC}	Write cycle time	$T_H + T_L - 1$	—	ns
t_{WH}	$\overline{\text{NFC\_WE}}$ hold time	$T_H - 1$	—	ns
t_{RR}	Ready to $\overline{\text{NFC\_RE}}$ low	$4T_H + 3T_L + 90$	—	ns
t_{RP}	$\overline{\text{NFC\_RE}}$ pulse width	$T_L + 1$	—	ns
t_{RC}	Read cycle time	$T_L + T_H - 1$	—	ns
t_{REH}	$\overline{\text{NFC\_RE}}$ high hold time	$T_H - 1$	—	ns
t_{IS}	Data input setup time	11	—	ns

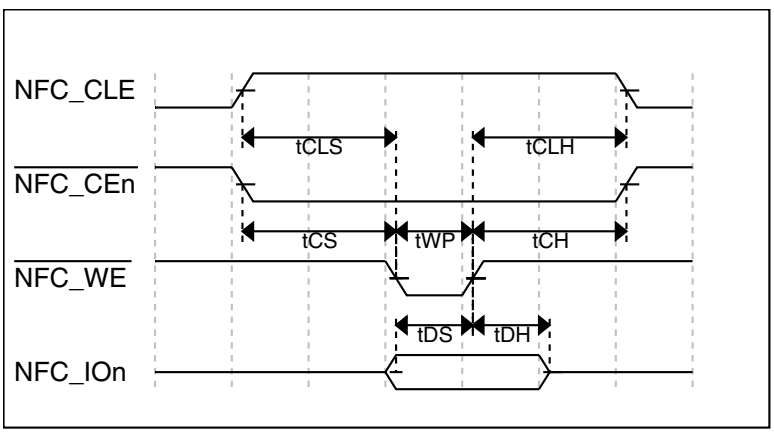


Figure 34. Command latch cycle timing

9.5.4.2 DDR3 Read Cycle

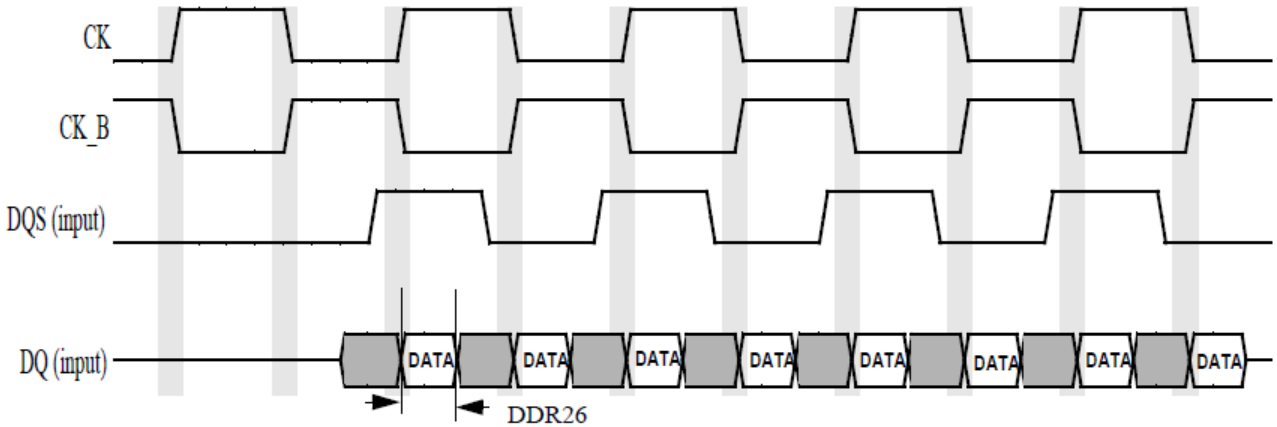


Figure 42. DDR3 Read Cycle

Table 55. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	-	750	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.5 LPDDR2 Read Cycle

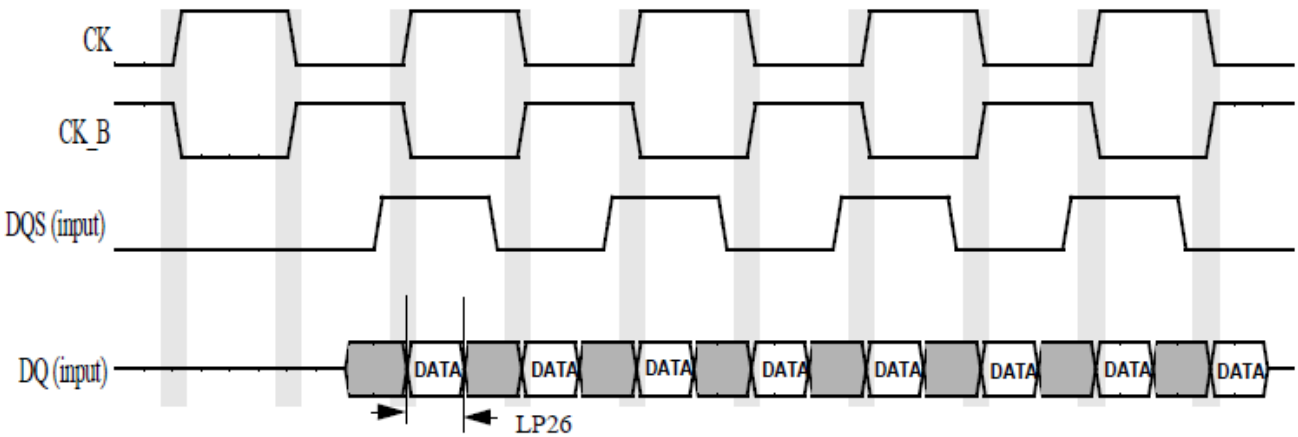


Figure 45. LPDDR2 Read cycle

Table 58. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	-	270	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.5.4.6 LPDDR2 Write Cycle

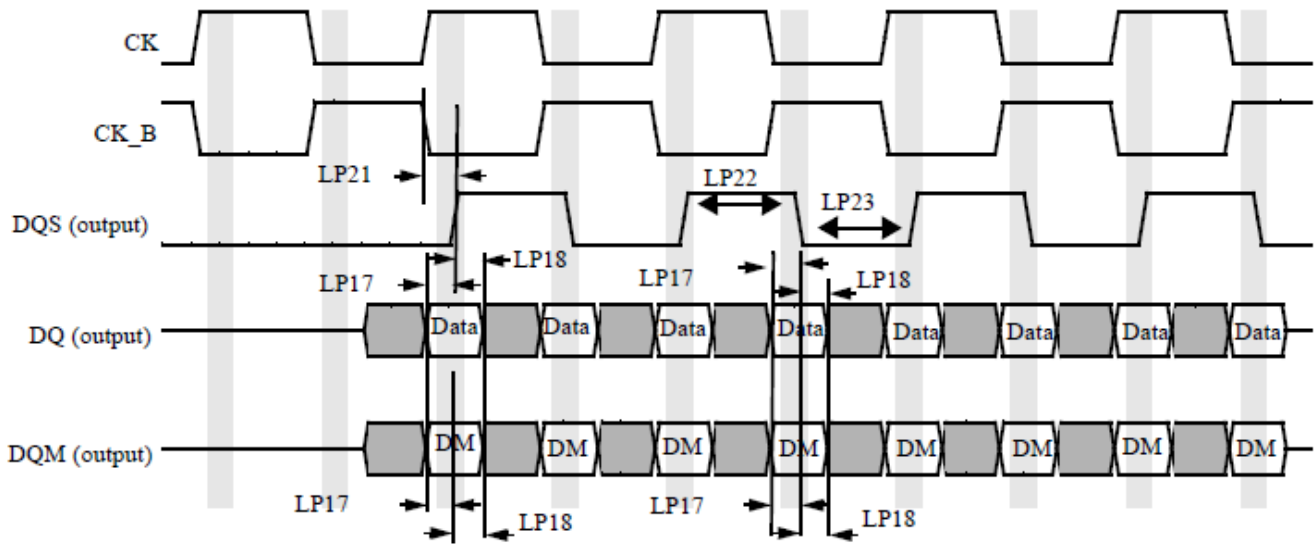


Figure 46. LPDDR3 Write Cycle

Table 59. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	tDS	220	0.55	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	tDH	220	0.55	ps
LP21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
LP22	DQS high level width	tDQSH	0.4	-	tCK
LP23	DQS low level width	tDQSL	0.4	-	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

Table 65. I2C output timing specifications — SCL and SDA1234 (continued)

No.	Parameter	Min	Max	Unit
2	Clock low time	10	—	PER_CLK Cycle
3	Bus free time between Start and Stop condition	4.7	—	µs
4	Data hold time	7	—	PER_CLK Cycle
5	Clock high time	10	—	PER_CLK Cycle
6	Data setup time	2	—	PER_CLK Cycle
7	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	Stop condition setup time	10	—	PER_CLK Cycle

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. Output parameters are valid for CL = 25 pF, where CL is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speedsand may cause incorrect operation.
4. Programming the IBFD register (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.
5. PER_CLK is the IPG Clock which drive the I2C BIU and module clock inputs. Typically this is 83Mhz. See the Clocking Overview chapter in the device reference manual for more details.

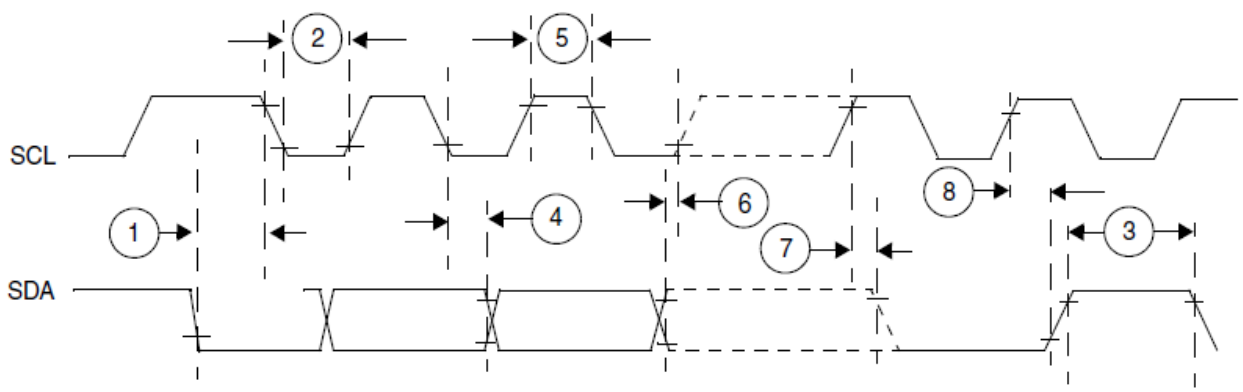


Figure 52. I2C input/output timing

9.7.4 Slow internal RC oscillator (128 KHz) electrical characteristics

This section describes a slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

Table 70. Slow internal RC oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCL}	RC oscillator low frequency	T_A= 25 °C, trimmed	—	128	—	kHz
I_{RCL}	RC oscillator low frequency current	T_A= 25 °C, trimmed	—	3.1		µA
RCLTRIM	RC oscillator precision after trimming of f_{RCL}	T_A= 25 °C	-1	—	+1	%
RCLVAR 3	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration	High frequency configuration	-5	—	+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.7.5 PLL1 and PLL2 (528 MHz System PLL) Electrical Parameters

Table 71. PLL1 and PLL2 Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<7500 reference cycles
Period jitter(p2p)	<140ps
Duty Cycle	48.9%~51.7% PLL output

9.7.6 PLL3 and PLL7 (480 MHz USB PLL) Electrical Parameters

Table 72. PLL3 and PLL7 Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<425 reference cycles
Period jitter(p2p)	<140 ps
Duty Cycle	48.9%~51.7% PLL output

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
T3	27	TEST			TEST							
T1	23	Ext_POR			TEST2							
V12	69	DECAP_ V11_LDO_ OUT			DECAP_ V11_LDO_ OUT							
T11	65	DECAP_ V25_LDO_ OUT			DECAP_ V25_LDO_ OUT							
T2	26	BCTRL			BCTRL							
P5	24	VDDREG			VDDREG							
T12	68	VDD33_ LDOIN			VDD33_ LDOIN							
V11	67	VSS			VSS							
U11	66	VSS_KEL0			VSS_KEL0							
W14	—	LVDS0P			LVDS0P							
Y14	—	LVDS0N			LVDS0N							
K4	3	JTCLK/ SWCLK	JTCLK/ SWCLK	PTA8	JTCLK/ SWCLK			DCU0_R0			MLBCLK	
K2	4	JTDI	JTDI	PTA9	JTDI	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK	DCU0_R1		WDOG_b		
K1	5	JTDO	JTDO/ TRACESWO	PTA10	JTDO	EXT_AUDIO_ MCLK		DCU0_G0		ENET_TS_ CLKIN	MLBSIGNAL	
L1	6	JTMS/ SWDIO	JTMS/ SWDIO	PTA11	JTMS/ SWDIO			DCU0_G1			MLBDATA	
L3	7	PTA12		PTA12	TRACECK	EXT_AUDIO_ MCLK				VIU_DATA13	I2C0_SCL	
Y5	43	PTA16		PTA16	TRACED0	USB0_ VBUS_EN	ADC1_SE0	LCD29	SAI2_TX_ BCLK	VIU_DATA14	I2C0_SDA	
Y6	44	PTA17		PTA17	TRACED1	USB0_ VBUS_OC	ADC1_SE1	LCD30	USB0_SOF_ PULSE	VIU_DATA15	I2C1_SCL	
V6	46	PTA18		PTA18	TRACED2	ADC0_SE0	FTM1_QD_ PHA	LCD31	SAI2_TX_ DATA	VIU_DATA16	I2C1_SDA	
U6	47	PTA19		PTA19	TRACED3	ADC0_SE1	FTM1_QD_ PHB	LCD32	SAI2_TX_ SYNC	VIU_DATA17	QSPI1_A_ SCK	
B18	143	PTA20		PTA20	TRACED4			LCD33		SCI3_TX	DCU1_ HSYNC/ DCU1_ TCON1	
D18	145	PTA21		PTA21/ MII0_RXCLK	TRACED5				SAI2_RX_ BCLK	SCI3_RX	DCU1_ VSYNC/ DCU1_ TCON2	
E17	147	PTA22		PTA22	TRACED6				SAI2_RX_ DATA	I2C2_SCL	DCU1_TAG/ DCU1_ TCON0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_SYNC	I2C2_SDA	DCU1_DE/DCU1_TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_VBUS_EN			SDHC1_CLK	DCU1_TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_VBUS_OC			SDHC1_CMD	DCU1_TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_BCLK			SDHC1_DAT0	DCU1_TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_BCLK			SDHC1_DAT1	DCU1_TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_DATA	ENET1_1588_TMR0	SCI4_TX	SDHC1_DAT2	DCU1_TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_DATA	ENET1_1588_TMR1	SCI4_RX	SDHC1_DAT3	DCU1_TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_SYNC	ENET1_1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_SYNC	ENET1_1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_BCLK	VIU_DATA18	QSPI1_A_CS0	
T7	50	PTB1	RCON30	PTB1	FTM0_CH1	ADC0_SE3	RCON30	LCD35	SAI2_RX_DATA	VIU_DATA19	QSPI1_A_DATA3	
V7	51	PTB2	RCON31	PTB2	FTM0_CH2	ADC1_SE2	RCON31	LCD36	SAI2_RX_SYNC	VIU_DATA20	QSPI1_A_DATA2	
W7	53	PTB3		PTB3	FTM0_CH3	ADC1_SE3	EXTRIG	LCD37		VIU_DATA21	QSPI1_A_DATA1	
Y7	54	PTB4		PTB4	FTM0_CH4	SCI1_TX	ADC0_SE4	LCD38	VIU_FID	VIU_DATA22	QSPI1_A_DATA0	
Y8	55	PTB5		PTB5	FTM0_CH5	SCI1_RX	ADC1_SE4	LCD39	VIU_DE	VIU_DATA23	QSPI1_A_DQS	
W8	56	PTB6		PTB6	FTM0_CH6	SCI1_RTS	QSPI0_A_CS1	LCD40	FB_CLKOUT	VIU_HSYNC	SCI2_TX	
D13	166	PTB7		PTB7	FTM0_CH7	SCI1_CTS	QSPI0_B_CS1	LCD41		VIU_VSYNC	SCI2_RX	
J16	121	PTB8		PTB8	FTM1CH0		FTM1_QD_PHA		VIU_DE		DCU1_R6	
J19	123	PTB9		PTB9	FTM1CH1		FTM1_QD_PHB				DCU1_R7	
B15	159	PTB10		PTB10	SCI0_TX			DCU0_TCON4	VIU_DE	CKO1	ENET_TS_CLKIN	
D14	164	PTB11		PTB11	SCI0_RX			DCU0_TCON5	SNVS_ALARM_OUT_B	CKO2	ENET0_1588_TMR0	
E13	165	PTB12	NMI	PTB12	SCI0_RTS		SPI0_PCS5	DCU0_TCON6	FB_AD1	NMI	ENET0_1588_TMR1	
D15	156	PTB13		PTB13	SCI0_CTS		SPI0_PCS4	DCU0_TCON7	FB_AD0	TRACECTL		

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B14	162	PTB14		PTB14	CAN0_RX	I2C0_SCL		DCU0_ TCON8			DCU1_PCLK	
A14	161	PTB15		PTB15	CAN0_TX	I2C0_SDA		DCU0_ TCON9			VIU_PIX_ CLK	
C14	163	PTB16		PTB16	CAN1_RX	I2C1_SCL		DCU0_ TCON10				
A15	160	PTB17		PTB17	CAN1_TX	I2C1_SDA		DCU0_ TCON11				
B12	171	PTB18		PTB18	SPI0_PCS1	EXT_AUDIO_ MCLK				VIU_DATA9	CCM_OBS0	
C13	167	PTB19		PTB19	SPI0_PCS0					VIU_DATA10	CCM_OBS1	
A13	169	PTB20		PTB20	SPI0_SIN			LCD42		VIU_DATA11	CCM_OBS2	
E12	173	PTB21		PTB21	SPI0_SOUT			LCD43		VIU_DATA12	DCU1_PCLK	
D12	172	PTB22		PTB22	SPI0_SCK				VIU_FID			
V10	61	USB0_GND			USB0_GND							
T10	63	USB0_DP			USB0_DP							
T9	62	USB0_DM			USB0_DM							
W11	60	USB0_VBUS			USB0_VBUS							
Y10	59	USB_DCAP			USB_DCAP							
Y11	64	USB0_ VBUS_ DETECT			USB0_ VBUS_ DETECT							
Y9	—	USB1_GND			USB1_GND							
W9	—	USB1_DP			USB1_DP							
V9	—	USB1_DM			USB1_DM							
W10	—	USB1_VBUS			USB1_VBUS							
U9	—	USB1_ VBUS_ DETECT			USB1_ VBUS_ DETECT							
L4	8	PTC0		PTC0	RMII0_MDC/ MII0_MDC	FTM1CH0	SPI0_PCS3	ESAI_SCKT	SDHC0_CLK	VIU_DATA0	RCON18	
L5	9	PTC1		PTC1	RMII0_MDIO/ MII0_MDC	FTM1CH1	SPI0_PCS2	ESAI_FST	SDHC0_CMD	VIU_DATA1	RCON19	
M5	11	PTC2		PTC2	RMII0_CRS_ DV	SCI1_TX		ESAI_SDO0	SDHC0_ DAT0	VIU_DATA2	RCON20	
M3	12	PTC3		PTC3	RMII0_RXD1/ MII0_RXD[1]	SCI1_RX		ESAI_SDO1	SDHC0_ DAT1	VIU_DATA3	DCU0_R0	
L2	14	PTC4		PTC4	RMII0_RXD0/ MII0_RXD[0]	SCI1_RTS	SPI1_PCS1	ESAI_SDO2/ ESAI_SDI3	SDHC0_ DAT2	VIU_DATA4	DCU0_R1	
M1	15	PTC5		PTC5	RMII0_RXER/ MII0_RXER	SCI1_CTS	SPI1_PCS0	ESAI_SDO3/ ESAI_SDI2	SDHC0_ DAT3	VIU_DATA5	DCU0_G0	
N1	16	PTC6		PTC6	RMII0_TXD1/ MII0_TXD[1]		SPI1_SIN	ESAI_SDO5/ ESAI_SDI0	SDHC0_WP	VIU_DATA6	DCU0_G1	
N2	17	PTC7		PTC7	RMII0_TXD0/ MII0_TXD[0]		SPI1_SOUT	ESAI_SDO4/ ESAI_SDI1		VIU_DATA7	DCU0_B0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G14	—	VSS			VSS							
J14	—	VSS			VSS							
L14	—	VSS			VSS							
N14	—	VSS			VSS							
N7	—	FA_VDD			FA_VDD							
V14	—	VBAT			VBAT							
—	FLG	VSS			VSS							

12.2 Pinout diagrams

NOTE

The 176 LQFP parts are not pin compatible between the F and R series families devices.

NOTE

If tamper detection is not required, the tamper pins must be tied to ground.

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTC11	P4	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC12	P3	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC13	P1	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC14	R1	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC15	P2	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC16	R3	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC17	R4	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC26	D16	153	VDD33	GPIO	ALT3	RCON24	Input	Disabled
PTC27	E16	154	VDD33	GPIO	ALT3	RCON25	Input	Disabled
PTC28	E15	155	VDD33	GPIO	ALT3	RCON26	Input	Disabled
PTC29	C16	152	VDD33	GPIO	ALT3	RCON27	Input	Disabled
PTC30	T8	58	VDD33	GPIO	ALT3	RCON28	Input	Disabled
PTC31	W5	42	VDD33	GPIO	ALT3	RCON29	Input	Disabled
PTD0	Y17	86	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD1	Y18	87	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD2	V18	88	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD3	Y19	89	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD4	W19	90	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD5	W20	91	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD6	V20	92	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD7	V19	93	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD8	U17	94	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD9	U18	97	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD10	U20	98	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD11	T20	99	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD12	T19	100	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD13	T18	101	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD16	D20	133	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD17	E20	132	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD18	E18	131	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD19	F16	130	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD20	F17	129	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD21	F19	128	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD22	F20	126	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD23	G20	124	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD24	G19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD25	G18	—	VDD33	GPIO	ALT0	GPIO	Disabled	

Table continues on the next page...

Table 82. Revision History

Rev. No.	Date	Substantial Changes
		supply), turn this 1.5 V supply on before turning on the 3.3V." • In "VideoADC specifications" table, added supply current values. • In "Receive and Transmit signal timing specifications," added the following note: "See the most current errata document when using the internally generated RXCLK and TXCLK clocks." • Updated "QuadSPI timing" section, presenting data based on a negative edge data launch from the device and a negative edge data capture; updated the figure, "QuadSPI Input/Read timing (SDR mode)"; updated the table, "QuadSPI Input/Read timing (SDR mode)." • For the "SDHC switching specifcations" table, added the statement, "A load of 50 pF is assumed"; updated max value for SD6, SDHC output delay (output valid). • In the "24 MHz oscillator specifications" section, added the statement, "The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5." • In "Pinouts" section, for the 176LQFP package, added information about exposed pad on the bottom side. • In "Special Signal Considerations" table, added that a "fundamental-mode" crystal should be connected between XTAL and EXTAL; updated maximum drive level of crystal rating to 250 µW.