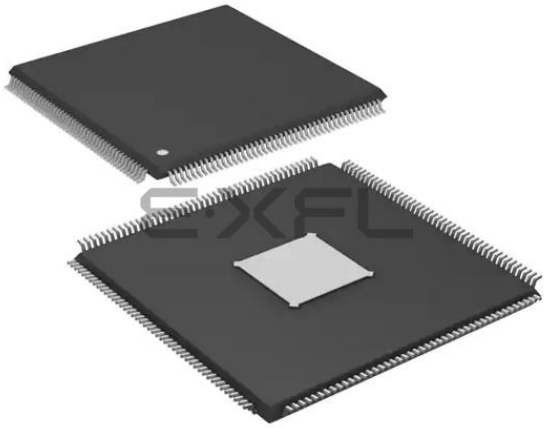

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	No
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-HLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf311r3k2cku2

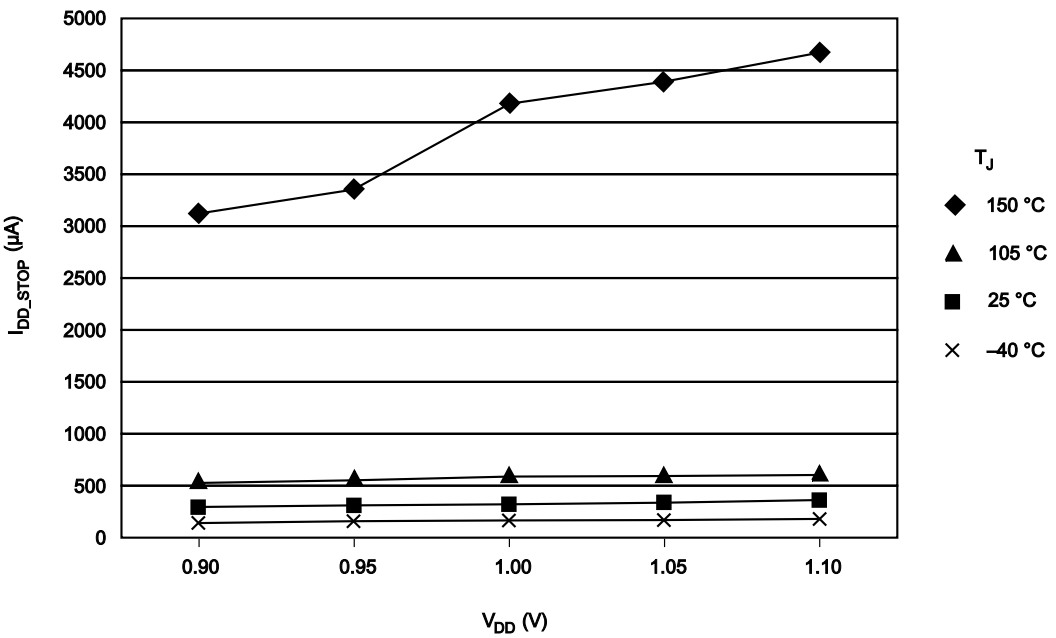
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV

6.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

6.2.8 Capacitance attributes

Table 18. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

7 I/O parameters

7.1 GPIO parameters

Table 19. GPIO DC operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi[1]	Core internal supply voltage		1.2		V
ovdd	I/O output supply voltage	3	3.3	3.6	V

1. This is internally controlled.

Table 20. GPIO DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voh	High-level output voltage	Ioh= -1mA	ovdd-0.15			V

Table continues on the next page...

Table 30. Recommended operating conditions (continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VSSA33_AFE	Ground supply of AFE (Video ADC)			0		V
VSS12_AFE	Ground supply for AFE (Video ADC)			0		V
SDRAMC_VDD1P5	LPDDR2	External CAP 10uF	1.142	1.2	1.26	V
SDRAMC_VDD1P5	DDR3	External CAP 10uF	1.425	1.5	1.575	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	External CAP 10uF	2.25	2.5	2.75	V
-	Maximum power supply ramp rate (Slew limit for power-up)		-		0.1	V/us

1. For customer applications, this is governed by ballast output which is controlled by the device and appropriate voltage ranges are maintained.

8.5 Recommended Connections for Unused Analog Interfaces

NOTE

There are two options to handle unused power pins:

1. Connect all unused supplies to their respective voltage. To save the power, do not enable the module and/or do not enable clock gate to the module.
2. Keep all unused supplies floating.

If pin is shared by several peripheral, then all peripherals connected to multiplexer have to be powered. For example: if pin is shared by GPIO and ADC input and GPIO functionality is used, then ADC has to be powered due to internal structure of the multiplexer. Keep unused input signals grounded if power pins are powered. Keep unused input signals floating if power pins are floating. Keep unused output signals floating.

Module	Name	Recommendation if Unused
ADC	VDDA33_ADC	3.3V or float (Note: Powers both ADC and DAC)
	VREFH_ADC, VREFL_ADC	VREFH_ADC same as VDDA33_ADC VREFL_ADC ground or float
	ADC0SE8, ADC0SE9, ADC1SE8, ADC1SE9	Ground or float
CCM	LVDS0P, LVDS0N	Float
DAC	DACO0, DACO1	Float

Table continues on the next page...

Table 35. VideoADC Specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage	—	0.6	—	V	Bandgap voltage on VADC_AFE_BANDGAP pin. Pin should be decoupled with a 100nF capacitor

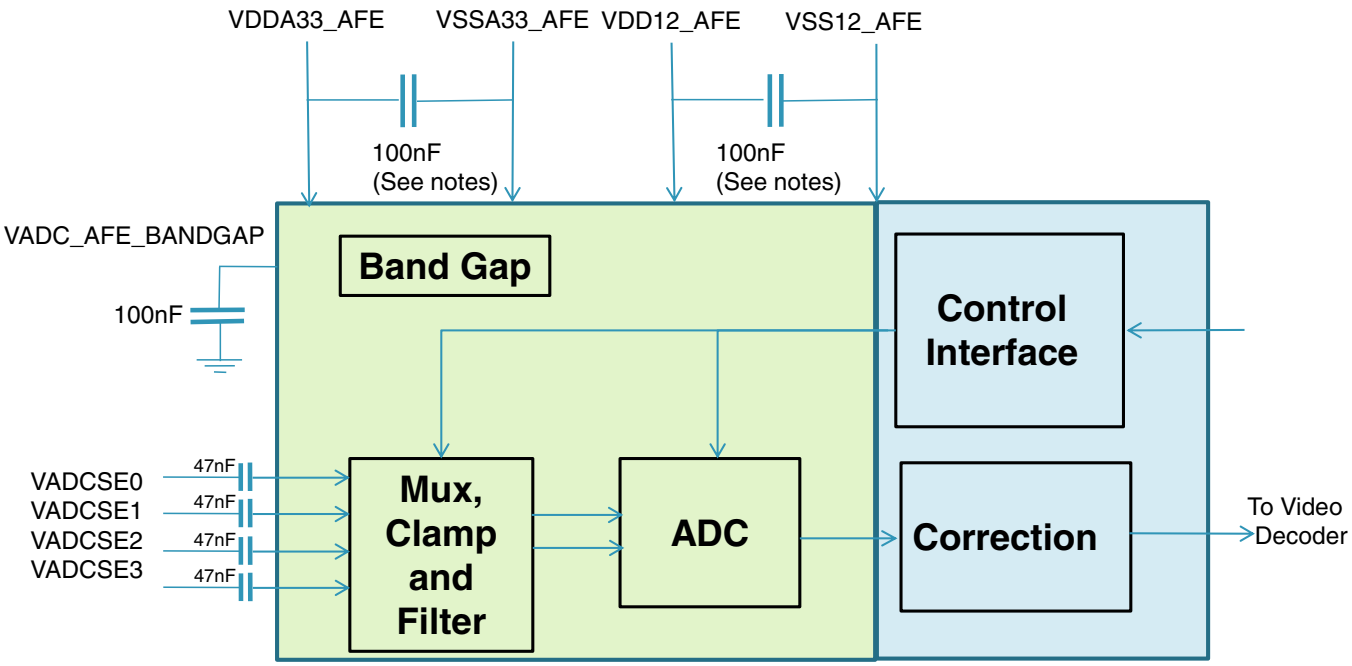


Figure 12. VideoADC supply scheme

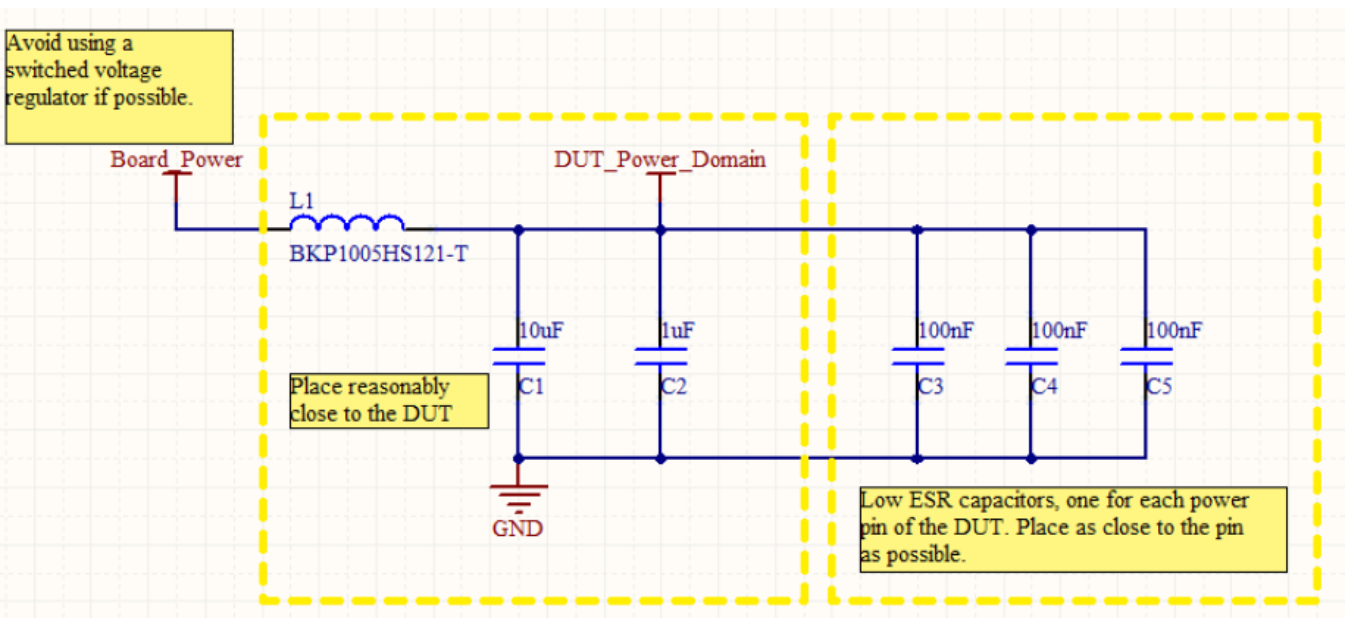
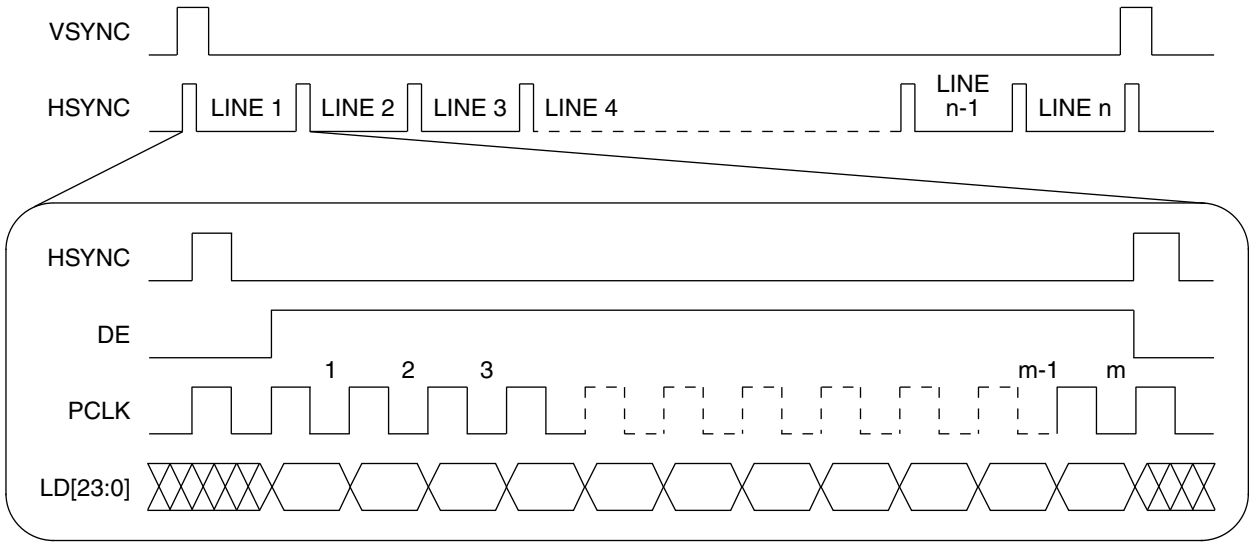


Figure 13. VideoADC supply decoupling



9.2.1.2 Interface to TFT LCD Panels—Pixel Level Timings

This section provides the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the figure below are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high. Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the clock divide . The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 36. LCD interface timing parameters—horizontal and vertical

Symbol	Characteristic		Unit
t_{PCP}	Display pixel clock period	11.2	ns
t_{PWH}	HSYNC pulse width	PW_H * t_{PCP}	ns
t_{BPH}	HSYNC back porch width	BP_H * t_{PCP}	ns
t_{FPH}	HSYNC front porch width	FP_H * t_{PCP}	ns
t_{SW}	Screen width	DELTA_X * t_{PCP}	ns
t_{HSP}	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) * t_{PCP}	ns
t_{PWV}	VSYNC pulse width	PWV * t_{HSP}	ns
t_{BPV}	VSYNC back porch width	BP_V * t_{HSP}	ns
t_{FPV}	VSYNC front porch width	FP_V * t_{HSP}	ns
t_{SH}	Screen height	DELTA_Y * t_{HSP}	ns
t_{VSP}	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) * t_{HSP}	ns

Table 40. Receive signal timing for RMII interfaces (continued)

	Characteristic	RMII Mode		Unit
		Min	Max	
E4, E8	RMII_CLK pulse width low	35%	65%	RMII_CLK period
E1	RXD[1:0], CVS_DV, RXER to RMII_CLK setup	4	—	ns
E2	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
E6	RMII_CLK to TXD[1:0], TXEN valid	—	14	ns
E5	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

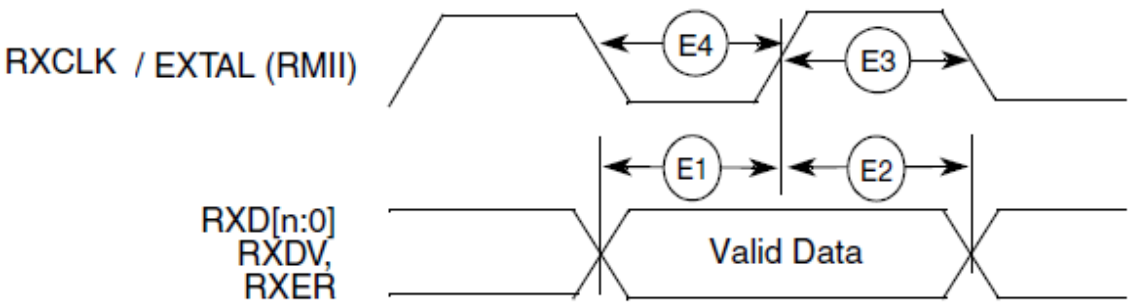


Figure 19. RMII receive signal timing diagram

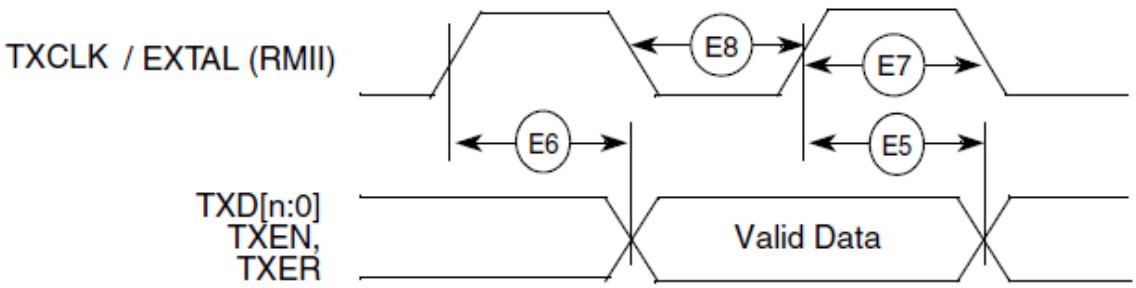


Figure 20. RMII transmit signal timing diagram

NOTE

See the most current device errata document when using the internally generated RXCLK and TXCLK clocks.

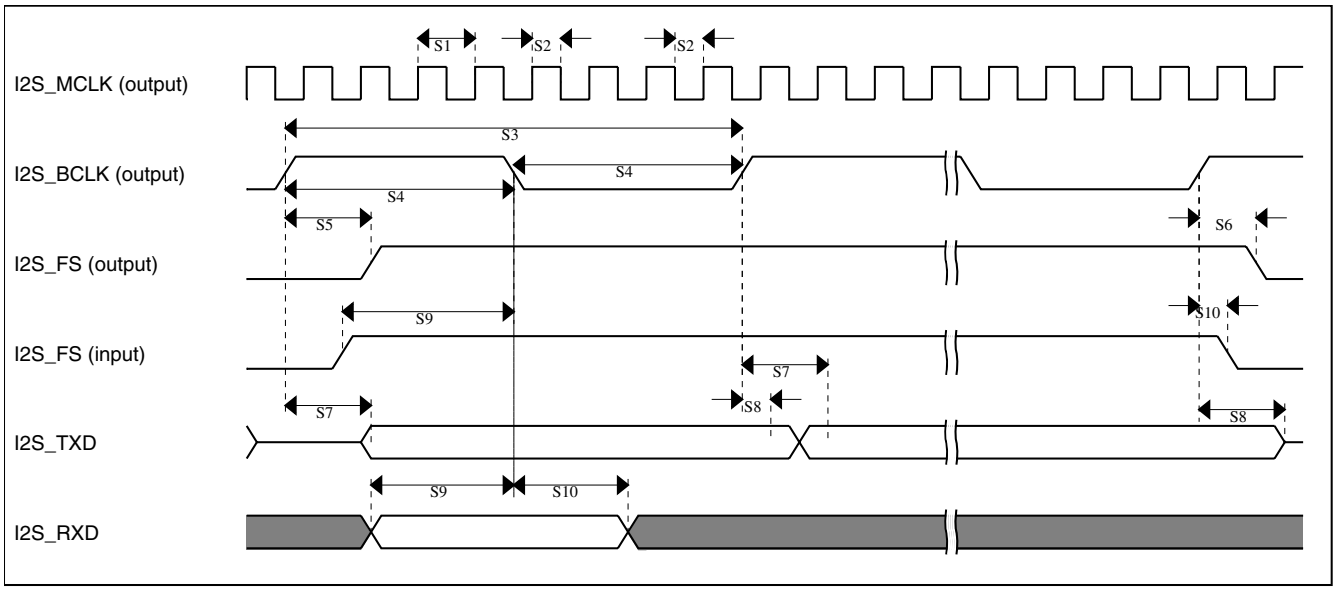


Figure 28. SAI Timing — Master Modes

Table 47. Slave Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{SYS}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FS input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

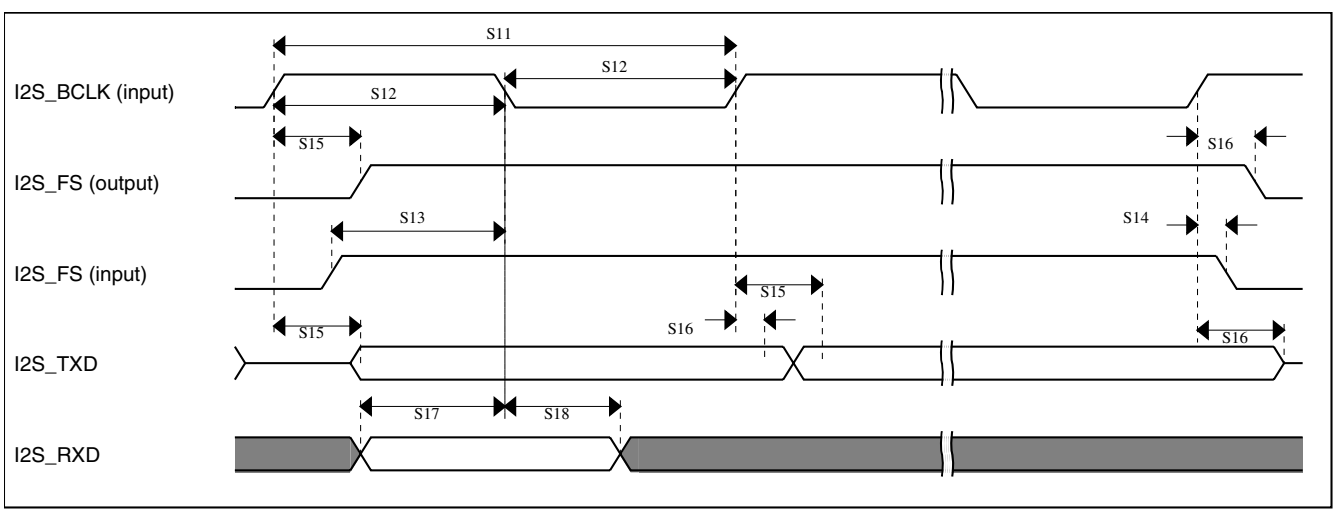


Figure 29. SAI Timing — Slave Modes

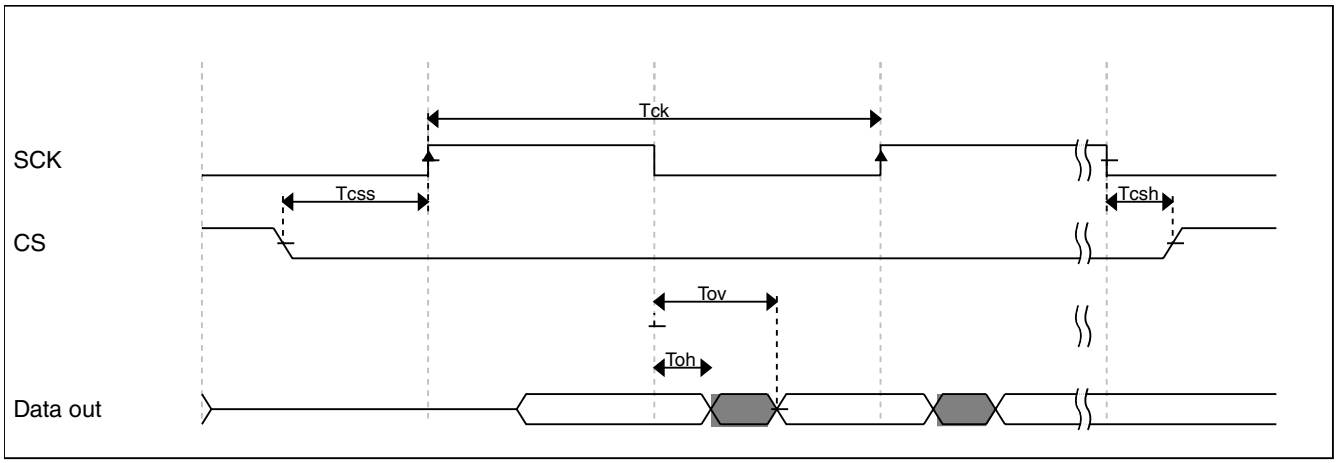


Figure 33. QuadSPI Output/Write timing (DDR mode)

Table 51. QuadSPI Output/Write timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	—	3.2	ns
T_{oh}	Output Data Hold	0	—	ns
T_{ck}	SCK clock period	-	45	MHz
T_{css}	Chip select output setup time	3	-	Clk(sck)
T_{csh}	Chip select output hold time	3	-	Clk(sck)

9.5.2 NFC specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

In the following table:

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$T_{NFC} = T_H + T_L$

NOTE

Refer to the Reference Manual for further details on setting up the NFC clocks (CCM_CSCDR2[NFC_FRAC_DIV_EN + NFC_FRAC_DIV] and CCM_CSCDR3[NFC_PRE_DIV]).

9.5.4 DDR controller specifications

9.5.4.1 DDR3 Timing Parameters

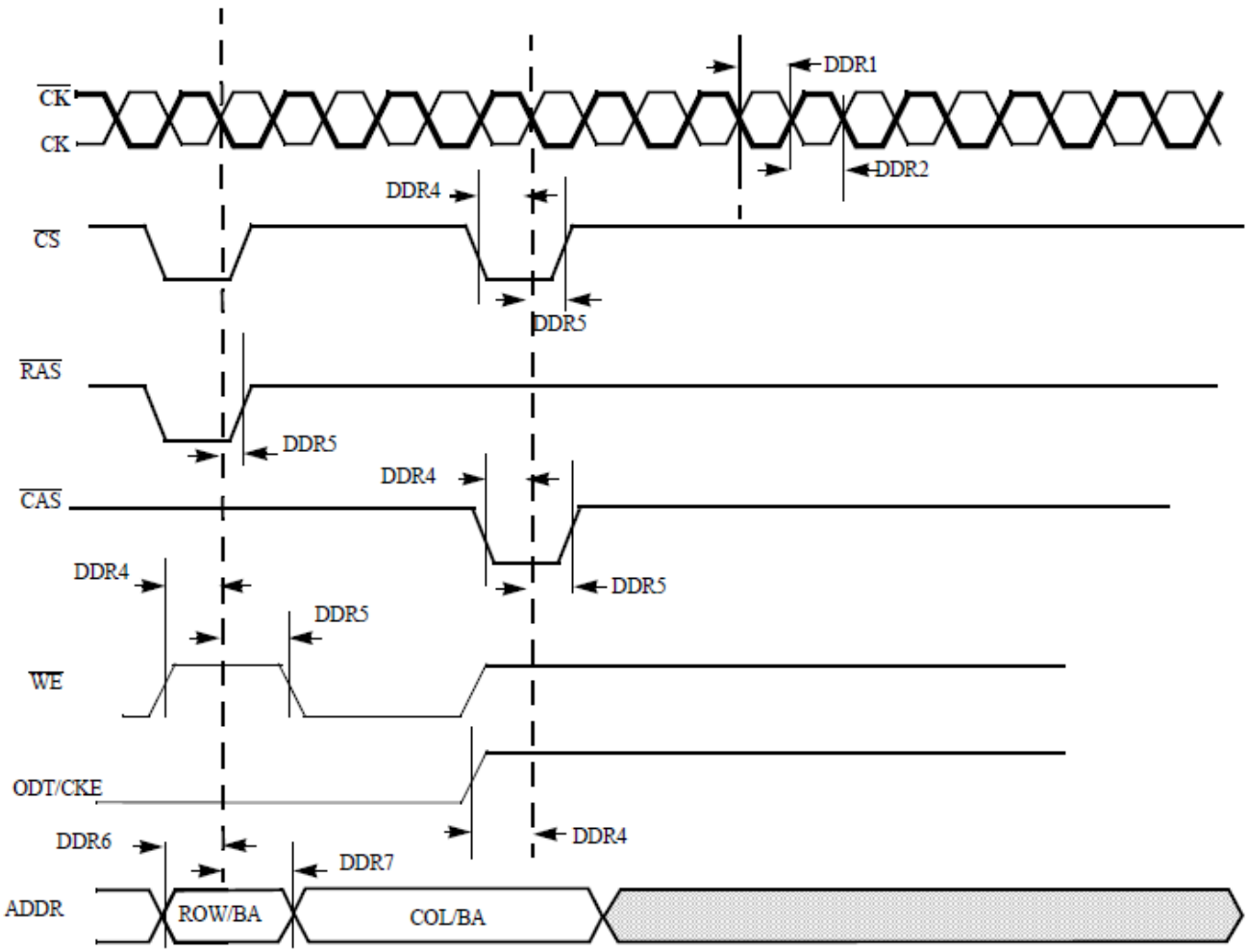


Figure 41. DDR3 Command and Address Timing Parameters

NOTE

RESET pin has a external weak pull DOWN requirement if DDR3 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has a external weak pull UP requirement if DDR3 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 54. DDR3 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tCK
DDR2	CK clock low-level width	tCL	0.47	0.53	tCK
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	440	-	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	315	-	ps
DDR6	Address output setup time	tIS	440	-	ps
DDR7	Address output hold time	tIH	315	-	ps

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.6 LPDDR2 Write Cycle

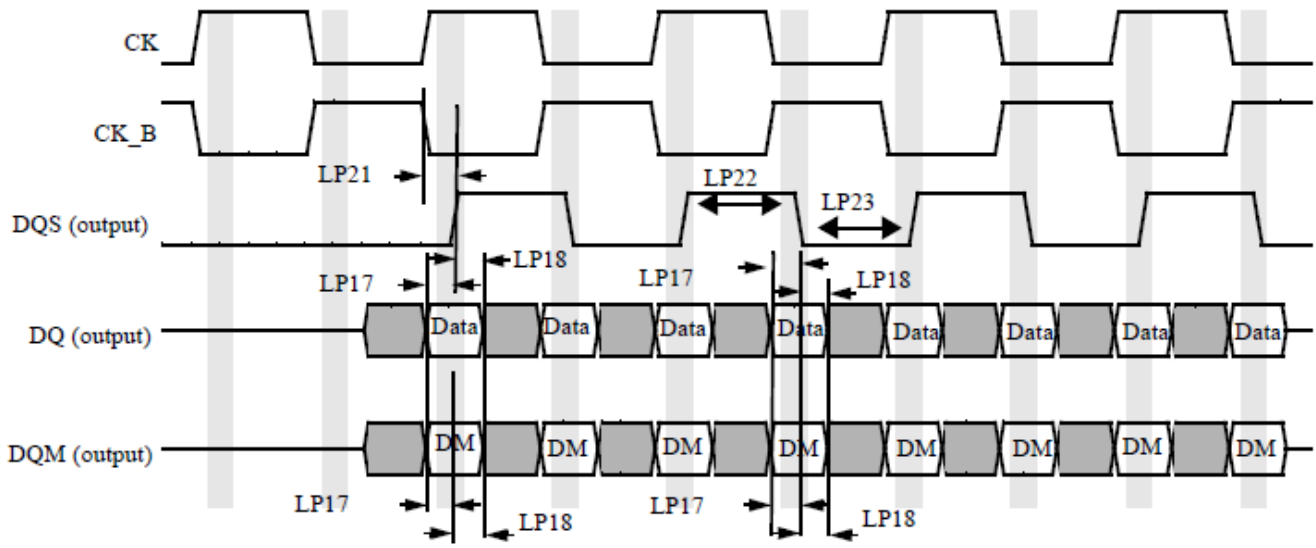


Figure 46. LPDDR3 Write Cycle

Table 59. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	tDS	220	0.55	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	tDH	220	0.55	ps
LP21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
LP22	DQS high level width	tDQSH	0.4	-	tCK
LP23	DQS low level width	tDQSL	0.4	-	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

Table 63. DSPI timing (continued)

No.	Symbol	Characteristic	Condition	Min	Max	Unit
			Slave	4	—	
10	t_{HI}	Data Hold Time for Inputs	Master	0	—	ns
			Slave	2	—	
11	t_{DV}	Data Valid (after SCK edge) for Outputs	Master	—	5	ns
			Slave	—	10	
12	t_{HO}	Data Hold Time for Outputs	Master	0	—	ns
			Slave	0	—	

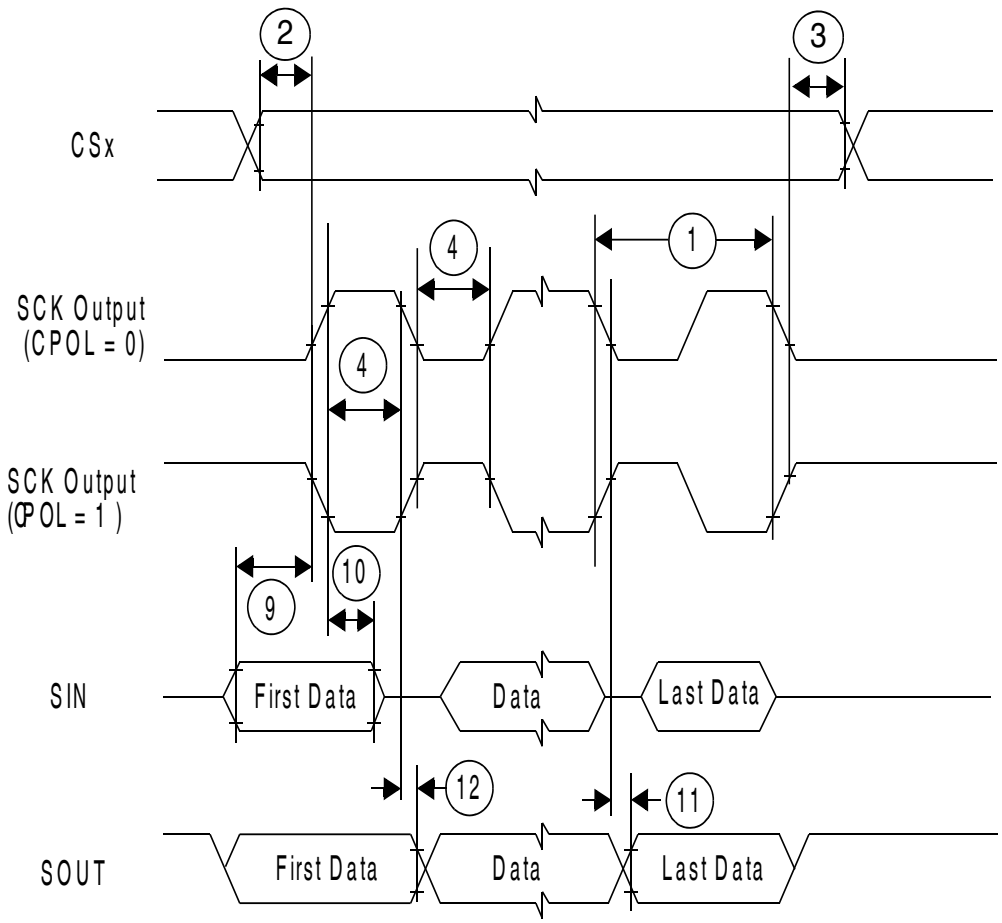


Figure 48. DSPI classic SPI timing master, CPHA=0

9.8.2 Debug trace timing specifications

Table 77. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	50		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	Refer Table 21		ns
T_f	Clock and data fall time Refer			ns
tDV	Data output valid	3	—	ns
tHO	Data output hold	1	—	ns

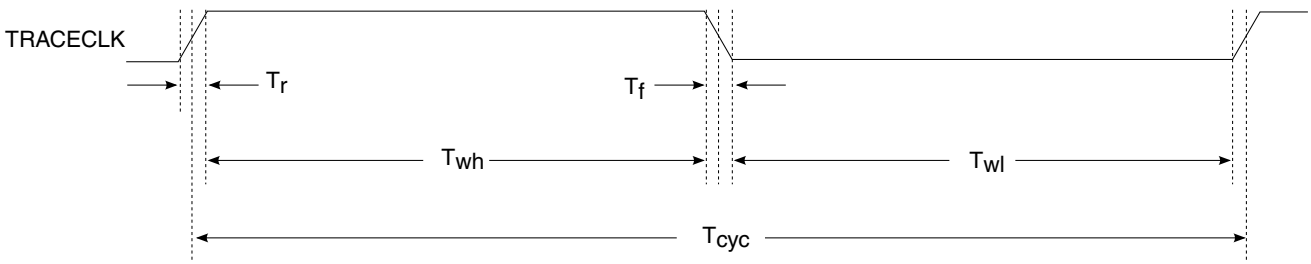


Figure 57. TRACE_CLKOUT specifications

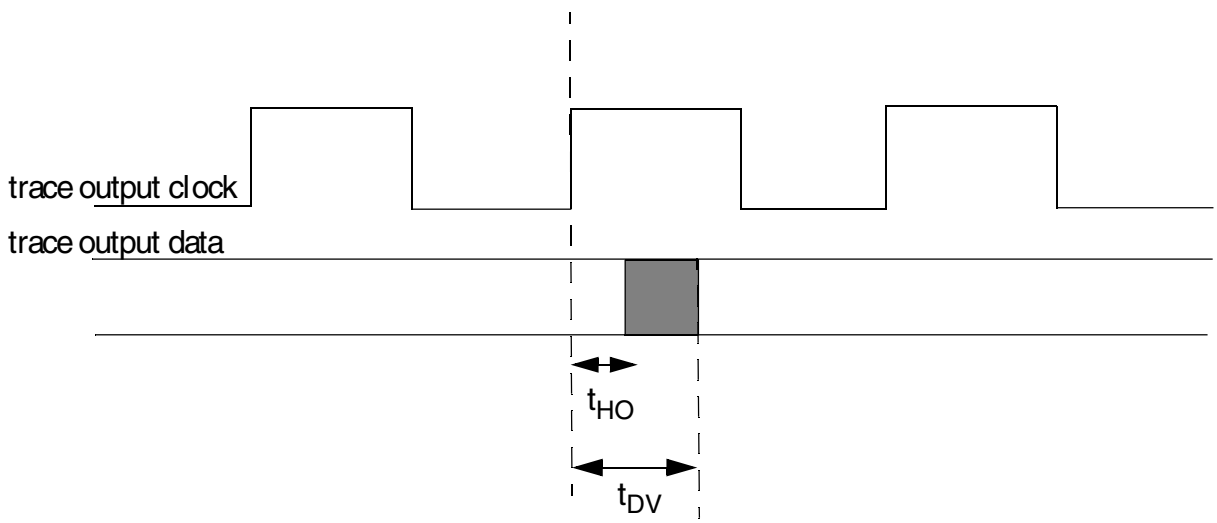
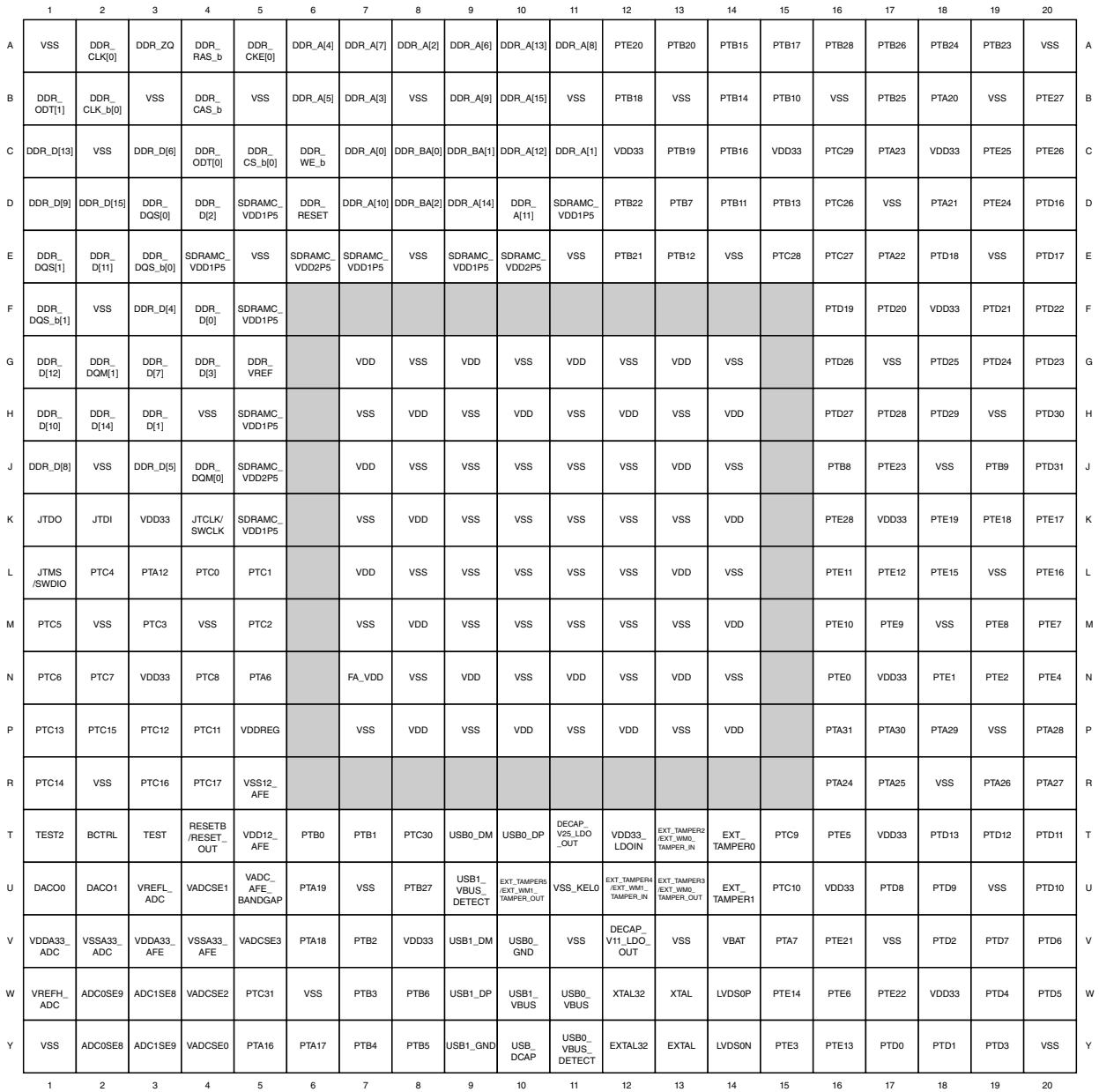


Figure 58. Trace data specifications

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_SYNC	I2C2_SDA	DCU1_DE/DCU1_TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_VBUS_EN			SDHC1_CLK	DCU1_TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_VBUS_OC			SDHC1_CMD	DCU1_TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_BCLK			SDHC1_DAT0	DCU1_TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_BCLK			SDHC1_DAT1	DCU1_TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_DATA	ENET1_1588_TMR0	SCI4_TX	SDHC1_DAT2	DCU1_TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_DATA	ENET1_1588_TMR1	SCI4_RX	SDHC1_DAT3	DCU1_TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_SYNC	ENET1_1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_SYNC	ENET1_1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_BCLK	VIU_DATA18	QSPI1_A_CS0	
T7	50	PTB1	RCON30	PTB1	FTM0_CH1	ADC0_SE3	RCON30	LCD35	SAI2_RX_DATA	VIU_DATA19	QSPI1_A_DATA3	
V7	51	PTB2	RCON31	PTB2	FTM0_CH2	ADC1_SE2	RCON31	LCD36	SAI2_RX_SYNC	VIU_DATA20	QSPI1_A_DATA2	
W7	53	PTB3		PTB3	FTM0_CH3	ADC1_SE3	EXTRIG	LCD37		VIU_DATA21	QSPI1_A_DATA1	
Y7	54	PTB4		PTB4	FTM0_CH4	SCI1_TX	ADC0_SE4	LCD38	VIU_FID	VIU_DATA22	QSPI1_A_DATA0	
Y8	55	PTB5		PTB5	FTM0_CH5	SCI1_RX	ADC1_SE4	LCD39	VIU_DE	VIU_DATA23	QSPI1_A_DQS	
W8	56	PTB6		PTB6	FTM0_CH6	SCI1_RTS	QSPI0_A_CS1	LCD40	FB_CLKOUT	VIU_HSYNC	SCI2_TX	
D13	166	PTB7		PTB7	FTM0_CH7	SCI1_CTS	QSPI0_B_CS1	LCD41		VIU_VSYNC	SCI2_RX	
J16	121	PTB8		PTB8	FTM1CH0		FTM1_QD_PHA		VIU_DE		DCU1_R6	
J19	123	PTB9		PTB9	FTM1CH1		FTM1_QD_PHB				DCU1_R7	
B15	159	PTB10		PTB10	SCI0_TX			DCU0_TCON4	VIU_DE	CKO1	ENET_TS_CLKIN	
D14	164	PTB11		PTB11	SCI0_RX			DCU0_TCON5	SNVS_ALARM_OUT_B	CKO2	ENET0_1588_TMR0	
E13	165	PTB12	NMI	PTB12	SCI0_RTS		SPI0_PCS5	DCU0_TCON6	FB_AD1	NMI	ENET0_1588_TMR1	
D15	156	PTB13		PTB13	SCI0_CTS		SPI0_PCS4	DCU0_TCON7	FB_AD0	TRACECTL		



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	DDR_ CLK[0]	DDR_ZQ	DDR_ RAS_b	DDR_ CKE[0]	DDR_A[4]	DDR_A[7]	DDR_A[2]	DDR_A[6]	DDR_A[13]	DDR_A[8]	PTE20	PTB20	PTB15	PTB17	PTB28	PTB26	PTB24	PTB23	VSS	A
B	DDR_ ODT[1]	DDR_ CLK_b[0]	VSS	DDR_ CAS_b	VSS	DDR_A[5]	DDR_A[3]	VSS	DDR_A[9]	DDR_A[15]	VSS	PTB18	VSS	PTB14	PTB10	VSS	PTB25	PTA20	VSS	PTE27	B
C	DDR_D[13]	VSS	DDR_D[6]	DDR_ ODT[0]	DDR_ CS_b[0]	DDR_ WE_b	DDR_A[0]	DDR_BA[0]	DDR_BA[1]	DDR_A[12]	DDR_A[1]	VDD33	PTB19	PTB16	VDD33	PTC29	PTA23	VDD33	PTE25	PTE26	C
D	DDR_D[9]	DDR_D[15]	DDR_ DQS[0]	DDR_ D[2]	SDRAMC_ VDD1P5	DDR_ RESET	DDR_A[10]	DDR_BA[2]	DDR_A[14]	DDR_ A[11]	SDRAMC_ VDD1P5	PTB22	PTB7	PTB11	PTB13	PTC26	VSS	PTA21	PTE24	PTD16	D
E	DDR_ DQS[1]	DDR_ D[11]	DDR_ DQS_b[0]	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD2P5	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD1P5	SDRAMC_ VDD2P5	VSS	PTB21	PTB12	VSS	PTC28	PTC27	PTA22	PTD18	VSS	PTD17	E
F	DDR_ DQS_b[1]	VSS	DDR_D[4]	DDR_ D[0]	SDRAMC_ VDD1P5											PTD19	PTD20	VDD33	PTD21	PTD22	F
G	DDR_ D[12]	DDR_ DQM[1]	DDR_ D[7]	DDR_ D[3]	DDR_ VREF		VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTD26	VSS	PTD25	PTD24	PTD23	G
H	DDR_ D[10]	DDR_ D[14]	DDR_ D[1]	VSS	SDRAMC_ VDD1P5		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTD27	PTD28	PTD29	VSS	PTD30	H
J	DDR_D[8]	VSS	DDR_D[5]	DDR_ DQM[0]	SDRAMC_ VDD2P5		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTB8	PTE23	VSS	PTB9	PTD31	J
K	JTDO	JTDI	VDD33	JTCLK/ SWCLK	SDRAMC_ VDD1P5		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE28	VDD33	PTE19	PTE18	PTE17	K
L	JTMS /SWDIO	PTC4	PTA12	PTC0	PTC1		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTE11	PTE12	PTE15	VSS	PTE16	L
M	PTC5	VSS	PTC3	VSS	PTC2		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE10	PTE9	VSS	PTE8	PTE7	M
N	PTC6	PTC7	VDD33	PTC8	PTA6		FA_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTE0	VDD33	PTE1	PTE2	PTE4	N
P	PTC13	PTC15	PTC12	PTC11	VDDREG		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTA31	PTA30	PTA29	VSS	PTA28	P
R	PTC14	VSS	PTC16	PTC17	VSS12_ AFE											PTA24	PTA25	VSS	PTA26	PTA27	R
T	TEST2	BCTRL	TEST	RESETB /RESET_ OUT	VDD12_ AFE	PTB0	PTB1	PTC30	USB0_DM	USB0_DP	DECAP_ V25_LDO _OUT	VDD33_ LDOIN	EXT_TAMPER2 /EXT_WM0_ TAMPER_IN	EXT_ TAMPER0	PTC9	PTE5	VDD33	PTD13	PTD12	PTD11	T
U	DACO0	DACO1	VREFL_ ADC	VADCSE1	VADC_ AFE_ BANDGAP	PTA19	VSS	PTB27	USB1_ VBUS_ DETECT	EXT_TAMPER5 /EXT_WM1_ TAMPER_OUT	VSS_KEL0	EXT_TAMPER4 /EXT_WM1_ TAMPER_IN	EXT_TAMPER3 /EXT_WM0_ TAMPER_OUT	EXT_ TAMPER1	PTC10	VDD33	PTD8	PTD9	VSS	PTD10	U
V	VDDA33_ ADC	VSSA33_ ADC	VDDA33_ AFE	VSSA33_ AFE	VADCSE3	PTA18	PTB2	VDD33	USB1_DM	USB0_ GND	VSS	DECAP_ V11_LDO_ OUT	VSS	VBAT	PTA7	PTE21	VSS	PTD2	PTD7	PTD6	V
W	VREFH_ ADC	ADC0SE9	ADC1SE8	VADCSE2	PTC31	VSS	PTB3	PTB6	USB1_DP	USB1_ VBUS	USB0_ VBUS	XTAL32	XTAL	LVDS0P	PTE14	PTE6	PTE22	VDD33	PTD4	PTD5	W
Y	VSS	ADC0SE8	ADC1SE9	VADCSE0	PTA16	PTA17	PTB4	PTB5	USB1_GND	USB_ DCAP	USB0_ VBUS_ DETECT	EXTAL32	EXTAL	LVDS0N	PTE3	PTE13	PTD0	PTD1	PTD3	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 60. 364-pin BGA package ballmap

12.2.1 GPIO Mapping

Table 78. RGPIO versus Pins

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[0]	PORT0[0]	PTA6	IOMUXC_PTA6	40048000

Table continues on the next page...

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[40]	PORT1[8]	PTB18	IOMUXC_PTB18	400480A0
RGPIO[41]	PORT1[9]	PTB19	IOMUXC_PTB19	400480A4
RGPIO[42]	PORT1[10]	PTB20	IOMUXC_PTB20	400480A8
RGPIO[43]	PORT1[11]	PTB21	IOMUXC_PTB21	400480AC
RGPIO[44]	PORT1[12]	PTB22	IOMUXC_PTB22	400480B0
RGPIO[45]	PORT1[13]	PTC0	IOMUXC_PTC0	400480B4
RGPIO[46]	PORT1[14]	PTC1	IOMUXC_PTC1	400480B8
RGPIO[47]	PORT1[15]	PTC2	IOMUXC_PTC2	400480BC
RGPIO[48]	PORT1[16]	PTC3	IOMUXC_PTC3	400480C0
RGPIO[49]	PORT1[17]	PTC4	IOMUXC_PTC4	400480C4
RGPIO[50]	PORT1[18]	PTC5	IOMUXC_PTC5	400480C8
RGPIO[51]	PORT1[19]	PTC6	IOMUXC_PTC6	400480CC
RGPIO[52]	PORT1[20]	PTC7	IOMUXC_PTC7	400480D0
RGPIO[53]	PORT1[21]	PTC8	IOMUXC_PTC8	400480D4
RGPIO[54]	PORT1[22]	PTC9	IOMUXC_PTC9	400480D8
RGPIO[55]	PORT1[23]	PTC10	IOMUXC_PTC10	400480DC
RGPIO[56]	PORT1[24]	PTC11	IOMUXC_PTC11	400480E0
RGPIO[57]	PORT1[25]	PTC12	IOMUXC_PTC12	400480E4
RGPIO[58]	PORT1[26]	PTC13	IOMUXC_PTC13	400480E8
RGPIO[59]	PORT1[27]	PTC14	IOMUXC_PTC14	400480EC
RGPIO[60]	PORT1[28]	PTC15	IOMUXC_PTC15	400480F0
RGPIO[61]	PORT1[29]	PTC16	IOMUXC_PTC16	400480F4
RGPIO[62]	PORT1[30]	PTC17	IOMUXC_PTC17	400480F8
RGPIO[63]	PORT1[31]	PTD31	IOMUXC_PTD31	400480FC
RGPIO[64]	PORT2[0]	PTD30	IOMUXC_PTD30	40048100
RGPIO[65]	PORT2[1]	PTD29	IOMUXC_PTD29	40048104
RGPIO[66]	PORT2[2]	PTD28	IOMUXC_PTD28	40048108
RGPIO[67]	PORT2[3]	PTD27	IOMUXC_PTD27	4004810C
RGPIO[68]	PORT2[4]	PTD26	IOMUXC_PTD26	40048110
RGPIO[69]	PORT2[5]	PTD25	IOMUXC_PTD25	40048114
RGPIO[70]	PORT2[6]	PTD24	IOMUXC_PTD24	40048118
RGPIO[71]	PORT2[7]	PTD23	IOMUXC_PTD23	4004811C
RGPIO[72]	PORT2[8]	PTD22	IOMUXC_PTD22	40048120
RGPIO[73]	PORT2[9]	PTD21	IOMUXC_PTD21	40048124
RGPIO[74]	PORT2[10]	PTD20	IOMUXC_PTD20	40048128
RGPIO[75]	PORT2[11]	PTD19	IOMUXC_PTD19	4004812C
RGPIO[76]	PORT2[12]	PTD18	IOMUXC_PTD18	40048130
RGPIO[77]	PORT2[13]	PTD17	IOMUXC_PTD17	40048134
RGPIO[78]	PORT2[14]	PTD16	IOMUXC_PTD16	40048138

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Table 79. Special Signal Considerations (continued)

Special Signal	Comments
JTCLK, JTDI, JTDO, JTMS	For JTAG the use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is matched. For example, do not use an external pull down on an input that has on-chip pull-up. JTDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTDO is detrimental and should be avoided.
LVDS0N, LVDS0P	Not recommended for application use, intended for clock observation purposes during debug only.
RESETB/RESET_OUT	Active low input used to generate a system wide reset (except the SRTC). A glitch filter is include to help prevent unexpected resets, a minimum pulse width of 125 nsecs is required to guarantee a reset is detected.
XTAL, EXTAL	A 24.0 MHz fundamental mode crystal should be connected between XTAL and EXTAL. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTAL must be directly driven by the external oscillator and EXTAL floated. The XTAL signal level must swing from ~0.8 x DECAP_V11_ LDO_OUT to ~0.2 V.
XTAL32, EXTAL32	If the user wishes to configure XTAL32 and EXTAL32 as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between XTAL32 and EXTAL32. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTAL32 and EXTAL32 to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTAL32 and EXTAL32 should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTAL32 the EXTAL32 pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed DECAP_V11_ LDO_OUT level and the frequency should be <100 kHz under typical conditions. In the case where the SIRC is used, it is recommended to connect XTAL32 to ground and leave EXTAL32 floating.

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_A[1]	C11	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[1]	—	—
DDR_A[2]	A8	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[2]	—	—
DDR_A[3]	B7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[3]	—	—
DDR_A[4]	A6	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[4]	—	—
DDR_A[5]	B6	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[5]	—	—
DDR_A[6]	A9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[6]	—	—
DDR_A[7]	A7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[7]	—	—
DDR_A[8]	A11	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[8]	—	—
DDR_A[9]	B9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[9]	—	—
DDR_A[10]	D7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[10]	—	—
DDR_A[11]	D10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[11]	—	—
DDR_A[12]	C10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[12]	—	—
DDR_A[13]	A10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[13]	—	—
DDR_A[14]	D9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[14]	—	—
DDR_A[15]	B10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[15]	—	—
DDR_BA[0]	C8	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[0]	—	—
DDR_BA[1]	C9	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[1]	—	—
DDR_BA[2]	D8	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[2]	—	—
DDR_CAS_ b	B4	—	SDRAMC_ VDD2P5	DDR	—	DDR_CAS_ b	—	—
DDR_CKE[0]	A5	—	SDRAMC_ VDD2P5	DDR	—	DDR_CKE[0]	—	—
DDR_CLK[0]	A2	—	SDRAMC_ VDD2P5	DDR	—	DDR_CLK[0]	—	—

Table continues on the next page...

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_CLK_b[0]	B2	—	SDRAMC_VDD2P5	DDR	—	DDR_CLK_b[0]	—	—
DDR_CS_b[0]	C5	—	SDRAMC_VDD2P5	DDR	—	DDR_CS_b[0]	—	—
DDR_D[0]	F4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[0]	—	—
DDR_D[1]	H3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[1]	—	—
DDR_D[2]	D4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[2]	—	—
DDR_D[3]	G4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[3]	—	—
DDR_D[4]	F3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[4]	—	—
DDR_D[5]	J3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[5]	—	—
DDR_D[6]	C3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[6]	—	—
DDR_D[7]	G3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[7]	—	—
DDR_D[8]	J1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[8]	—	—
DDR_D[9]	D1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[9]	—	—
DDR_D[10]	H1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[10]	—	—
DDR_D[11]	E2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[11]	—	—
DDR_D[12]	G1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[12]	—	—
DDR_D[13]	C1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[13]	—	—
DDR_D[14]	H2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[14]	—	—
DDR_D[15]	D2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[15]	—	—
DDR_DQM[0]	J4	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[0]	—	—
DDR_DQM[1]	G2	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[1]	—	—
DDR_DQS[0]	D3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[0]	—	—

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Removed Temperature Voltage Monitor section to security RM • Updated VideoADC Specifications table
Rev 5	April 2013	Updated pin muxing table with the following changes: • Added MII0 including M AC0.TXDATA[2], MAC0.TXDATA[3], MAC0.RXDATA[2], MAC0.RXDATA[3] , MAC0.TXERR, MAC0.TXCLK, MAC0.RXCLK, MAC0.COL, MAC0.CRS • Following signals muxed on same RMII0 Pins : MII0_MDC, MII0_MDC, MII0_RXD[1], MII0_RXD[0], MII0_RXER, MII0_TXD[1], MII0_TXD[0], MII0_TXEN • Replaced FB_ALE with FB_MUXED_ALE, FB_CS4_b with FB_MUXED_TSIZ0, FB_TSIZ1 with FB_MUXED_TSIZ1, FB_TBST_b with FB_MUXED_TBST_b, FB_BE0_b with FB_MUXED_BE0_b • Removed RCON18,19,20 • Replaced ESAI_SDO2 with ESAI_SDO2/ESAI_SDI3 Replaced ESAI_SDO3 with ESAI_SDO3/ ESAI_SDI2 Replaced ESAI_SDI0 with ESAI_SDO5/ESAI_SDI0 Replaced ESAI_SDI1 with ESAU_SDO4/ESAI_SDI1 • CKO1 additionally muxed at PAD40
Rev 5	May 2013	In the Features, minor editorial updates Added Part Number Format figure Updated the Fields table as per the device part numbers Added Part Numbers table Added External NPN Ballast section In the LVD Dig Electrical Specs, minimum value of Upper Voltage Threshold and Lower Voltage threshold In the FlexBus timing specifications table, clarified the Frequency of operation In the Power consumption, filled TBDs. Updated footnotes

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