Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-HLQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=svf312r3k1cku2

Table 28. Power sequencing (continued)

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VDD33_LDOIN	VDD33	LDO input supply (LDO1P1, LDO2P5, LDO1P1_RTC)	1	VDD33_LDOIN,VDDREG and VDD33 should come from a common supply source (represented as 3.3V SMPS in the Figure 4)
VDDREG	VDD33	Device PMU regulator and External ballast supply	1	
VDD33	VDD33	GPIO 3.3V IO supply, LCD Supply	1	
SDRAMC_VDD1P5	SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	NA	In case the Ballast transistor's collector is connected to the 1.5V DRAM supply (instead of the 3.3V supply), turn this 1.5V supply on before turning on the 3.3V.
VDDA33_ADC	VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	1	
VREFH_ADC	VREFH_ADC	High Reference of ADC, DAC	1	
VDDA33_AFE	VDDA33_AFE	3.3V supply of AFE (Video ADC)	1	
VDD12_AFE	VDD	1.2V supply for AFE (Video ADC)	2	
FA_VDD	VDD	Shorted with VDD at Board Level in 364BGA (Test pin only)	NA	
VDD	VDD	1.2V core supply from External ballast	2	
USB0_VBUS	USB_VBUS	VBUS supply for USB	NA	
USB1_VBUS	USB_VBUS	VBUS supply for USB	NA	

NOTE

NA stands for no sequencing needs, for example, the supply can come in any order.

NOTE

All supplies grouped together e.g. 1,2, others. These have no power sequencing restriction in between them.

NOTE

If none of the SDRAMC pins are connected on the board, the SDRAMC supply could be left floating.

NOTE

At power up, 1.2V supply will follow 3.3V supply. At power down, it should be checked that 1.2V falls before 3.3V.

NOTE

The standby current on USBx_VBUS is 300 - 500 uA. This is well below the 2.5 mA limit set by the USB 2.0 specification. This supply will be ON for applications that need to monitor the

8.4 Recommended operating conditions

Table 30. Recommended operating conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
USB0_VBUS	VBUS supply for USB w.r.t USB0_GND		4.4	5	5.25	V
USB1_VBUS	VBUS supply for USB w.r.t USB1_GND		4.4	5	5.25	V
USB_DCAP	USB LDO 5V->3 V Output	External DCAP (10uF termination for USBREG)		3		V
VBAT	Battery supply in case of LDOIN fails	External CAP 0.1uF	2.4	3.3	3.6	V
VDD33_LDOIN	LDO input supply		3	3.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	Recommended External DCAP: 1uF(Min) 10uF (Max)		1.1		V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR pre-driver, EFUSE	Recommended External DCAP: 1uF(Min) 10uF (Max)		2.5		V
VDD33	GPIO 3.3V IO supply	External CAP (10uF)	3	3.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	External CAP (10uF)	3	3.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	External CAP (10uF)	3	3.3	3.6	V
VREFH_ADC	High reference voltage for ADC and DAC	Relation with VDDDA33_ADC (1uF)	2.5	3.3	VDDA33_ADC	V
VREFL_ADC	Low reference voltage for ADC and DAC	External CAP (10uF)		0		V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	External CAP 10uF	3	3.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)		1.16	1.23	1.26	V
FA_VDD	For testing purpose only should be shorted to VDD on board.		1.16	1.23	1.26	V
VDD[1]	1.2V core supply	4.7uF with a low ESR value (100 milliohms)	1.16	1.23	1.26	V
USB0_GND	Ground supply for USB			0		V
USB1_GND	Ground supply for USB			0		V
VSS_KEL0	USB LDO ground output			0		V
VSS	VSS ground			0		V
VSSA33_ADC	Ground supply for ADC, DAC and IO segment			0		V

Table continues on the next page...

Table 31. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	-	-	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	-	40	MHz	-
	ADLPC=0, ADHSC=0 12 bit mode		4	-	30	MHz	-
	ADLPC=1, ADHSC=0 12 bit mode		4	-	20	MHz	-

1. Typical values assume VDDAD = 3.3 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference

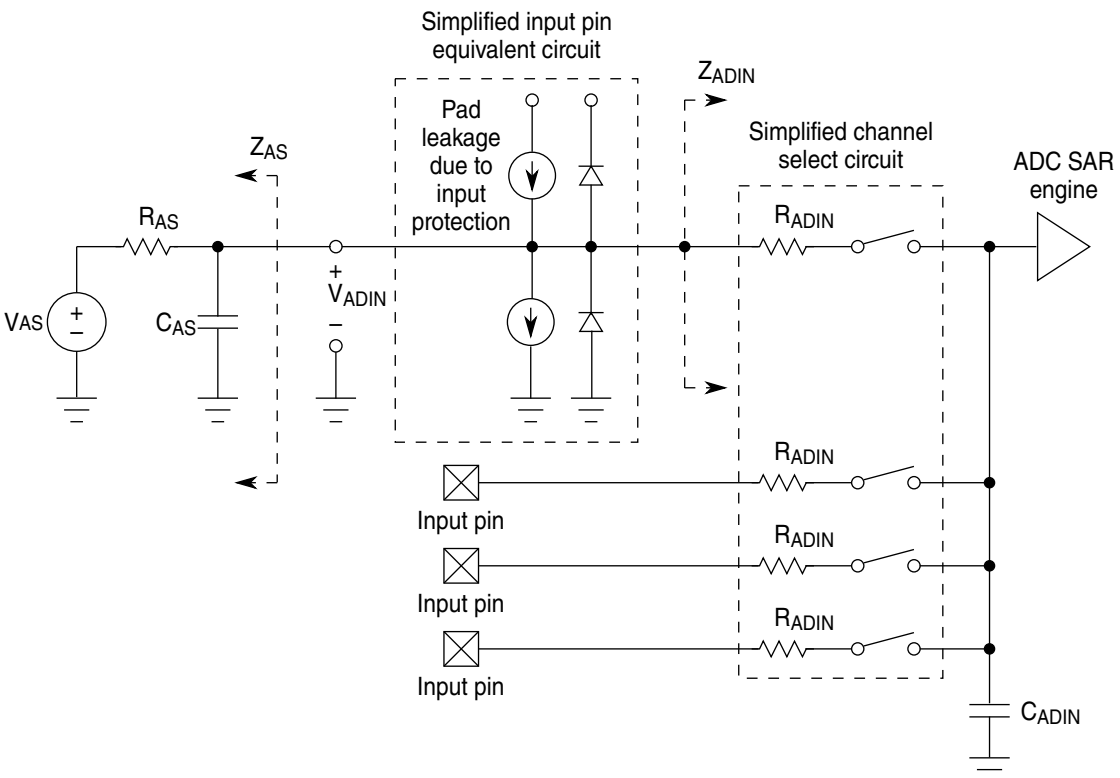

Figure 5. 12-bit ADC Input Impedance Equivalency Diagram

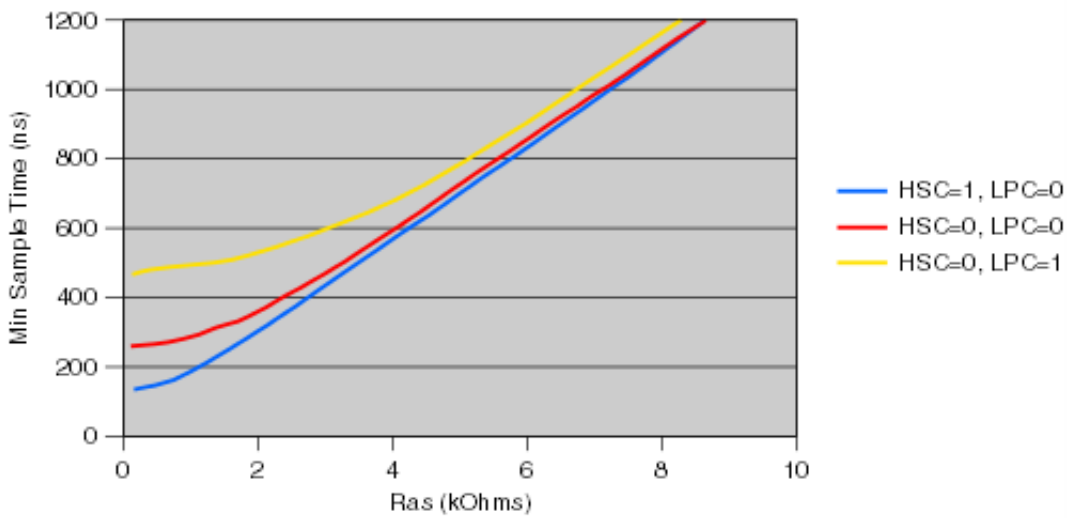

Figure 8. Minimum Sample Time Vs Ras (Cas = 10pF)

9.1.2 12-bit DAC electrical characteristics

9.1.2.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Typ	Max.	Unit	Notes
VDDA33_ADC	Supply voltage	3.0	3.3	3.6	V	
VREFH_ADC	Reference voltage	2.5	3.3	VDDA33_ADC	V	1
C_L	Output load capacitance	—		100	pF	2
I_L	Output load current	—		1	mA	

1. User will need to set up DACx_STATCTRL [DACRFS]=1 to select the valid VREFH_ADC reference. When DACx_STATCTRL [DACRFS]=0, the DAC reference is connected to an internal ground node and is not a valid voltage reference. Note that the DAC and ADC share the VREFH_ADC reference simultaneously.)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

9.1.2.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	100	μA	
I_{DDA_DACHP}	Supply current — high-power mode	—	—	500	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	10	15	μs	

Table continues on the next page...

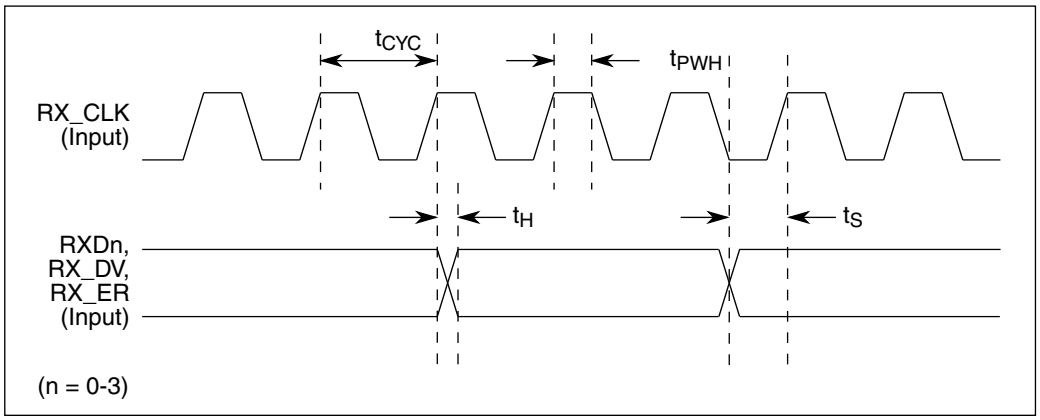

Figure 21. MII receive signal timing diagram

Table 41. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_S	5			ns
Input setup time after RX_CLK	t_H	5			ns

9.3.3 Receive and Transmit signal timing specifications for MII interfaces

This section provides timing specs that meet the requirements for MII interfaces for a range of transceiver devices.

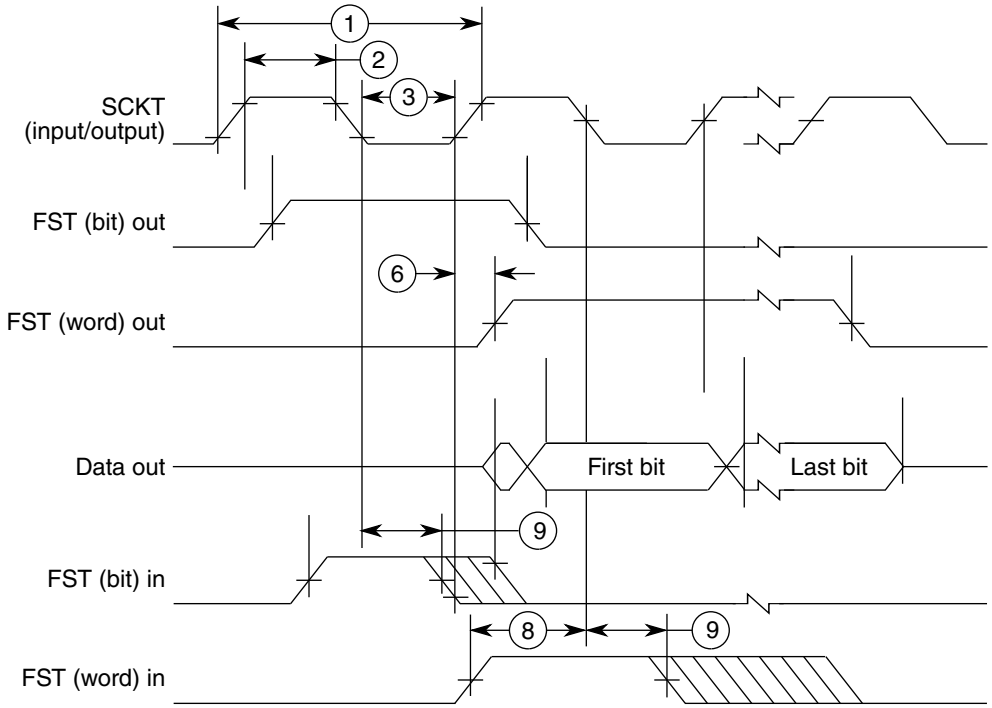

Figure 24. ESAI Transmitter Timing

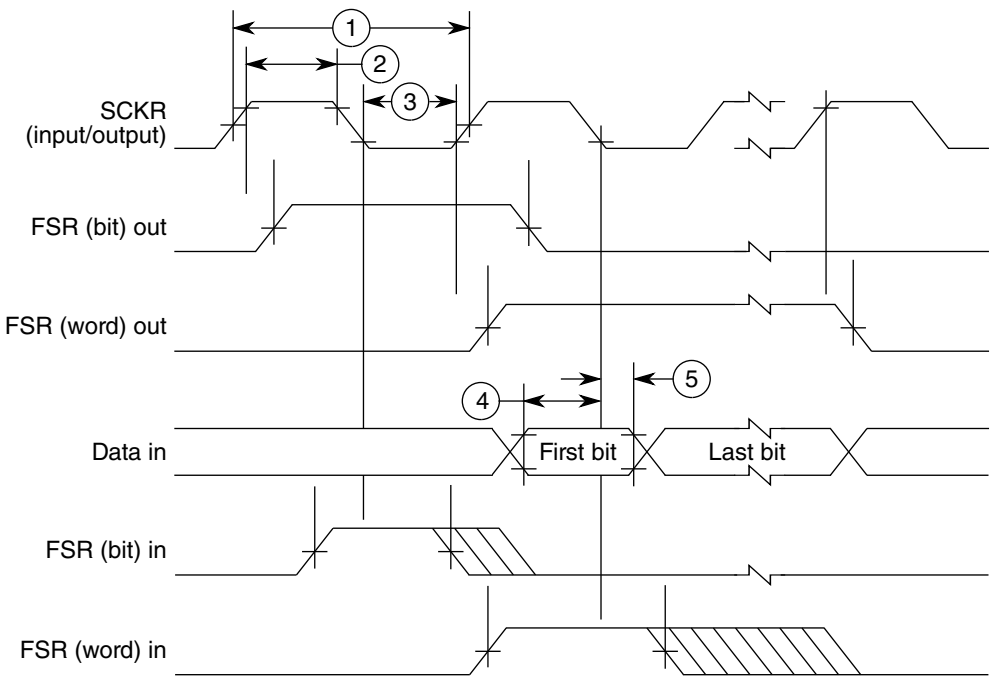

Figure 25. ESAI Receiver Timing

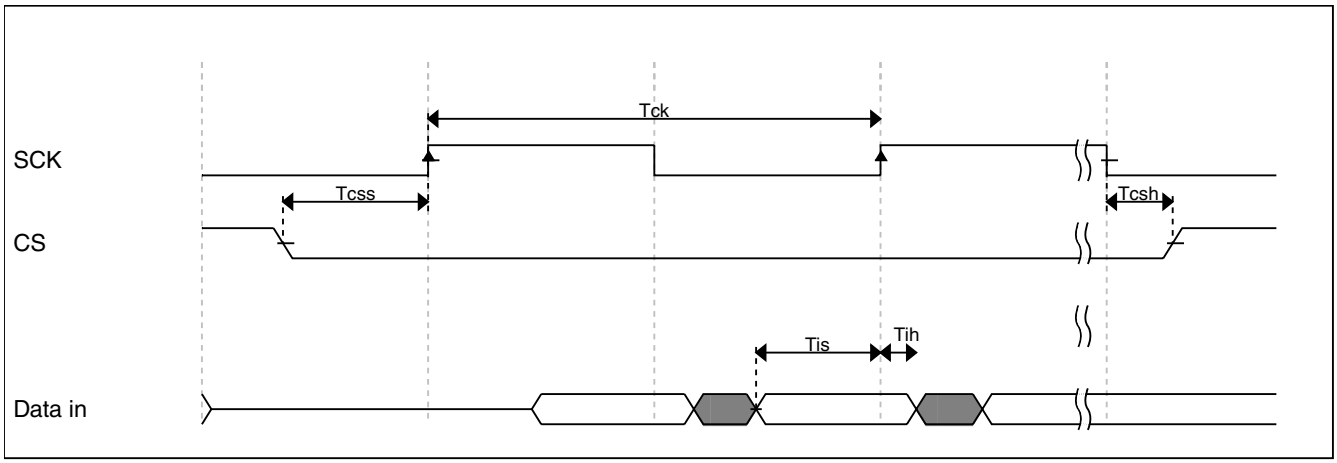

Figure 32. QuadSPI Input/Read timing (DDR mode)

NOTE

- The numbers are for a setting of 0x1 in regiater QuadSPI_SMPR[DDRSMP]
- Read frequency calculations should be: SCK/2 > (flash access time) + Setup (Tis) - (QuadSPI_SMPR[DDRSMP])x SCK/4
- Frequency calculator guideline (Max read frequency): SCK/2 > (Flash access time)max + (Tis)max - (QuadSPI_SMPR[DDRSMP]) xSCK/4
- Hold timing: flash_access (min) + flash_data_valid (min) > SCK/2 + HOLD(Tih) + (QuadSPI_SMPR[DDRSMP])SCK/4
- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.

Table 50. QuadSPI Input/Read timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	6.4	—	ns
T_{ih}	Hold time requirement for incoming data	-3.0	—	ns

NOTE

9.5.4 DDR controller specifications

9.5.4.1 DDR3 Timing Parameters

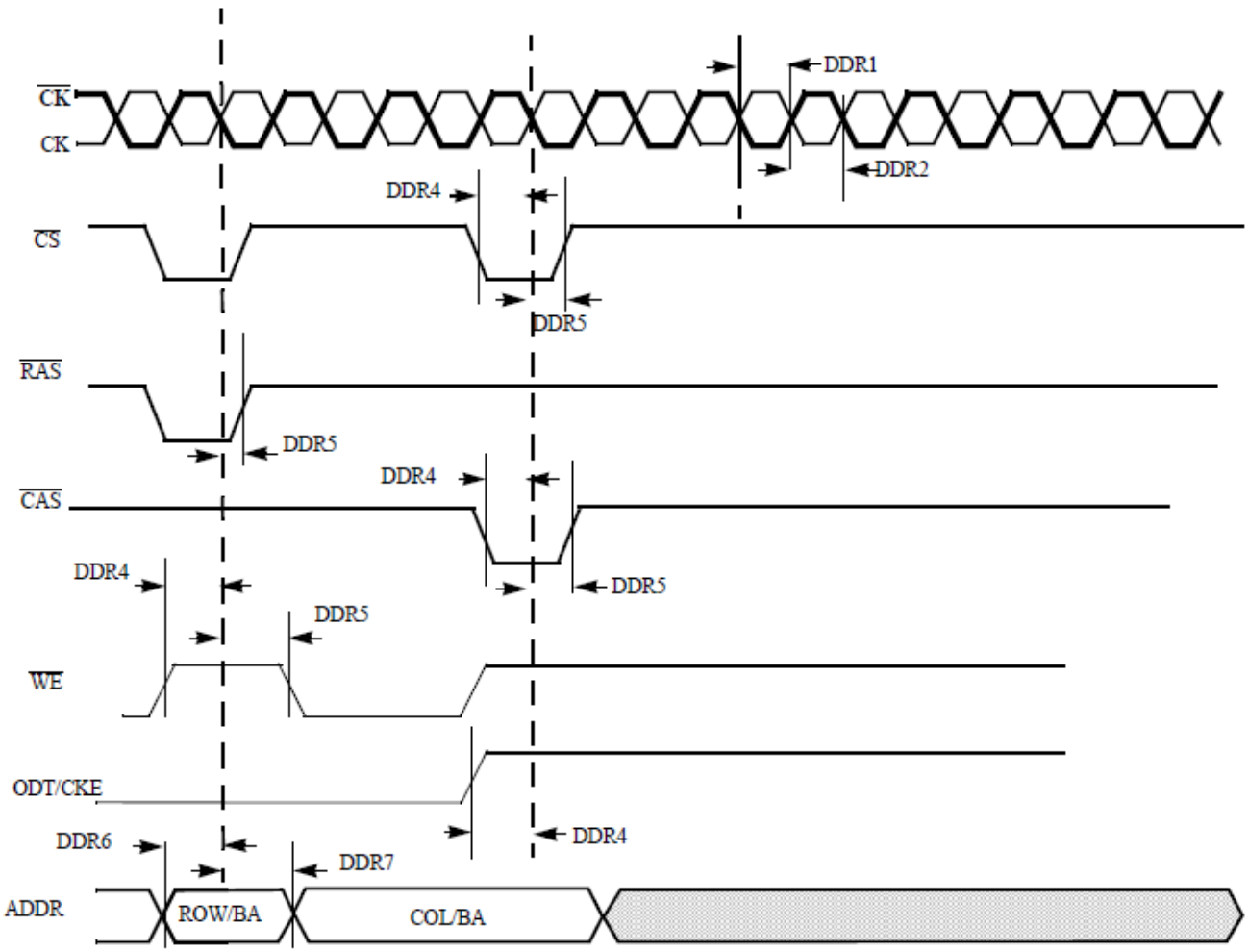

Figure 41. DDR3 Command and Address Timing Parameters

NOTE

RESET pin has a external weak pull DOWN requirement if DDR3 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has a external weak pull UP requirement if DDR3 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 54. DDR3 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tCK
DDR2	CK clock low-level width	tCL	0.47	0.53	tCK
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	440	-	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	315	-	ps
DDR6	Address output setup time	tIS	440	-	ps
DDR7	Address output hold time	tIH	315	-	ps

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.6 Communication interfaces

9.6.1 MediaLB (MLB) DC Characteristics

The section lists the MediaLB 3-pin interface electrical characteristics.

Table 60. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = –6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	$_{IL}$	0 < Vin < VDD	—	±10	µA

1. Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

9.6.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module.

Table 68. OSC32K Main Characteristics (continued)

	Notes	Min	Typ	Max
	oscillator is running. Another 1.5 µA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 µA on vdd_rtc when the ring oscillator is not running.			
Bias resistor	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.		14 MΩ	
Crystal Properties				
Cload	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal		12.5 pF	
ESR	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.		50 kΩ	

9.7.3 Fast internal RC oscillator (24 MHz) electrical characteristics

This section describes a fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 69. Fast internal oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCM}	RC oscillator high frequency	T_A= 25 °C, trimmed	—	24	—	MHz
I_{RCMRUN}	RC oscillator high frequency current in running mode	T_A= 25 °C, trimmed	—	55		µA
I_{RCMPWD}	RC oscillator high frequency current in power down mode	T_A= 25 °C		100		nA
RCMTRIM	RC oscillator precision after trimming of f_{RC}	T_A= 25 °C	-1	—	+1	%
RCMVAR	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration		-5		+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.7.7 PLL5 (Ethernet PLL) Electrical Parameters

Table 73. PLL5 Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Cycle to cycle jitter (p2p)[1]	<400ps @ 50 MHz
Duty Cycle	45%~55%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out IO pad.

9.7.8 PLL4 (Audio PLL) Electrical Parameters

Table 74. PLL4 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)	<42ps @1128MHz
Period jitter(p2p)[1]	<115ps@1128MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad.

9.7.9 PLL6 (Video PLL) Electrical Parameters

Table 75. PLL6 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)[1]	<42ps @ 1128 MHz
Period jitter(p2p)	<130ps @960MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad & at use case frequency.

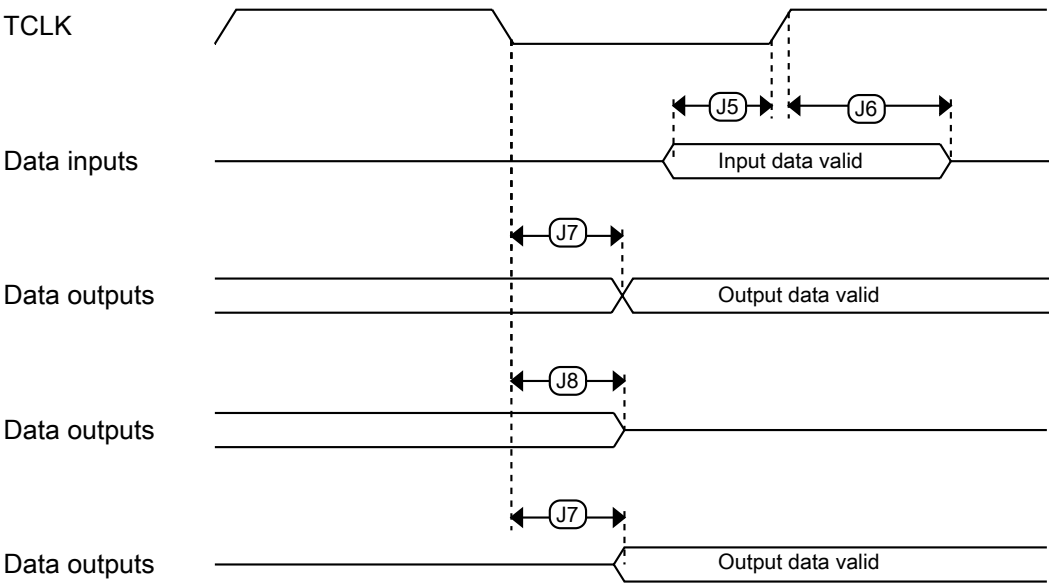

Figure 55. Boundary scan (JTAG) timing

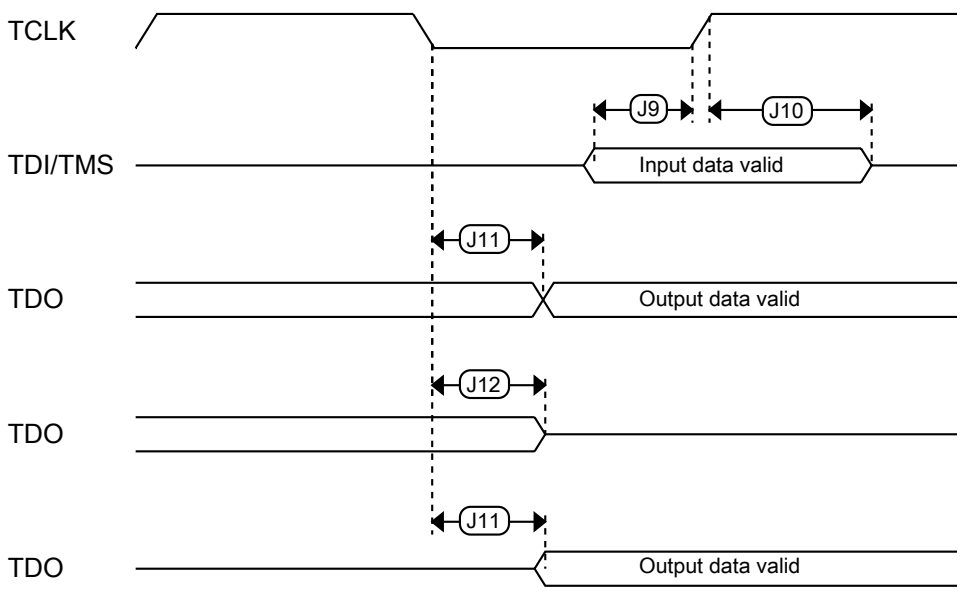

Figure 56. Test Access Port timing

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
T3	27	TEST			TEST							
T1	23	Ext_POR			TEST2							
V12	69	DECAP_ V11_LDO_ OUT			DECAP_ V11_LDO_ OUT							
T11	65	DECAP_ V25_LDO_ OUT			DECAP_ V25_LDO_ OUT							
T2	26	BCTRL			BCTRL							
P5	24	VDDREG			VDDREG							
T12	68	VDD33_ LDOIN			VDD33_ LDOIN							
V11	67	VSS			VSS							
U11	66	VSS_KEL0			VSS_KEL0							
W14	—	LVDS0P			LVDS0P							
Y14	—	LVDS0N			LVDS0N							
K4	3	JTCLK/ SWCLK	JTCLK/ SWCLK	PTA8	JTCLK/ SWCLK			DCU0_R0			MLBCLK	
K2	4	JTDI	JTDI	PTA9	JTDI	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK	DCU0_R1		WDOG_b		
K1	5	JTDO	JTDO/ TRACESWO	PTA10	JTDO	EXT_AUDIO_ MCLK		DCU0_G0		ENET_TS_ CLKIN	MLBSIGNAL	
L1	6	JTMS/ SWDIO	JTMS/ SWDIO	PTA11	JTMS/ SWDIO			DCU0_G1			MLBDATA	
L3	7	PTA12		PTA12	TRACECK	EXT_AUDIO_ MCLK				VIU_DATA13	I2C0_SCL	
Y5	43	PTA16		PTA16	TRACED0	USB0_ VBUS_EN	ADC1_SE0	LCD29	SAI2_TX_ BCLK	VIU_DATA14	I2C0_SDA	
Y6	44	PTA17		PTA17	TRACED1	USB0_ VBUS_OC	ADC1_SE1	LCD30	USB0_SOF_ PULSE	VIU_DATA15	I2C1_SCL	
V6	46	PTA18		PTA18	TRACED2	ADC0_SE0	FTM1_QD_ PHA	LCD31	SAI2_TX_ DATA	VIU_DATA16	I2C1_SDA	
U6	47	PTA19		PTA19	TRACED3	ADC0_SE1	FTM1_QD_ PHB	LCD32	SAI2_TX_ SYNC	VIU_DATA17	QSPI1_A_ SCK	
B18	143	PTA20		PTA20	TRACED4			LCD33		SCI3_TX	DCU1_ HSYNC/ DCU1_ TCON1	
D18	145	PTA21		PTA21/ MII0_RXCLK	TRACED5				SAI2_RX_ BCLK	SCI3_RX	DCU1_ VSYNC/ DCU1_ TCON2	
E17	147	PTA22		PTA22	TRACED6				SAI2_RX_ DATA	I2C2_SCL	DCU1_TAG/ DCU1_ TCON0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G20	124	PTD23		PTD23/ MII0_ RXDATA[3]	FB_AD23	NF_IO7	FTM2CH0	ENET0_ 1588_TMR0	SDHC0_ DAT4	SCI2_TX	DCU1_R3	
F20	126	PTD22		PTD22/ MII0_ RXDATA[2]	FB_AD22	NF_IO6	FTM2CH1	ENET0_ 1588_TMR1	SDHC0_ DAT5	SCI2_RX	DCU1_R4	
F19	128	PTD21		PTD21/ MII0_CRS	FB_AD21	NF_IO5		ENET0_ 1588_TMR2	SDHC0_ DAT6	SCI2_RTS	DCU1_R5	
F17	129	PTD20		PTD20/ MII0_COL	FB_AD20	NF_IO4		ENET0_ 1588_TMR3	SDHC0_ DAT7	SCI2_CTS	DCU1_R0	
F16	130	PTD19		PTD19	FB_AD19	NF_IO3	ESAI_SCKR	I2C0_SCL	FTM2_QD_ PHA	MII0_ TXDATA[3]	DCU1_R1	
E18	131	PTD18		PTD18	FB_AD18	NF_IO2	ESAI_FSR	I2C0_SDA	FTM2_QD_ PHB	MII0_ TXDATA[2]	DCU1_G0	
E20	132	PTD17		PTD17	FB_AD17	NF_IO1	ESAI_HCKR	I2C1_SCL		MII0_TXERR	DCU1_G1	
D20	133	PTD16		PTD16	FB_AD16	NF_IO0	ESAI_HCKT	I2C1_SDA			DCU1_G2	
Y17	86	PTD0		PTD0	QSPI0_A_ SCK	SCI2_TX		FB_AD15	SPDIF_ EXTCLK			
Y18	87	PTD1		PTD1	QSPI0_A_ CS0	SCI2_RX		FB_AD14	SPDIF_IN1			
V18	88	PTD2		PTD2	QSPI0_A_ DATA3	SCI2_RTS	SPI1_PCS3	FB_AD13	SPDIF_OUT1			
Y19	89	PTD3		PTD3	QSPI0_A_ DATA2	SCI2_CTS	SPI1_PCS2	FB_AD12	SPDIF_ PLOCK			
W19	90	PTD4		PTD4	QSPI0_A_ DATA1		SPI1_PCS1	FB_AD11	SPDIF_ SRCLK			
W20	91	PTD5		PTD5	QSPI0_A_ DATA0		SPI1_PCS0	FB_AD10				
V20	92	PTD6		PTD6	QSPI0_A_ DQS		SPI1_SIN	FB_AD9				
V19	93	PTD7		PTD7	QSPI0_B_ SCK		SPI1_SOUT	FB_AD8				
U17	94	PTD8		PTD8	QSPI0_B_ CS0	FB_CLKOUT	SPI1_SCK	FB_AD7				
U18	97	PTD9		PTD9	QSPI0_B_ DATA3	SPI3_PCS1		FB_AD6		SAI1_TX_ SYNC	DCU1_B0	
U20	98	PTD10		PTD10	QSPI0_B_ DATA2	SPI3_PCS0		FB_AD5			DCU1_B1	
T20	99	PTD11		PTD11	QSPI0_B_ DATA1	SPI3_SIN		FB_AD4				
T19	100	PTD12		PTD12	QSPI0_B_ DATA0	SPI3_SOUT		FB_AD3				
T18	101	PTD13		PTD13	QSPI0_B_ DQS	SPI3_SCK		FB_AD2				
A19	141	PTB23		PTB23	SAI0_TX_ BCLK	SCI1_TX		FB_MUXED_ ALE	FB_TS_b	SCI3_RTS	DCU1_G3	

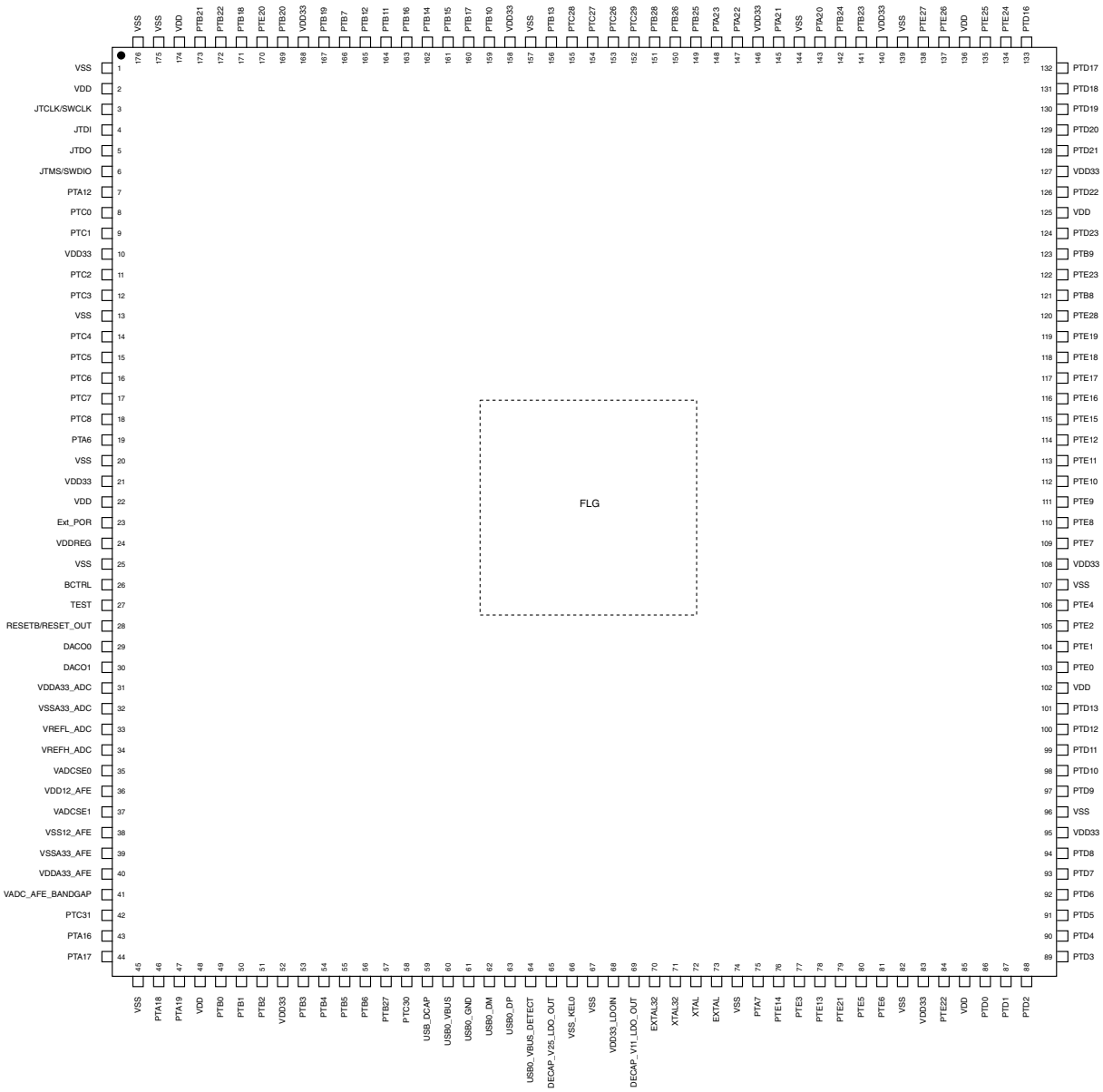

Figure 59. 176 LQFP Pinout Diagram

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[1]	PORT0[1]	PTA8	IOMUXC_PTA8	40048004
RGPIO[2]	PORT0[2]	PTA9	IOMUXC_PTA9	40048008
RGPIO[3]	PORT0[3]	PTA10	IOMUXC_PTA10	4004800C
RGPIO[4]	PORT0[4]	PTA11	IOMUXC_PTA11	40048010
RGPIO[5]	PORT0[5]	PTA12	IOMUXC_PTA12	40048014
RGPIO[6]	PORT0[6]	PTA16	IOMUXC_PTA16	40048018
RGPIO[7]	PORT0[7]	PTA17	IOMUXC_PTA17	4004801C
RGPIO[8]	PORT0[8]	PTA18	IOMUXC_PTA18	40048020
RGPIO[9]	PORT0[9]	PTA19	IOMUXC_PTA19	40048024
RGPIO[10]	PORT0[10]	PTA20	IOMUXC_PTA20	40048028
RGPIO[11]	PORT0[11]	PTA21	IOMUXC_PTA21	4004802C
RGPIO[12]	PORT0[12]	PTA22	IOMUXC_PTA22	40048030
RGPIO[13]	PORT0[13]	PTA23	IOMUXC_PTA23	40048034
RGPIO[14]	PORT0[14]	PTA24	IOMUXC_PTA24	40048038
RGPIO[15]	PORT0[15]	PTA25	IOMUXC_PTA25	4004803C
RGPIO[16]	PORT0[16]	PTA26	IOMUXC_PTA26	40048040
RGPIO[17]	PORT0[17]	PTA27	IOMUXC_PTA27	40048044
RGPIO[18]	PORT0[18]	PTA28	IOMUXC_PTA28	40048048
RGPIO[19]	PORT0[19]	PTA29	IOMUXC_PTA29	4004804C
RGPIO[20]	PORT0[20]	PTA30	IOMUXC_PTA30	40048050
RGPIO[21]	PORT0[21]	PTA31	IOMUXC_PTA31	40048054
RGPIO[22]	PORT0[22]	PTB0	IOMUXC_PTB0	40048058
RGPIO[23]	PORT0[23]	PTB1	IOMUXC_PTB1	4004805C
RGPIO[24]	PORT0[24]	PTB2	IOMUXC_PTB2	40048060
RGPIO[25]	PORT0[25]	PTB3	IOMUXC_PTB3	40048064
RGPIO[26]	PORT0[26]	PTB4	IOMUXC_PTB4	40048068
RGPIO[27]	PORT0[27]	PTB5	IOMUXC_PTB5	4004806C
RGPIO[28]	PORT0[28]	PTB6	IOMUXC_PTB6	40048070
RGPIO[29]	PORT0[29]	PTB7	IOMUXC_PTB7	40048074
RGPIO[30]	PORT0[30]	PTB8	IOMUXC_PTB8	40048078
RGPIO[31]	PORT0[31]	PTB9	IOMUXC_PTB9	4004807C
RGPIO[32]	PORT1[0]	PTB10	IOMUXC_PTB10	40048080
RGPIO[33]	PORT1[1]	PTB11	IOMUXC_PTB11	40048084
RGPIO[34]	PORT1[2]	PTB12	IOMUXC_PTB12	40048088
RGPIO[35]	PORT1[3]	PTB13	IOMUXC_PTB13	4004808C
RGPIO[36]	PORT1[4]	PTB14	IOMUXC_PTB14	40048090
RGPIO[37]	PORT1[5]	PTB15	IOMUXC_PTB15	40048094
RGPIO[38]	PORT1[6]	PTB16	IOMUXC_PTB16	40048098
RGPIO[39]	PORT1[7]	PTB17	IOMUXC_PTB17	4004809C

Table continues on the next page...

Table 79. Special Signal Considerations (continued)

Special Signal	Comments
JTCLK, JTDI, JTDO, JTMS	For JTAG the use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is matched. For example, do not use an external pull down on an input that has on-chip pull-up. JTDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTDO is detrimental and should be avoided.
LVDS0N, LVDS0P	Not recommended for application use, intended for clock observation purposes during debug only.
RESETB/RESET_OUT	Active low input used to generate a system wide reset (except the SRTC). A glitch filter is include to help prevent unexpected resets, a minimum pulse width of 125 nsecs is required to guarantee a reset is detected.
XTAL, EXTAL	A 24.0 MHz fundamental mode crystal should be connected between XTAL and EXTAL. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTAL must be directly driven by the external oscillator and EXTAL floated. The XTAL signal level must swing from ~0.8 x DECAP_V11_ LDO_OUT to ~0.2 V.
XTAL32, EXTAL32	If the user wishes to configure XTAL32 and EXTAL32 as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between XTAL32 and EXTAL32. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTAL32 and EXTAL32 to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTAL32 and EXTAL32 should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTAL32 the EXTAL32 pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed DECAP_V11_ LDO_OUT level and the frequency should be <100 kHz under typical conditions. In the case where the SIRC is used, it is recommended to connect XTAL32 to ground and leave EXTAL32 floating.

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
TEST	T3	27	VDD33	GPIO	—	TEST	—	—
USB0_DM	T9	62	USB_DCAP	Analog	—	USB0_DM	—	—
USB0_DP	T10	63	USB_DCAP	Analog	—	USB0_DP	—	—
USB0_VBUS	W11	60	USB_DCAP	Analog	—	USB0_VBUS	—	—
USB0_VBUS_ DETECT	Y11	64	USB_DCAP	Analog	—	USB0_VBUS_ DETECT	—	—
USB1_DM	V9	—	USB_DCAP	Analog	—	USB1_DM	—	—
USB1_DP	W9	—	USB_DCAP	Analog	—	USB1_DP	—	—
USB1_VBUS	W10	—	USB_DCAP	Analog	—	USB1_VBUS	—	—
USB1_VBUS_ DETECT	U9	—	USB_DCAP	Analog	—	USB1_VBUS_ DETECT	—	—
VADCSE0	Y4	35	VDDA33_ADC / VDD12_AFE / VADC_AFE_BANDGAP ?	Analog	—	VADCSE0	—	—
VADCSE1	U4	37	VDDA33_ADC / VDD12_AFE / VADC_AFE_BANDGAP ?	Analog	—	VADCSE1	—	—
VADCSE2	W4	—	VDDA33_ADC / VDD12_AFE / VADC_AFE_BANDGAP ?	Analog	—	VADCSE2	—	—
VADCSE3	V5	—	VDDA33_ADC / VDD12_AFE / VADC_AFE_BANDGAP ?	Analog	—	VADCSE3	—	—
XTAL	W13	72	DECAP_V11_ LDO_OUT	Analog	—	XTAL	—	—
XTAL32	W12	71	DECAP_V11_ LDO_OUT	Analog	—	XTAL32	—	—

Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		Updated Power sequencing Updated Power supply figure Updated Recommended operating conditions table Removed Reset specifications Updated 12-bit DAC operating requirements Added a note in 12-bit ADC operating conditions section Updated VideoADC Specifications table Updated LCD driver specifications table QuadSPI timing- Replaced VDDE with VDD33 Added notes in DDR3 Timing Parameters and LPDD2 Timing Parameters sections. Updated 24MHz external oscillator electrical characteristics table Updated OSC32K Main Characteristics table Updated Freescale Document Number for 144-pin LQFP Changed pin-name from EXT_POR to TEST2, VBAT to VBB Updated Pinouts section Updated GPIO Mapping
Rev4	08/2012	Updated Part identification Editorial changes in USB PHY Current Consumption in Normal Mode, GPIO AC Electrical Characteristics (3.3V power mode) Updated Power sequencing table Updated Power supply diagram Updated AC electrical specification of following modules: DCU, 12-bit DAC, Ethernet, Enhanced Serial Audio Interface (ESAI), SAI/I2S, Flexbus, MLB, DSPI, 24MHz External Oscillator, JTAG, Debug, ESAI, QSPI Updated Thermal Attributes for 364 MAPBGA Updated Freescale document number for 176-pin LQFP and 364 MAPBGA Updated VREG specifications

Table continues on the next page...