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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	DDR3, DRAM, LPDDR2
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf312r3k2cku2

Field	Description	Values
M	Memory option	• 3 = Standard (1.5MB SRAM) • 2 = Optional (1MB SRAM and 512K L2 Cache)
T	Temperature spec	• C = -40 ^{0}C to +85 ^{0}C T_a
P	Package	• KU = 176LQFP • MK = 364BGA
S	Speed (A5 core)	• 2 = 266MHz • 4 = 400MHz

2.4 Part Numbers

This table lists the part numbers on the device.

Part Number	Package	Description
SVF311R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, 176LQFP-EP
SVF312R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, OpenVG GPU, 176LQFP-EP
SVF321R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, M4, 176LQFP-EP
SVF322R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, M4, OpenVG GPU, 176LQFP-EP
SVF331R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, 176LQFP-EP
SVF332R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, OpenVG GPU, 176LQFP-EP
SVF511R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, 364BGA
SVF512R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, OpenVG GPU, 364BGA
SVF521R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4, 364BGA
SVF522R2K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4, L2 Cache, OpenVG GPU, 364BGA
SVF522R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4, OpenVG GPU, 364BGA
SVF531R3K1CMK4	MAP 364 17*171.5 P0.8	A5-400, M4 Primary, 364BGA
SVF532R2K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, L2 Cache OpenVG GPU, 364BGA
SVF532R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, OpenVG GPU, 364BGA

4 Handling ratings

4.1 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I_{LAT}	Latch-up Current at ambient temperature of 85 °C	-100	100	mA	

1. Determined according to the AEC spec AEC-Q100-002 for HBM
2. Determined according to AEC spec AEC-Q100-011

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5 Operating Requirements

5.1 Thermal operating requirements

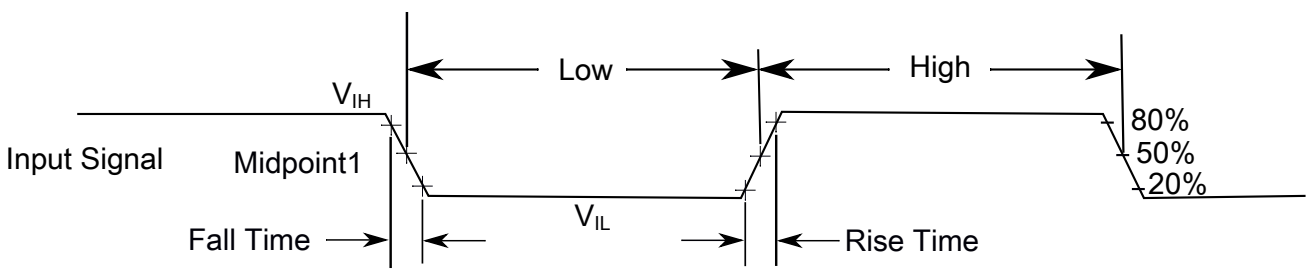
Table 1. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature	–40	85	°C
T_J	Junction temperature		105	°C

6 General

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

Table 22. Output Buffer Average Impedance (3.3V power mode) (continued)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
		1 0 0	30	37	58	
		1 0 1	24	30	46	
		1 1 0 Extra drive strength	20	25	38	
		1 1 1	17	20	32	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.2 DDR parameters

Table 23. DDR operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi	Core internal supply voltage	1.16	1.23	1.26	V
ovdd	I/O output supply voltage (DDR3 mode)	1.425	1.5	1.575	V
ovdd	I/O output supply voltage (LPDDR2 mode)	1.14	1.2	1.26	V
vdd2p5	I/O PD predriver and level shifters supply voltage	2.25	2.5	2.75	V

Table 24. LPDDR2 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.9*ovdd			V	Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.
Vol	Low-level output voltage				0.1*ovdd	V	
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	
Vih(dc)	DC input high voltage		Vref+0.13		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.13	V	
Vih(diff)	DC differential input logic high		0.26		Note[1]	V	
Vil(diff)	DC differential input logic low		Note		-0.26	V	

Table continues on the next page...

NOTE

WBREG is the Well Bias Regulator. Supplies PD1 WELL during well bias modes.

8.3 Absolute maximum ratings

NOTE

These are the values above which device can get damaged. Refer to the recommended operating conditions table for intended use case values

Table 29. Absolute maximum ratings

Symbol	Parameters	Min	Max	Unit
USB0_VBUS	VBUS supply for USB	-	5.25	V
USB1_VBUS	VBUS supply for USB	-	5.25	V
USB_DCAP	USB LDO 5V->3.3V Outpu	-0.3	3.6	V
VBAT	Battery supply in case of LDOIN fails	-0.3	3.6	V
VDD33_LDOIN	LDO input supply	-0.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	-0.3	1.3	V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR, EFUSE	-0.3	3.6	V
VDD33	GPIO 3.3V IO supply	-0.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	-0.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	-0.3	3.6	V
VREFH_ADC	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)	-0.3	1.3	V
FA_VDD	Test purpose only	-0.3	1.3	V
VDD	1.2V core supply	-0.3	1.3	V
SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	-0.3	1.975	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	-0.3	3.6	V

Table 31. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	-	-	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	-	40	MHz	-
	ADLPC=0, ADHSC=0 12 bit mode		4	-	30	MHz	-
	ADLPC=1, ADHSC=0 12 bit mode		4	-	20	MHz	-

1. Typical values assume VDDAD = 3.3 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference

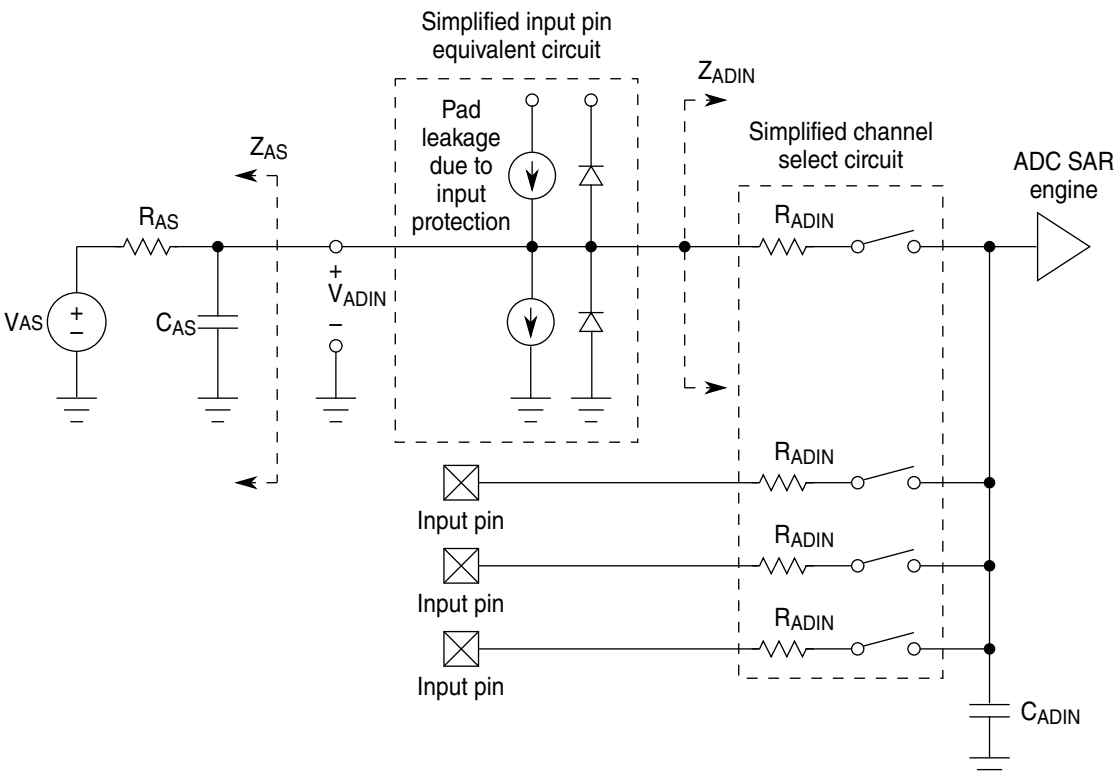


Figure 5. 12-bit ADC Input Impedance Equivalency Diagram

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions	Symb	Min	Typ	Max	Unit	Comment
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
Total Unadjusted Error	12 bit mode	TUE	-2	-	+5	LSB	With Max Averaging
	10 bit mode		-0.5	-	+2		
	8 bit mode		-0.25	-	+1.5		
Differential Non-Linearity	12 bit mode	DNL	-	±0.6	±1.5	LSB[1]	Waiting for histogram method confirmation
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.5		
Integral Non-Linearity	12 bit mode	INL	-	±2	±4	LSB[1]	Waiting for histogram method confirmation
	10bit mode		-	±1	±2		
	8 bit mode		-	±0.5	±1		
Zero-Scale Error	12 bit mode	E_{ZS}	-	+1.0	±1.6	LSB[1]	VADIN = V_{REFL} With Max Averaging
	10bit mode		-	±0.4	±0.8		
	8 bit mode		-	±0.1	±0.4		
Full-Scale Error	12 bit mode	E_{FS}	-	±2	±3.5	LSB[1]	VADIN = V_{REFH} With Max Averaging
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.75		
Quantization Error	12 bit mode	E_Q	-	±1 to 0		LSB[1]	
	10bit mode		-	±0.5			
	8 bit mode		-	±0.5			
Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	-	Bits	Fin = 100Hz
Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	
Input Leakage Error	all modes	EIL	I_{In} x RAS			mV	I_{In} = 400 nA leakage current
Temp Sensor Slope	Across the full temperature range of the device	m	--	1.84	--	mV/°C	
Temp Sensor Voltage	25°C	V_{TEMP25}	-	696	-	mV	

1. 1 LSB = (V_{REFH} - V_{REFL})/2N

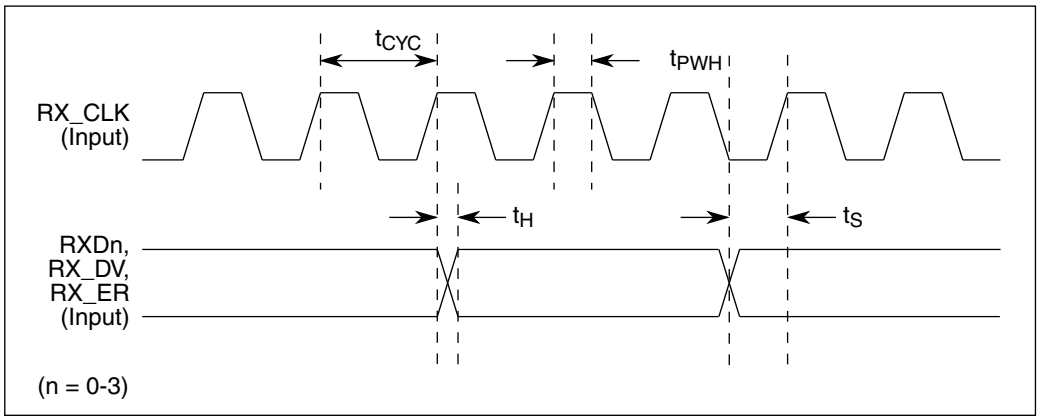


Figure 21. MII receive signal timing diagram

Table 41. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_S	5			ns
Input setup time after RX_CLK	t_H	5			ns

9.3.3 Receive and Transmit signal timing specifications for MII interfaces

This section provides timing specs that meet the requirements for MII interfaces for a range of transceiver devices.

9.4 Audio interfaces

9.4.1 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The following table shows the interface timing values.

Table 44. Enhanced Serial Audio Interface (ESAI) Timing

No	Characteristics	Symbol	Min	Max	Condition[1]	Unit
1	Clock cycle[2]	t_{SSICC}	30.0 $(4 \times T_c)$	— —	master	ns
2	Clock high period: • master • slave	— —	6 $(2 \times T_c - 9.0)$ 15 $(2 \times T_c)$	— —	— —	ns
3	Clock low period: • master • slave	— —	6 $(2 \times T_c - 9.0)$ 15 $(2 \times T_c)$	— —	— —	ns
4	FSR Input and Data Input setup time before SCKR (SCK in synchronous mode) falling edge	— —	6 15	— —	Slave Master	ns
5	FSR Input and Data Input hold time after SCKR falling edge	— —	2 0	— —	Slave Master	ns
6	SCKT rising edge to FST out and Data out valid	— —	— —	15 6	Slave Master	ns
7	SCKT rising edge to FST out and Data out hold	— —	— —	0 0	Slave Master	ns
8	FST input setup time before SCKT falling edge	— —	6 15	— —	Slave Master	ns
9	FST input hold time after SCKT falling edge	— —	2 0	— —	Slave Master	ns
10	HCKR/HCKT clock cycle	—	15 $(2 \times T_C)$	—	—	ns
11	HCKT input rising edge to SCKT output	—	—	18.0	—	ns
12	HCKR input rising edge to SCKR output	—	—	18.0	—	ns

1. SCKT(SCKT pin) = transmit clock SCKR(SCKR pin) = receive clock FST(FST pin) = transmit frame sync FSR(FSR pin) = receive frame sync HCKT(HCKT pin) = transmit high frequency clock HCKR(HCKR pin) = receive high frequency clock
2. For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

Table 52. NFC specifications

Num	Description	Min.	Max.	Unit
t_{CLS}	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
t_{CLH}	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
t_{CS}	$\overline{\text{NFC\_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
t_{CH}	$\overline{\text{NFC\_CEn}}$ hold time	$T_H + T_L$	—	ns
t_{WP}	$\overline{\text{NFC\_WP}}$ pulse width	$T_L - 1$	—	ns
t_{ALS}	NFC_ALE setup time	$2T_H + T_L$	—	ns
t_{ALH}	NFC_ALE hold time	$T_H + T_L$	—	ns
t_{DS}	Data setup time	$T_L - 1$	—	ns
t_{DH}	Data hold time	$T_H - 1$	—	ns
t_{WC}	Write cycle time	$T_H + T_L - 1$	—	ns
t_{WH}	$\overline{\text{NFC\_WE}}$ hold time	$T_H - 1$	—	ns
t_{RR}	Ready to $\overline{\text{NFC\_RE}}$ low	$4T_H + 3T_L + 90$	—	ns
t_{RP}	$\overline{\text{NFC\_RE}}$ pulse width	$T_L + 1$	—	ns
t_{RC}	Read cycle time	$T_L + T_H - 1$	—	ns
t_{REH}	$\overline{\text{NFC\_RE}}$ high hold time	$T_H - 1$	—	ns
t_{IS}	Data input setup time	11	—	ns

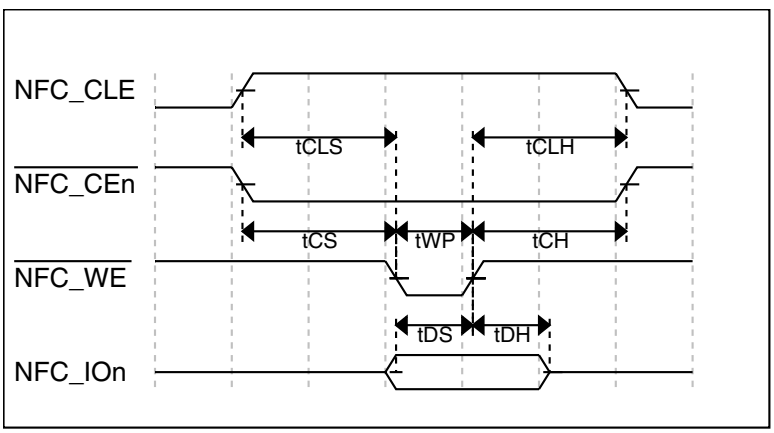


Figure 34. Command latch cycle timing

9.5.4 DDR controller specifications

9.5.4.1 DDR3 Timing Parameters

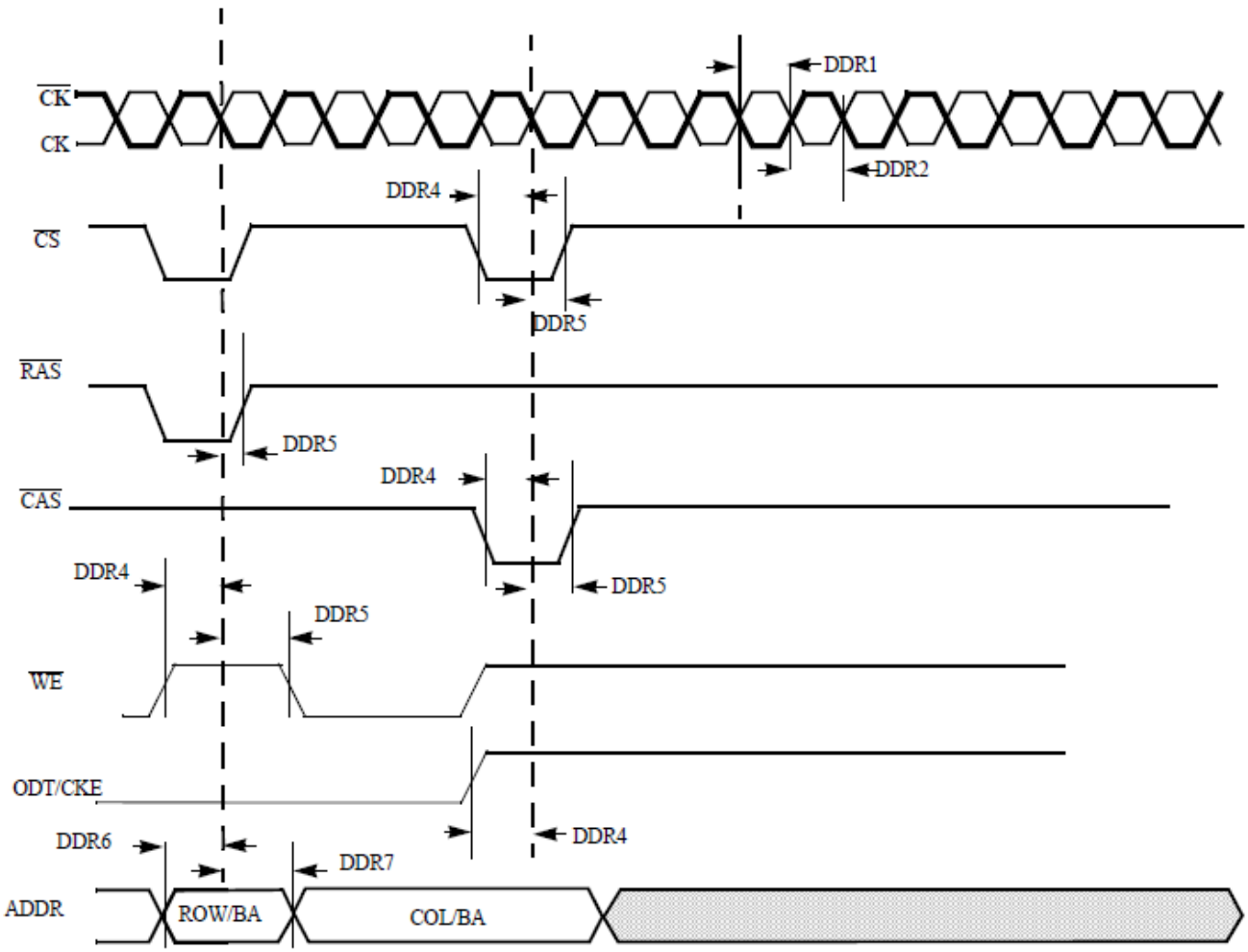


Figure 41. DDR3 Command and Address Timing Parameters

NOTE

RESET pin has a external weak pull DOWN requirement if DDR3 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

9.5.4.3 DDR3 Write cycle

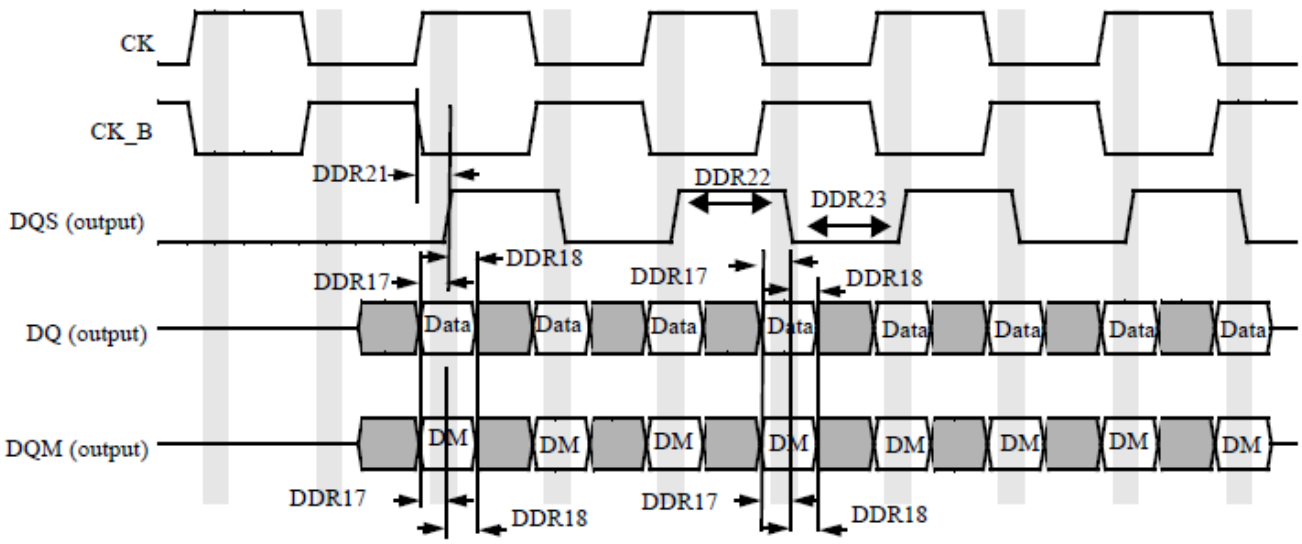


Figure 43. DDR3 Write cycle

Table 56. DDR3 Write cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	240	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	215	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR22	DQS low level width	tDQSL	0.45	0.55	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

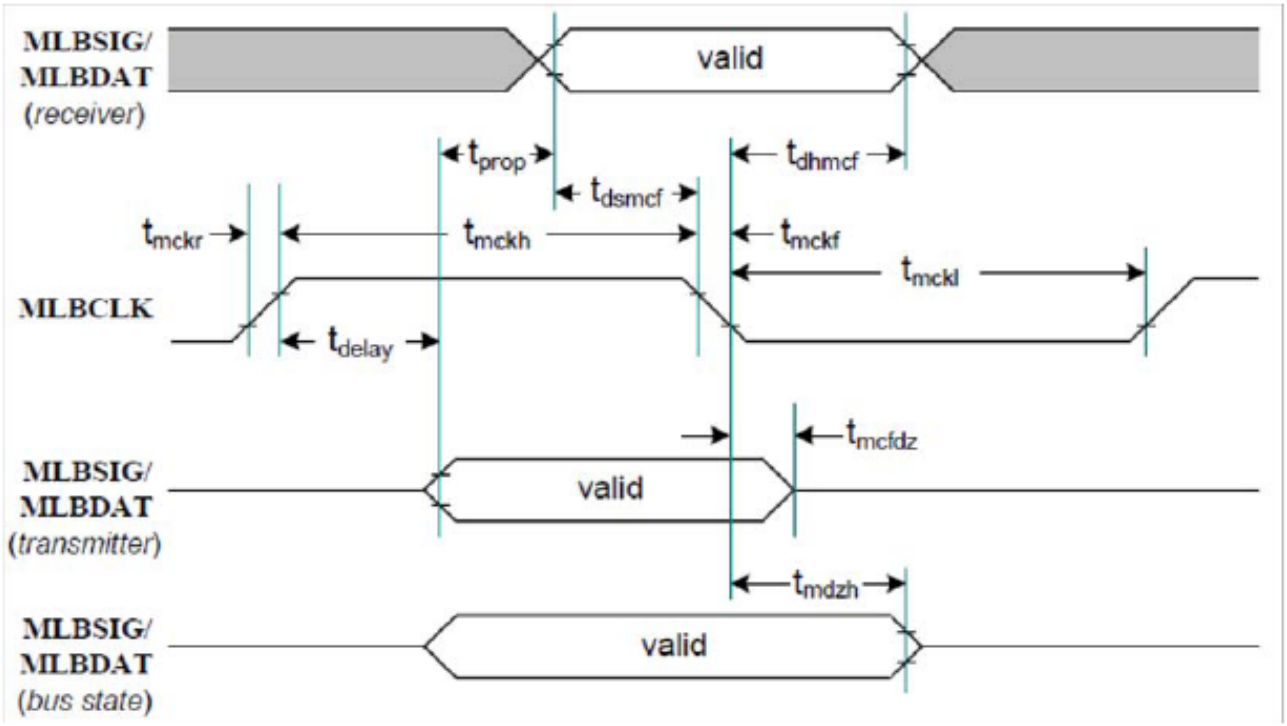


Figure 47. MediaLB 3-PinTiming

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 61. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
MLBCLK rise time	$t_{mck}r$	Refer Table 21		ns	$V_{IL\ to\ V_{IH}}$
MLBCLK fall time	$t_{mck}f$			ns	$V_{IH\ to\ V_{IL}}$
MLBCLK low time[1]	$t_{mck}l$	30, 14	—	ns	256xFs, 512xFs
MLBCLK high time	$t_{mck}h$	30, 14	—	ns	256xFs, 512xFs
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	3	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	2	—	ns	—
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	16	ns	2
Bus output hold from MLBCLK low	t_{mdzh}	2	—	ns	—

1. MLBCLK low/high time includes the pluse width variation.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
T3	27	TEST			TEST							
T1	23	Ext_POR			TEST2							
V12	69	DECAP_ V11_LDO_ OUT			DECAP_ V11_LDO_ OUT							
T11	65	DECAP_ V25_LDO_ OUT			DECAP_ V25_LDO_ OUT							
T2	26	BCTRL			BCTRL							
P5	24	VDDREG			VDDREG							
T12	68	VDD33_ LDOIN			VDD33_ LDOIN							
V11	67	VSS			VSS							
U11	66	VSS_KEL0			VSS_KEL0							
W14	—	LVDS0P			LVDS0P							
Y14	—	LVDS0N			LVDS0N							
K4	3	JTCLK/ SWCLK	JTCLK/ SWCLK	PTA8	JTCLK/ SWCLK			DCU0_R0			MLBCLK	
K2	4	JTDI	JTDI	PTA9	JTDI	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK	DCU0_R1		WDOG_b		
K1	5	JTDO	JTDO/ TRACESWO	PTA10	JTDO	EXT_AUDIO_ MCLK		DCU0_G0		ENET_TS_ CLKIN	MLBSIGNAL	
L1	6	JTMS/ SWDIO	JTMS/ SWDIO	PTA11	JTMS/ SWDIO			DCU0_G1			MLBDATA	
L3	7	PTA12		PTA12	TRACECK	EXT_AUDIO_ MCLK				VIU_DATA13	I2C0_SCL	
Y5	43	PTA16		PTA16	TRACED0	USB0_ VBUS_EN	ADC1_SE0	LCD29	SAI2_TX_ BCLK	VIU_DATA14	I2C0_SDA	
Y6	44	PTA17		PTA17	TRACED1	USB0_ VBUS_OC	ADC1_SE1	LCD30	USB0_SOF_ PULSE	VIU_DATA15	I2C1_SCL	
V6	46	PTA18		PTA18	TRACED2	ADC0_SE0	FTM1_QD_ PHA	LCD31	SAI2_TX_ DATA	VIU_DATA16	I2C1_SDA	
U6	47	PTA19		PTA19	TRACED3	ADC0_SE1	FTM1_QD_ PHB	LCD32	SAI2_TX_ SYNC	VIU_DATA17	QSPI1_A_ SCK	
B18	143	PTA20		PTA20	TRACED4			LCD33		SCI3_TX	DCU1_ HSYNC/ DCU1_ TCON1	
D18	145	PTA21		PTA21/ MII0_RXCLK	TRACED5				SAI2_RX_ BCLK	SCI3_RX	DCU1_ VSYNC/ DCU1_ TCON2	
E17	147	PTA22		PTA22	TRACED6				SAI2_RX_ DATA	I2C2_SCL	DCU1_TAG/ DCU1_ TCON0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_SYNC	I2C2_SDA	DCU1_DE/DCU1_TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_VBUS_EN			SDHC1_CLK	DCU1_TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_VBUS_OC			SDHC1_CMD	DCU1_TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_BCLK			SDHC1_DAT0	DCU1_TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_BCLK			SDHC1_DAT1	DCU1_TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_DATA	ENET1_1588_TMR0	SCI4_TX	SDHC1_DAT2	DCU1_TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_DATA	ENET1_1588_TMR1	SCI4_RX	SDHC1_DAT3	DCU1_TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_SYNC	ENET1_1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_SYNC	ENET1_1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_BCLK	VIU_DATA18	QSPI1_A_CS0	
T7	50	PTB1	RCON30	PTB1	FTM0_CH1	ADC0_SE3	RCON30	LCD35	SAI2_RX_DATA	VIU_DATA19	QSPI1_A_DATA3	
V7	51	PTB2	RCON31	PTB2	FTM0_CH2	ADC1_SE2	RCON31	LCD36	SAI2_RX_SYNC	VIU_DATA20	QSPI1_A_DATA2	
W7	53	PTB3		PTB3	FTM0_CH3	ADC1_SE3	EXTRIG	LCD37		VIU_DATA21	QSPI1_A_DATA1	
Y7	54	PTB4		PTB4	FTM0_CH4	SCI1_TX	ADC0_SE4	LCD38	VIU_FID	VIU_DATA22	QSPI1_A_DATA0	
Y8	55	PTB5		PTB5	FTM0_CH5	SCI1_RX	ADC1_SE4	LCD39	VIU_DE	VIU_DATA23	QSPI1_A_DQS	
W8	56	PTB6		PTB6	FTM0_CH6	SCI1_RTS	QSPI0_A_CS1	LCD40	FB_CLKOUT	VIU_HSYNC	SCI2_TX	
D13	166	PTB7		PTB7	FTM0_CH7	SCI1_CTS	QSPI0_B_CS1	LCD41		VIU_VSYNC	SCI2_RX	
J16	121	PTB8		PTB8	FTM1CH0		FTM1_QD_PHA		VIU_DE		DCU1_R6	
J19	123	PTB9		PTB9	FTM1CH1		FTM1_QD_PHB				DCU1_R7	
B15	159	PTB10		PTB10	SCI0_TX			DCU0_TCON4	VIU_DE	CKO1	ENET_TS_CLKIN	
D14	164	PTB11		PTB11	SCI0_RX			DCU0_TCON5	SNVS_ALARM_OUT_B	CKO2	ENET0_1588_TMR0	
E13	165	PTB12	NMI	PTB12	SCI0_RTS		SPI0_PCS5	DCU0_TCON6	FB_AD1	NMI	ENET0_1588_TMR1	
D15	156	PTB13		PTB13	SCI0_CTS		SPI0_PCS4	DCU0_TCON7	FB_AD0	TRACECTL		

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
W15	76	PTE14		PTE14	DCU0_G1			LCD14				
L18	115	PTE15	RCON6	PTE15	DCU0_G2		RCON6	LCD15				
L20	116	PTE16	RCON7	PTE16	DCU0_G3		RCON7	LCD16				
K20	117	PTE17	RCON8	PTE17	DCU0_G4		RCON8	LCD17				
K19	118	PTE18	RCON9	PTE18	DCU0_G5		RCON9	LCD18				
K18	119	PTE19	RCON10	PTE19	DCU0_G6		RCON10	LCD19	I2C0_SCL			
A12	170	PTE20	RCON11	PTE20	DCU0_G7		RCON11	LCD20	I2C0_SDA		EWM_in	
V16	79	PTE21		PTE21	DCU0_B0			LCD21				
W17	84	PTE22		PTE22	DCU0_B1			LCD22				
J17	122	PTE23	RCON12	PTE23	DCU0_B2		RCON12	LCD23				
D19	134	PTE24	RCON13	PTE24	DCU0_B3		RCON13	LCD24				
C19	135	PTE25	RCON14	PTE25	DCU0_B4		RCON14	LCD25				
C20	137	PTE26	RCON15	PTE26	DCU0_B5		RCON15	LCD26				
B20	138	PTE27	RCON16	PTE27	DCU0_B6		RCON16	LCD27	I2C1_SCL			
K16	120	PTE28	RCON17	PTE28	DCU0_B7		RCON17	LCD28	I2C1_SDA		EWM_out	
V15	75	PTA7		PTA7	VIU_PIX_CLK							
T14	—	EXT_TAMPER0			EXT_TAMPER0							
U14	—	EXT_TAMPER1			EXT_TAMPER1							
T13	—	EXT_TAMPER2/EXT_WM0_TAMPER_IN			EXT_TAMPER2/EXT_WM0_TAMPER_IN							
U13	—	EXT_TAMPER3/EXT_WM0_TAMPER_OUT			EXT_TAMPER3/EXT_WM0_TAMPER_OUT							
U12	—	EXT_TAMPER4/EXT_WM1_TAMPER_IN			EXT_TAMPER4/EXT_WM1_TAMPER_IN							
U10	—	EXT_TAMPER5/EXT_WM1_TAMPER_OUT			EXT_TAMPER5/EXT_WM1_TAMPER_OUT							
G7	2	VDD			VDD							
J7	22	VDD			VDD							
L7	48	VDD			VDD							
H8	—	VDD			VDD							
K8	85	VDD			VDD							
M8	102	VDD			VDD							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
P8	125	VDD			VDD							
G9	136	VDD			VDD							
N9	174	VDD			VDD							
H10	—	VDD			VDD							
P10	—	VDD			VDD							
G11	—	VDD			VDD							
N11	—	VDD			VDD							
H12	—	VDD			VDD							
P12	—	VDD			VDD							
G13	—	VDD			VDD							
J13	—	VDD			VDD							
L13	—	VDD			VDD							
N13	—	VDD			VDD							
H14	—	VDD			VDD							
K14	—	VDD			VDD							
M14	—	VDD			VDD							
P14	—	VDD			VDD							
A1	1	VSS			VSS							
A20	13	VSS			VSS							
B3	20	VSS			VSS							
B5	25	VSS			VSS							
B8	45	VSS			VSS							
B11	—	VSS			VSS							
B13	—	VSS			VSS							
B16	—	VSS			VSS							
B19	—	VSS			VSS							
C2	—	VSS			VSS							
D17	—	VSS			VSS							
E5	—	VSS			VSS							
E8	—	VSS			VSS							
E11	—	VSS			VSS							
E14	—	VSS			VSS							
E19	—	VSS			VSS							
F2	—	VSS			VSS							
G17	—	VSS			VSS							
H4	—	VSS			VSS							
J2	—	VSS			VSS							
J18	—	VSS			VSS							
M2	—	VSS			VSS							
M4	—	VSS			VSS							

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTB3	W7	53	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB4	Y7	54	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB5	Y8	55	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB6	W8	56	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB7	D13	166	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB8	J16	121	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB9	J19	123	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB10	B15	159	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB11	D14	164	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB12	E13	165	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB13	D15	156	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB14	B14	162	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB15	A14	161	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB16	C14	163	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB17	A15	160	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB18	B12	171	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB19	C13	167	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB20	A13	169	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB21	E12	173	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB22	D12	172	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB23	A19	141	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB24	A18	142	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB25	B17	149	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB26	A17	150	VDD33	GPIO	ALT3	RCON21	Input	Disabled
PTB27	U8	57	VDD33	GPIO	ALT3	RCON22	Input	Disabled
PTB28	A16	151	VDD33	GPIO	ALT3	RCON23	Input	Disabled
PTC0	L4	8	VDD33	GPIO	ALT7	RCON18	Input	Disabled
PTC1	L5	9	VDD33	GPIO	ALT7	RCON19	Input	Disabled
PTC2	M5	11	VDD33	GPIO	ALT7	RCON20	Input	Disabled
PTC3	M3	12	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC4	L2	14	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC5	M1	15	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC6	N1	16	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC7	N2	17	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC8	N4	18	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC9	T15	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC10	U15	—	VDD33	GPIO	ALT0	GPIO	Disabled	

Table continues on the next page...

Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• In the USB PHY Current Consumption table, removed the Normal Mode • In the Power Sequence table, revised the Power UP/ Down Order column for USB0_VBUs and USB1_VBUS • In the Recommended operating conditions table, revised the min value of VBAT. Revised the min value of VREFH_ADC Revised the min and max values of SDRAMC_VDD1P5 • In the Recommended Connections for Unused Analog Interfaces section, added the notes. Revised the Recommendation if Unused column • In the 12-bit ADC operating conditions, revised Conditions for Ground voltage. Revised min Ref High Voltage • In the 12-bit DAC operating requirements, revised the min and max value of VREFH_ADC • In the SDHC switching specifications, revised the max value of SD6 • In the 24MHz external oscillator electrical characteristics table, revised the min value of VIH and max value of VIL
Rev 7	November 2014	• Updated list of security features on page 1. • In "Part number format" figure, updated explanation for '1'. • In "Fields" table, updated definition of 'R'. • In "Part Numbers" table, added parts SVF331R3K1CKU2, SVF531R3K1CMK4, and SVF532R2K1CMK4. • In "External NPN ballast" section, updated recommendations for transistor selection. • In "DDR parameters" section, updated table footnotes regarding typical condition. • In "Power sequencing" table, added comment regarding SDRAMC_VDD1P5: "In case the Ballast transistor's collector is connected to the 1.5 V DRAM supply (instead of the 3.3 V

Table 82. Revision History

Rev. No.	Date	Substantial Changes
		supply), turn this 1.5 V supply on before turning on the 3.3V." • In "VideoADC specifications" table, added supply current values. • In "Receive and Transmit signal timing specifications," added the following note: "See the most current errata document when using the internally generated RXCLK and TXCLK clocks." • Updated "QuadSPI timing" section, presenting data based on a negative edge data launch from the device and a negative edge data capture; updated the figure, "QuadSPI Input/Read timing (SDR mode)"; updated the table, "QuadSPI Input/Read timing (SDR mode)." • For the "SDHC switching specifcations" table, added the statement, "A load of 50 pF is assumed"; updated max value for SD6, SDHC output delay (output valid). • In the "24 MHz oscillator specifications" section, added the statement, "The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5." • In "Pinouts" section, for the 176LQFP package, added information about exposed pad on the bottom side. • In "Special Signal Considerations" table, added that a "fundamental-mode" crystal should be connected between XTAL and EXTAL; updated maximum drive level of crystal rating to 250 µW.