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RAM Size	-
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Operating Temperature	-
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Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf511r3k1cmk4

5 Operating Requirements

5.1 Thermal operating requirements

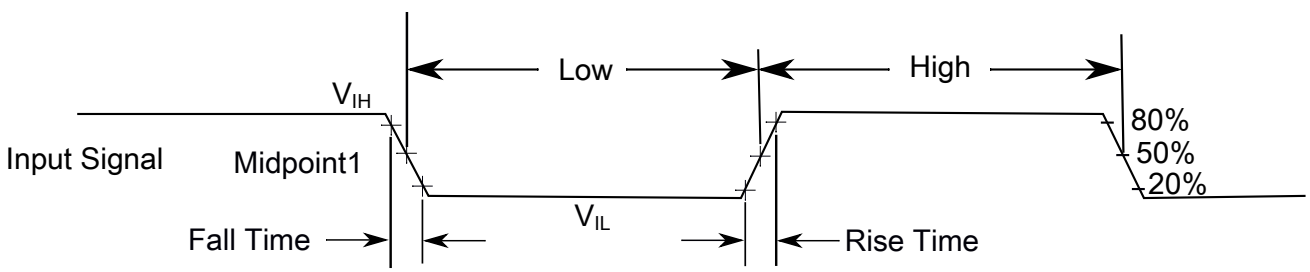
Table 1. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature	–40	85	°C
T_J	Junction temperature		105	°C

6 General

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

6.2.2 LVD electrical specifications

6.2.2.1 Main Supply electrical characteristics

Table 9. LVD_MAIN supply electrical characteristics

Main Supply LVD Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold (value @27°C)		2.76	2.915	V	
Lower voltage threshold (value @27°C)	2.656	2.73		V	
Time constant of RC filter at LVD input (0.69*RC)	3.3			µs	3.3 V noise rejection at LVD comparator input

6.2.2.2 LVD DIG characteristics

Table 10. LVD DIG electrical specifications [HPREG(RUN MODE) and LPREG(STOP MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.135	1.16	1.185	V	
Lower voltage threshold	1.105	1.13	1.155	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

Table 11. LVD DIG electrical specifications [ULPREG(STANDBY MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.105	1.13	1.155	V	
Lower voltage threshold	1.075	1.10	1.125	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

6.2.3 LDO electrical specifications

6.2.3.1 LDO_1P1

Table 12. LDO_1P1 parameters

Specification	Min	Typ	Max	Unit	Comments
VDDIO	3	3.3	3.6	V	IO supply
VDD1P1_OUT	0.9	1.1	1.2	V	Regulator output
I_out	-		150	mA	>= 300mV drop out
Regulator output programming range	0.8	1.1	1.4	V	Programmable in 25mV steps
Brownout Voltage	0.85	0.94		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

For additional information, see the device reference manual.

6.2.3.2 LDO_2P5

Table 13. LDO_2P5 parameters

Specification	Min	Typ	Max	Unit	Comments
VDDIO	3	3.3	3.6	V	IO supply
VDD2P5_OUT	2.3	2.5	2.6	V	Regulator output
I_out	-		350	mA	@500mV drop out
Regulator output programming range	2.0	2.5	2.75	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.25	2.33		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

For additional information, see the reference manual.

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV

6.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

6.2.8 Capacitance attributes

Table 18. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

7 I/O parameters

7.1 GPIO parameters

Table 19. GPIO DC operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi[1]	Core internal supply voltage		1.2		V
ovdd	I/O output supply voltage	3	3.3	3.6	V

1. This is internally controlled.

Table 20. GPIO DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voh	High-level output voltage	Ioh= -1mA	ovdd-0.15			V

Table continues on the next page...

Table 22. Output Buffer Average Impedance (3.3V power mode) (continued)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
		1 0 0	30	37	58	
		1 0 1	24	30	46	
		1 1 0 Extra drive strength	20	25	38	
		1 1 1	17	20	32	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.2 DDR parameters

Table 23. DDR operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi	Core internal supply voltage	1.16	1.23	1.26	V
ovdd	I/O output supply voltage (DDR3 mode)	1.425	1.5	1.575	V
ovdd	I/O output supply voltage (LPDDR2 mode)	1.14	1.2	1.26	V
vdd2p5	I/O PD predriver and level shifters supply voltage	2.25	2.5	2.75	V

Table 24. LPDDR2 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.9*ovdd			V	Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.
Vol	Low-level output voltage				0.1*ovdd	V	
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	
Vih(dc)	DC input high voltage		Vref+0.13		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.13	V	
Vih(diff)	DC differential input logic high		0.26		Note[1]	V	
Vil(diff)	DC differential input logic low		Note		-0.26	V	

Table continues on the next page...

NOTE

WBREG is the Well Bias Regulator. Supplies PD1 WELL during well bias modes.

8.3 Absolute maximum ratings

NOTE

These are the values above which device can get damaged. Refer to the recommended operating conditions table for intended use case values

Table 29. Absolute maximum ratings

Symbol	Parameters	Min	Max	Unit
USB0_VBUS	VBUS supply for USB	-	5.25	V
USB1_VBUS	VBUS supply for USB	-	5.25	V
USB_DCAP	USB LDO 5V->3.3V Outpu	-0.3	3.6	V
VBAT	Battery supply in case of LDOIN fails	-0.3	3.6	V
VDD33_LDOIN	LDO input supply	-0.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	-0.3	1.3	V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR, EFUSE	-0.3	3.6	V
VDD33	GPIO 3.3V IO supply	-0.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	-0.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	-0.3	3.6	V
VREFH_ADC	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)	-0.3	1.3	V
FA_VDD	Test purpose only	-0.3	1.3	V
VDD	1.2V core supply	-0.3	1.3	V
SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	-0.3	1.975	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	-0.3	3.6	V

8.4 Recommended operating conditions

Table 30. Recommended operating conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
USB0_VBUS	VBUS supply for USB w.r.t USB0_GND		4.4	5	5.25	V
USB1_VBUS	VBUS supply for USB w.r.t USB1_GND		4.4	5	5.25	V
USB_DCAP	USB LDO 5V->3 V Output	External DCAP (10uF termination for USBREG)		3		V
VBAT	Battery supply in case of LDOIN fails	External CAP 0.1uF	2.4	3.3	3.6	V
VDD33_LDOIN	LDO input supply		3	3.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	Recommended External DCAP: 1uF(Min) 10uF (Max)		1.1		V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR pre-driver, EFUSE	Recommended External DCAP: 1uF(Min) 10uF (Max)		2.5		V
VDD33	GPIO 3.3V IO supply	External CAP (10uF)	3	3.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	External CAP (10uF)	3	3.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	External CAP (10uF)	3	3.3	3.6	V
VREFH_ADC	High reference voltage for ADC and DAC	Relation with VDDDA33_ADC (1uF)	2.5	3.3	VDDA33_ADC	V
VREFL_ADC	Low reference voltage for ADC and DAC	External CAP (10uF)		0		V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	External CAP 10uF	3	3.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)		1.16	1.23	1.26	V
FA_VDD	For testing purpose only should be shorted to VDD on board.		1.16	1.23	1.26	V
VDD[1]	1.2V core supply	4.7uF with a low ESR value (100 milliohms)	1.16	1.23	1.26	V
USB0_GND	Ground supply for USB			0		V
USB1_GND	Ground supply for USB			0		V
VSS_KEL0	USB LDO ground output			0		V
VSS	VSS ground			0		V
VSSA33_ADC	Ground supply for ADC, DAC and IO segment			0		V

Table continues on the next page...

Module	Name	Recommendation if Unused
USB	USB_DCAP, USB0_VBUS, USB1_VBUS	Connect USBx_VBUS and USB_DCAP together and tie to ground through a 10K ohm resistor. Do NOT tie directly to ground, latch-up risk.
	USB0_GND, USB1_GND	Ground
	USB0_VBUS_DETECT, USB1_VBUS_DETECT	Float
	USB0_DM, USB0_DP, USB1_DM, USB1_DP	Float
Video ADC	VDDA33_AFE	3.3V or Float
	VDD12_AFE	1.2V or Float
	VADC_AFE_BANDGAP	Float
	VADCSE0, VADCSE1, VADCSE2, VADCSE3	Ground or Float

9 Peripheral operating requirements and behaviours

9.1 Analog

9.1.1 12-bit ADC electrical characteristics

9.1.1.1 12-bit ADC operating conditions

Table 31. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.5	-	3.6	V	-
	Delta to V_{DDAD} (VDD-VDDAD)	ΔVDDAD	-100	0	100	mV	-
Ground voltage	Delta to V_{SSAD} (VSS-VSSAD)[2]	ΔVSSAD	-100	0	100	mV	-
Ref Voltage High	-	V_{REFH}	1.5	V_{DDAD}	V_{DDAD}	V	-
Ref Voltage Low	-	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	-
Input Voltage	-	V_{ADIN}	V_{REFL}	-	V_{REFH}	V	-
Input Capacitance	8/10/12 bit modes	C_{ADIN}	-	1.5	2	pF	-
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	-	5	7	kohms	-
	ADLPC=0, ADHSC=0		-	12.5	15	kohms	-
	ADLPC=1, ADHSC=0		-	25	30	kohms	-

Table continues on the next page...

9.1.1.2 12-bit ADC characteristics

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	Symb	Min	Typ	Max	Unit	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}		250		µA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
Supply Current	Stop, Reset, Module Off	I_{DDAD}		0.01	0.8	µA	
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}		10		MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADHSC=1			20			
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp		2		cycles	
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv		28		cycles	
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv		0.7		µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			

Table continues on the next page...

9.5.4.2 DDR3 Read Cycle

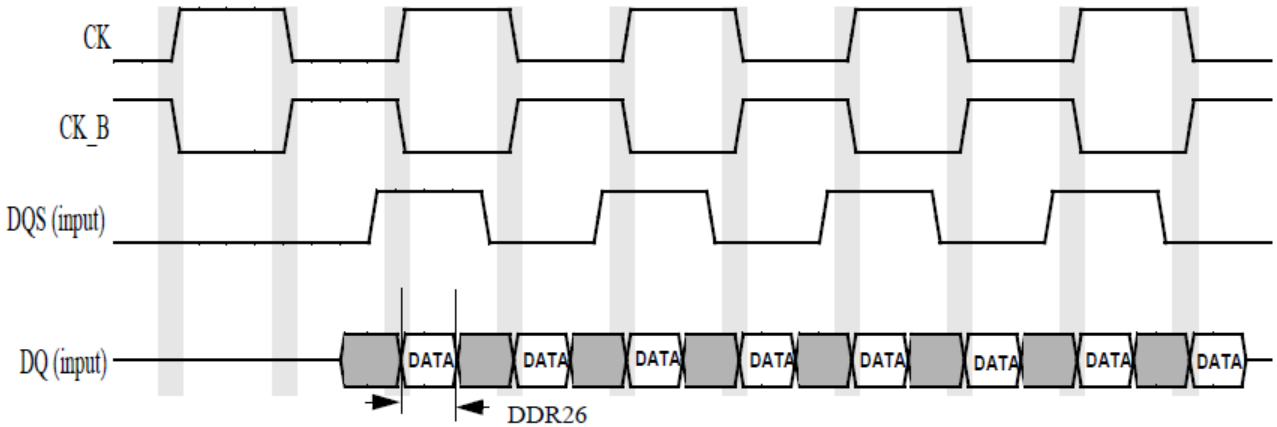


Figure 42. DDR3 Read Cycle

Table 55. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	-	750	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.5.4.4 LPDDR2 Timing Parameter

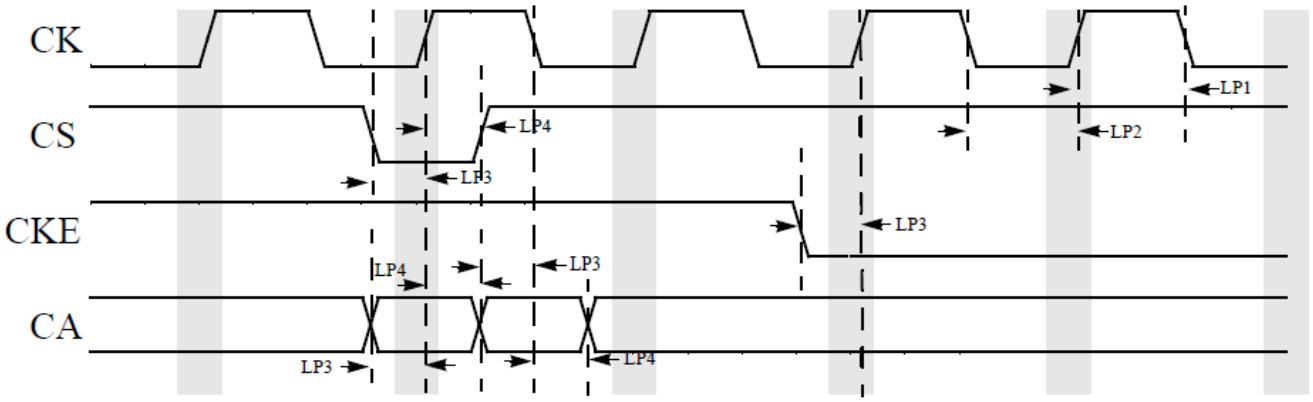


Figure 44. LPDDR2 Command and Address timing parameter

NOTE

RESET pin has a external weak pull DOWN requirement if LPDDR2 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has a external weak pull UP requirement if LPDDR2 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 57. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	tCH	0.45	0.55	tCK
LP2	SDRAM clock LOW-level width	tCL	0.45	0.55	tCK
LP3	CS, CKE setup time	tIS	230	-	ps
LP4	CS, CKE hold time	tIH	230	-	ps
LP3	CA setup time	tIS	230	-	ps
LP4	CA hold time	tIH	230	-	ps

NOTE

All measurements are in reference to Vref level.

9.6.6 USB PHY specifications

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

9.7 Clocks and PLL Specifications

9.7.1 24 MHz Oscillator Specifications

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5.

Table 67. 24MHz external oscillator electrical characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
f_{osc}	Crystal oscillator range	—	—	24	—	MHz
I_{osc}	Startup current	—	—	< 5	—	mA
t_{uposc}	Oscillator startup time	—	—	< 5	—	ms

Table continues on the next page...

Table 68. OSC32K Main Characteristics (continued)

	Notes	Min	Typ	Max
	oscillator is running. Another 1.5 µA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 µA on vdd_rtc when the ring oscillator is not running.			
Bias resistor	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.		14 MΩ	
Crystal Properties				
Cload	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal		12.5 pF	
ESR	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.		50 kΩ	

9.7.3 Fast internal RC oscillator (24 MHz) electrical characteristics

This section describes a fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 69. Fast internal oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCM}	RC oscillator high frequency	T_A= 25 °C, trimmed	—	24	—	MHz
I_{RCMRUN}	RC oscillator high frequency current in running mode	T_A= 25 °C, trimmed	—	55		µA
I_{RCMPWD}	RC oscillator high frequency current in power down mode	T_A= 25 °C		100		nA
RCMTRIM	RC oscillator precision after trimming of f_{RC}	T_A= 25 °C	-1	—	+1	%
RCMVAR	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration		-5		+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A18	142	PTB24		PTB24	SAI0_RX_BCLK	SCI1_RX		FB_MUXED_TSIZ0	NF_WE_b	SCI3_CTS	DCU1_G4	
B17	149	PTB25		PTB25	SAI0_RX_DATA	SCI1_RTS		FB_CS1_b	NF_CE0_b		DCU1_G5	
A17	150	PTB26	RCON21	PTB26	SAI0_TX_DATA	SCI1_CTS	RCON21	FB_CS0_b	NF_CE1_b		DCU1_G6	
U8	57	PTB27	RCON22	PTB27	SAI0_RX_SYNC		RCON22	FB_OE_b	FB_MUXED_TBST_b	NF_RE_b	DCU1_G7	
A16	151	PTB28	RCON23	PTB28	SAI0_TX_SYNC		RCON23	FB_RW_b			DCU1_B6	
D16	153	PTC26	RCON24	PTC26	SAI1_TX_BCLK	SPI0_PCS5	RCON24	FB_TA_b	NF_RB_b		DCU1_B7	
E16	154	PTC27	RCON25	PTC27	SAI1_RX_BCLK	SPI0_PCS4	RCON25	FB_BE3_b	FB_CS3_b	NF_ALE	DCU1_B2	
E15	155	PTC28	RCON26	PTC28	SAI1_RX_DATA	SPI0_PCS3	RCON26	FB_BE2_b	FB_CS2_b	NF_CLE	DCU1_B3	
C16	152	PTC29	RCON27	PTC29	SAI1_TX_DATA	SPI0_PCS2	RCON27	FB_BE1_b	FB_MUXED_TSIZ1		DCU1_B4	
T8	58	PTC30	RCON28	PTC30	SAI1_RX_SYNC	SPI1_PCS2	RCON28	FB_MUXED_BE0_b	FB_TSIZ0	ADC0_SE5	DCU1_B5	
W5	42	PTC31	RCON29	PTC31	SAI1_TX_SYNC		RCON29			ADC1_SE5	DCU1_B6	
N16	103	PTE0	BOOTMOD1	PTE0	DCU0_HSYNC/DCU0_TCON1	BOOTMOD1		LCD0				
N18	104	PTE1	BOOTMOD0	PTE1	DCU0_VSYNC/DCU0_TCON2	BOOTMOD0		LCD1				
N19	105	PTE2		PTE2	DCU0_PCLK			LCD2				
Y15	77	PTE3		PTE3	DCU0_TAG/DCU0_TCON0			LCD3				
N20	106	PTE4		PTE4	DCU0_DE/DCU0_TCON3			LCD4				
T16	80	PTE5		PTE5	DCU0_R0			LCD5				
W16	81	PTE6		PTE6	DCU0_R1			LCD6				
M20	109	PTE7	RCON0	PTE7	DCU0_R2		RCON0	LCD7				
M19	110	PTE8	RCON1	PTE8	DCU0_R3		RCON1	LCD8				
M17	111	PTE9	RCON2	PTE9	DCU0_R4		RCON2	LCD9				
M16	112	PTE10	RCON3	PTE10	DCU0_R5		RCON3	LCD10				
L16	113	PTE11	RCON4	PTE11	DCU0_R6		RCON4	LCD11				
L17	114	PTE12	RCON5	PTE12	DCU0_R7	SPI1_PCS3	RCON5	LCD12			LPT_ALT0	
Y16	78	PTE13		PTE13	DCU0_G0			LCD13				

Table 79. Special Signal Considerations (continued)

Special Signal	Comments
JTCLK, JTDI, JTDO, JTMS	For JTAG the use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is matched. For example, do not use an external pull down on an input that has on-chip pull-up. JTDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTDO is detrimental and should be avoided.
LVDS0N, LVDS0P	Not recommended for application use, intended for clock observation purposes during debug only.
RESETB/RESET_OUT	Active low input used to generate a system wide reset (except the SRTC). A glitch filter is include to help prevent unexpected resets, a minimum pulse width of 125 nsecs is required to guarantee a reset is detected.
XTAL, EXTAL	A 24.0 MHz fundamental mode crystal should be connected between XTAL and EXTAL. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTAL must be directly driven by the external oscillator and EXTAL floated. The XTAL signal level must swing from ~0.8 x DECAP_V11_ LDO_OUT to ~0.2 V.
XTAL32, EXTAL32	If the user wishes to configure XTAL32 and EXTAL32 as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between XTAL32 and EXTAL32. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTAL32 and EXTAL32 to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTAL32 and EXTAL32 should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTAL32 the EXTAL32 pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed DECAP_V11_ LDO_OUT level and the frequency should be <100 kHz under typical conditions. In the case where the SIRC is used, it is recommended to connect XTAL32 to ground and leave EXTAL32 floating.

Table 80. Power Supply Pins (continued)

Supply Rail Name	364 MAP BGA	176 LQFP (R-series ONLY)	Comment
VSS	A1, A20, B3, B5, B8, B11, B13, B16, B19, C2, D17, E5, E8, E11, E14, E19, F2, G8, G10, G12, G14, G17, H4, H7, H9, H11, H13, H19, J2, J8, J9, J10, J11, J12, J14, J18, K7, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L14, L19, M2, M4, M7, M9, M10, M11, M12, M13, M18, N8, N10, N12, N14, P7, P9, P11, P13, P19, R2, R18, U7, U19, V11, V13, V17, W6, Y1, Y20	1, 13, 20, 25, 45, 67, 74, 82, 96, 107, 139, 144, 157, 175, 176, FLG	Ground. Connect "Flag pad (FLG)" to the internal GND plane with numerous vias—for both electrical and thermal purposes.
VSSA33_ADC	V2	32	ATD Ground
VSS12_AFE	R5	38	Video ADC Ground
VSSA33_AFE	V4	39	Video ADC Ground
VSS_KEL0	U11	66	Ground (VSS and VSS_KEL0 are NOT connected internally)

14 Functional Assignment Pins

14.1 Functional Assignment Pins

Table 81. Functional Assignment Pins

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
ADC0SE8	Y2	—	VDDA33_ADC	Analog	—	ADC0SE8	—	—
ADC0SE9	W2	—	VDDA33_ADC	Analog	—	ADC0SE9	—	—
ADC1SE8	W3	—	VDDA33_ADC	Analog	—	ADC1SE8	—	—
ADC1SE9	Y3	—	VDDA33_ADC	Analog	—	ADC1SE9	—	—
BCTRL	T2	26	VDDREG	Analog	—	BCTRL	—	—
DACO0	U1	29	VDDA33_ADC	Analog	—	DACO0	—	—
DACO1	U2	30	VDDA33_ADC	Analog	—	DACO1	—	—
DDR_A[0]	C7	—	SDRAMC_VDD2P5	DDR	—	DDR_A[0]	—	—

Table continues on the next page...

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_A[1]	C11	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[1]	—	—
DDR_A[2]	A8	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[2]	—	—
DDR_A[3]	B7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[3]	—	—
DDR_A[4]	A6	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[4]	—	—
DDR_A[5]	B6	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[5]	—	—
DDR_A[6]	A9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[6]	—	—
DDR_A[7]	A7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[7]	—	—
DDR_A[8]	A11	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[8]	—	—
DDR_A[9]	B9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[9]	—	—
DDR_A[10]	D7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[10]	—	—
DDR_A[11]	D10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[11]	—	—
DDR_A[12]	C10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[12]	—	—
DDR_A[13]	A10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[13]	—	—
DDR_A[14]	D9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[14]	—	—
DDR_A[15]	B10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[15]	—	—
DDR_BA[0]	C8	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[0]	—	—
DDR_BA[1]	C9	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[1]	—	—
DDR_BA[2]	D8	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[2]	—	—
DDR_CAS_ b	B4	—	SDRAMC_ VDD2P5	DDR	—	DDR_CAS_ b	—	—
DDR_CKE[0]	A5	—	SDRAMC_ VDD2P5	DDR	—	DDR_CKE[0]	—	—
DDR_CLK[0]	A2	—	SDRAMC_ VDD2P5	DDR	—	DDR_CLK[0]	—	—

Table continues on the next page...

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_DQS_b[0]	E3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS_b[0]	—	—
DDR_DQS[1]	E1	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[1]	—	—
DDR_DQS_b[1]	F1	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS_b[1]	—	—
DDR_ODT[0]	C4	—	SDRAMC_VDD2P5	DDR	—	DDR_ODT[0]	—	—
DDR_ODT[1]	B1	—	SDRAMC_VDD2P5	DDR	—	DDR_ODT[1]	—	—
DDR_RAS_b	A4	—	SDRAMC_VDD2P5	DDR	—	DDR_RAS_b	—	—
DDR_RESET	D6	—	SDRAMC_VDD2P5	DDR	—	DDR_RESET	—	—
DDR_VREF	G5	—	SDRAMC_VDD2P5	DDR	—	DDR_VREF	—	—
DDR_WE_b	C6	—	SDRAMC_VDD2P5	DDR	—	DDR_WE_b	—	—
DDR_ZQ	A3	—	SDRAMC_VDD2P5	DDR	—	DDR_ZQ	—	—
EXT_POR	T1	23	VDD33	GPIO	—	EXT_POR	—	—
EXT_TAMPER0	T14	—	VBAT	Analog	—	EXT_TAMPER0	—	—
EXT_TAMPER1	U14	—	VBAT	Analog	—	EXT_TAMPER1	—	—
EXT_TAMPER2/ EXT_WM0_TAMPER_IN	T13	—	VBAT	Analog	—	EXT_TAMPER2/ EXT_WM0_TAMPER_IN	—	—
EXT_TAMPER3/ EXT_WM0_TAMPER_OUT	U13	—	VBAT	Analog	—	EXT_TAMPER3/ EXT_WM0_TAMPER_OUT	—	—
EXT_TAMPER4/ EXT_WM1_TAMPER_IN	U12	—	VBAT	Analog	—	EXT_TAMPER4/ EXT_WM1_TAMPER_IN	—	—
EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	U10	—	VBAT	Analog	—	EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	—	—

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15 Revision History

The following table provides a revision history for this document.

Table 82. Revision History

Rev. No.	Date	Substantial Changes
Rev1	12/2011	Initial release
Rev2	02/2012	Updated feature list Updated VREG electrical specifications Updated LDO_1P1, LDO2P5 tables Updated DDR IO parameters Added DDR memory controller parameters Updated Power sequencing table Added Power supply diagram Updated Recommended operating conditions Replaced DryIce Tamper Electrical Specifications with Voltage and temperature monitor electrical specifications Updated VideoADC electricals. Updated VideoADC supply scheme diagram. Added VideoADC supply_decoupling diagram Added QuadSPI DDR mode electrical specifications Updated Fast internal RC oscillator table Updated Slow internal RC oscillator table Updated Pinouts section
Rev3	04/2012	Updated device name throughout the document Minor editorial updates in the feature list Updated VREG electrical specifications Updated LDO electrical specifications Updated Power consumption operating behaviors table Added USB PHY Current Consumption table Updated GPIO parameters Updated DDR parameters

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		Added WBREG specifications Updated Recommended operating conditions table Updated DAC INL and DNL charts Updated Pinouts
Rev 5	April 2013	• Removed references to VF1xxR and refernces to F100 and 144 LQFP and 256 MAPBGA • Replaced references to Auto and IMM by R-series and F-series respectively • In the feature list, the ARM Core frequency changed to 500 MHz for F-series • In the feature list, changed the DRAM controller frequency • Updated Part Nummbering format • Clarified the Fields table as per Marketing • Sample numbers updated • From the VREG electrical specifications tables, deleted pre-trimming rows and comments • .In the HPREG electrical characteristics table, add footnote on maximum Output Current Capacity • In the ULPREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the WBREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the LVD electrical specifications table, added typ. values of Upper voltage threshold (value @27oC) and Lower voltage threshold (value @27oC) • In the LVD DIG electrical specifications table, removed pretrimming values and clarified other values • Updated LVD DIG electrical specifications values • Updated LDO_1P1 tables • Updated LDO_2P5 table • Updated Power consumption operating behaviors tables • Updated Absolute maximum ratings table

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