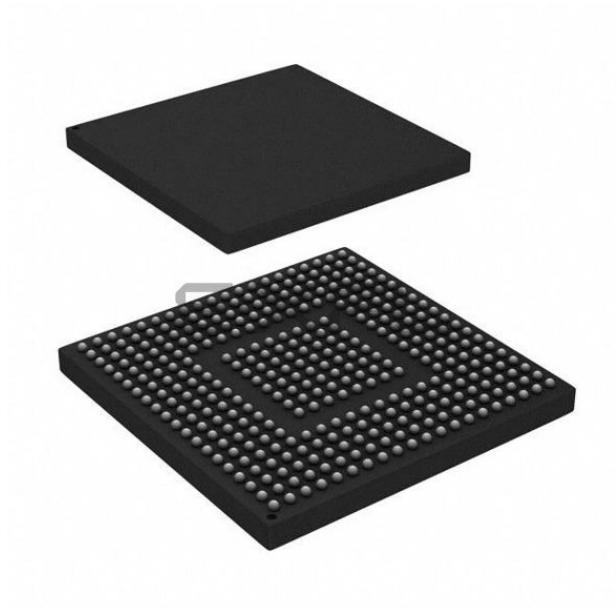

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf512r3k1cmk4

Field	Description	Values
M	Memory option	• 3 = Standard (1.5MB SRAM) • 2 = Optional (1MB SRAM and 512K L2 Cache)
T	Temperature spec	• C = -40 ^{0}C to +85 ^{0}C T_a
P	Package	• KU = 176LQFP • MK = 364BGA
S	Speed (A5 core)	• 2 = 266MHz • 4 = 400MHz

2.4 Part Numbers

This table lists the part numbers on the device.

Part Number	Package	Description
SVF311R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, 176LQFP-EP
SVF312R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, OpenVG GPU, 176LQFP-EP
SVF321R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, M4, 176LQFP-EP
SVF322R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, M4, OpenVG GPU, 176LQFP-EP
SVF331R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, 176LQFP-EP
SVF332R3K1CKU2	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, OpenVG GPU, 176LQFP-EP
SVF511R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, 364BGA
SVF512R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, OpenVG GPU, 364BGA
SVF521R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4, 364BGA
SVF522R2K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4, L2 Cache, OpenVG GPU, 364BGA
SVF522R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4, OpenVG GPU, 364BGA
SVF531R3K1CMK4	MAP 364 17*171.5 P0.8	A5-400, M4 Primary, 364BGA
SVF532R2K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, L2 Cache OpenVG GPU, 364BGA
SVF532R3K1CMK4	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, OpenVG GPU, 364BGA

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 27. DDR3 mode AC Electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vih(ac)	AC input logic high		Vref+0.175	ovdd	V	Note that the JEDEC JESD79_3E specification supersedes any specification in this document
Vil(ac)	AC input logic low		ovss	Vref-0.175	V	
Vidh(ac)	AC differential input high voltage		0.35	-	V	
Vidl(ac)[1]	AC differential input low voltage		0.35		V	
Vix(ac)[2]	AC differential input crosspoint voltage	relative to ovdd/2	Vref-0.15	Vref+0.15	V	
Vpeak	Over/undershoot peak			0.4	V	
Varea	Over/undershoot area (above ovdd or below ovss)	at 800 MHz data rate		0.5	V*ns	
tsr	Single output slew rate		0.4	2	V/ns	
tskd	Skew between pad rise/fall asymmetry + skew cased by SSN			0.2	ns	

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

8 Power supplies and sequencing

8.1 Power sequencing

Table 28. Power sequencing

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VBAT	VBAT	Battery supply in case of LDOIN fails	NA	

Table continues on the next page...

9.1.1.2 12-bit ADC characteristics

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	Symb	Min	Typ	Max	Unit	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}		250		µA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
Supply Current	Stop, Reset, Module Off	I_{DDAD}		0.01	0.8	µA	
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}		10		MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADHSC=1			20			
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp		2		cycles	
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv		28		cycles	
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv		0.7		µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			

Table continues on the next page...

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

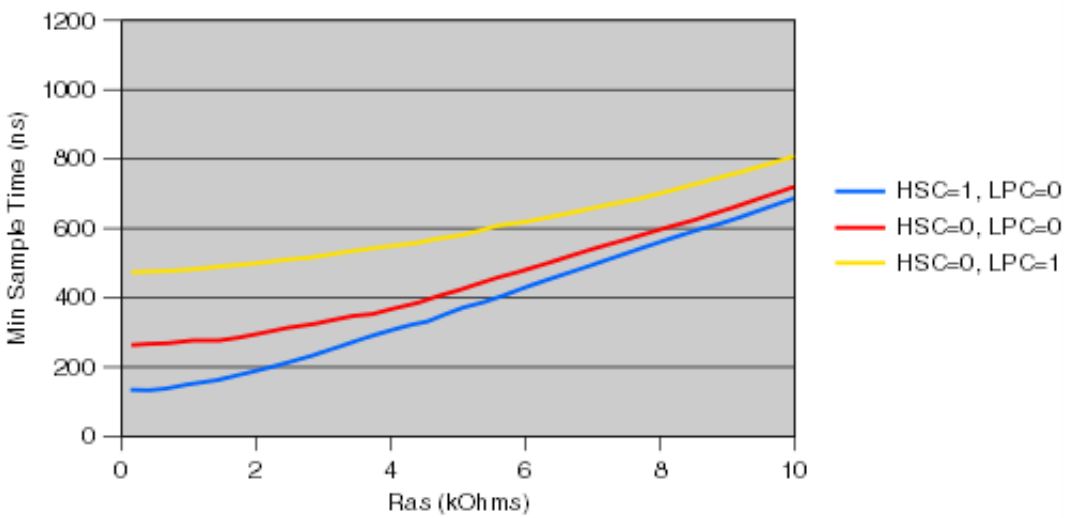


Figure 6. Minimum Sample Time Vs Ras (Cas = 2pF)

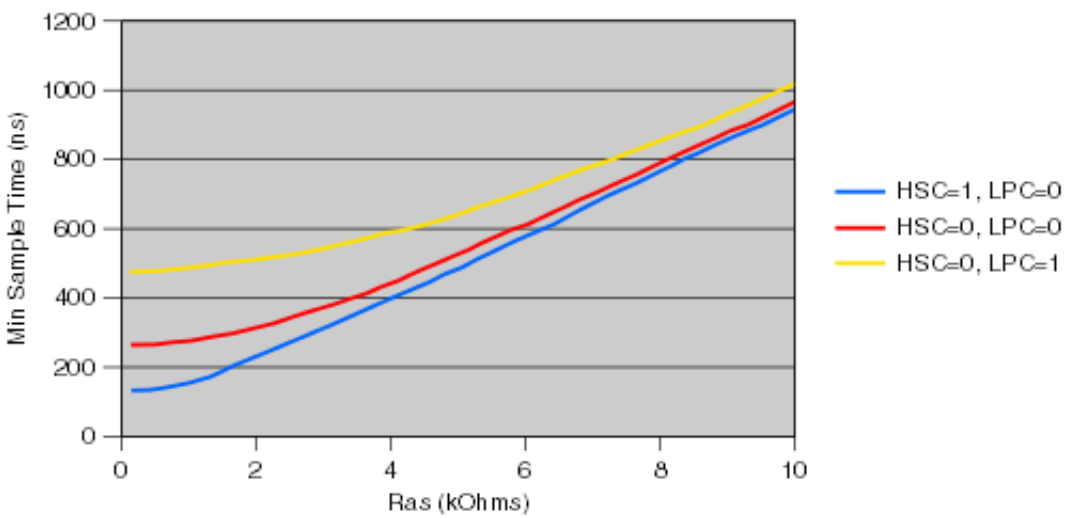


Figure 7. Minimum Sample Time Vs Ras (Cas = 5pF)

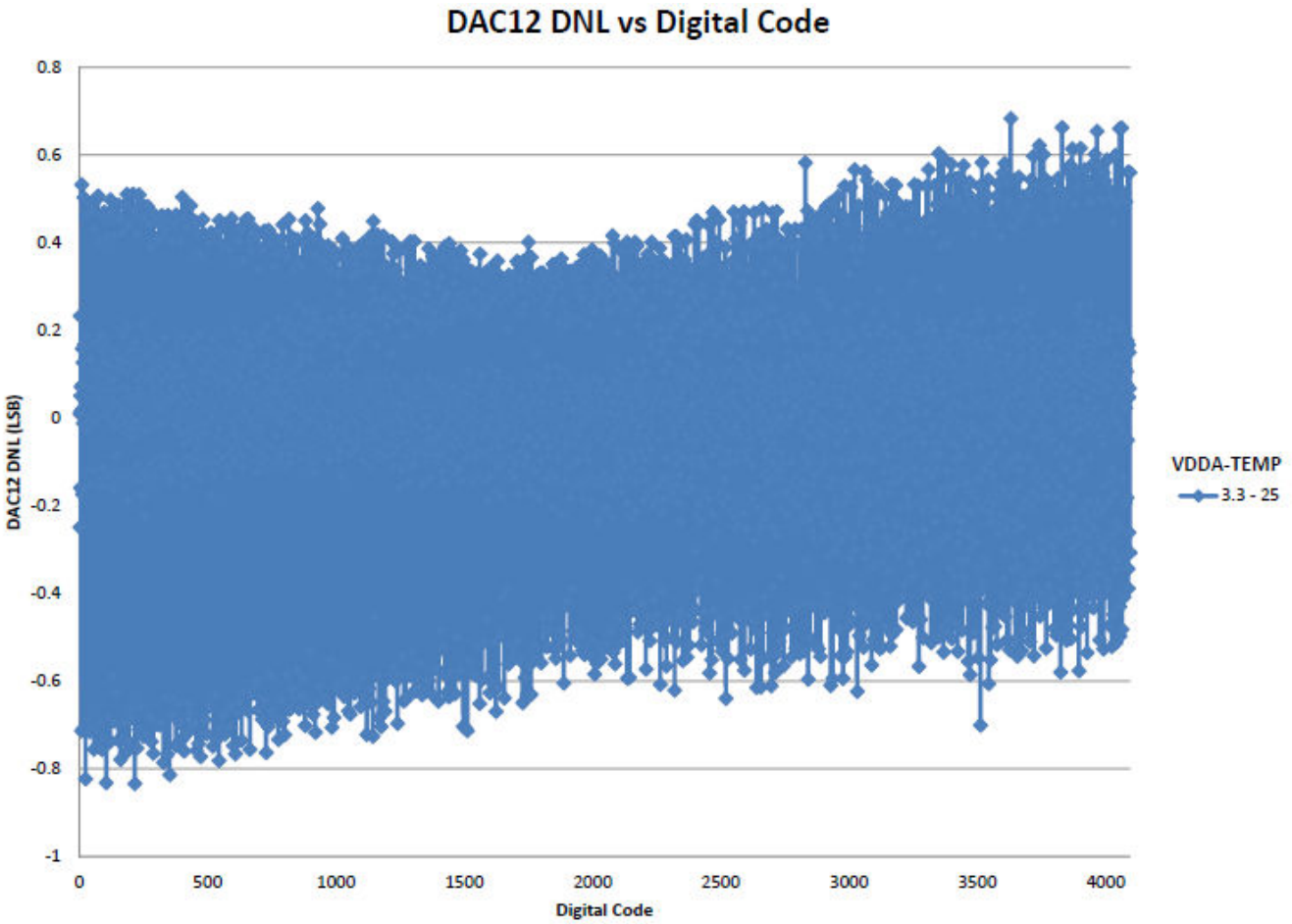
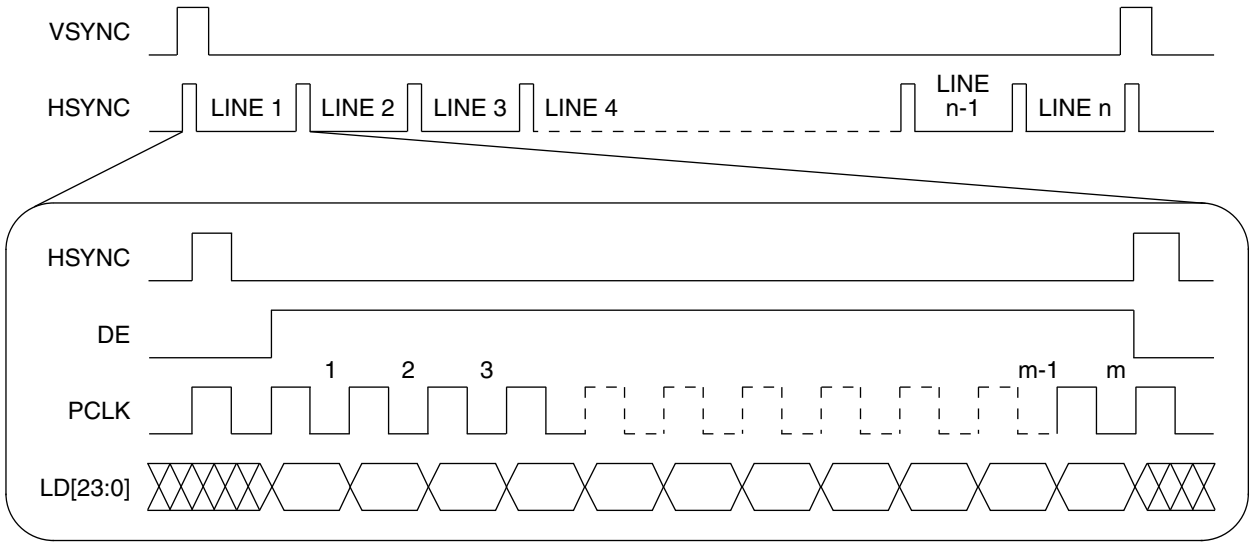


Figure 10. DNL error vs. digital code



9.2.1.2 Interface to TFT LCD Panels—Pixel Level Timings

This section provides the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the figure below are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high. Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the clock divide . The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 36. LCD interface timing parameters—horizontal and vertical

Symbol	Characteristic		Unit
t_{PCP}	Display pixel clock period	11.2	ns
t_{PWH}	HSYNC pulse width	PW_H * t_{PCP}	ns
t_{BPH}	HSYNC back porch width	BP_H * t_{PCP}	ns
t_{FPH}	HSYNC front porch width	FP_H * t_{PCP}	ns
t_{SW}	Screen width	DELTA_X * t_{PCP}	ns
t_{HSP}	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) * t_{PCP}	ns
t_{PWV}	VSYNC pulse width	PWV * t_{HSP}	ns
t_{BPV}	VSYNC back porch width	BP_V * t_{HSP}	ns
t_{FPV}	VSYNC front porch width	FP_V * t_{HSP}	ns
t_{SH}	Screen height	DELTA_Y * t_{HSP}	ns
t_{VSP}	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) * t_{HSP}	ns

9.2.3 LCD driver electrical characteristics

This section provides LCD driver electrical specification at V_{DD33} = 3.3 V ± 10%.

Table 39. LCD driver specifications

Symbol	Parameter	Min	Typical	Max	Unit
VLCD	Voltage on VLCD (LCD supply) pin with respect to VSS	0		VDD33 + 0.3	V
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VDDE, VSS	_	_	5.0	KΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VDDE2/3, VDDE1/2, VDDE/3)[1]	_	25	_	µA

1. With PWR=10, BSTEN=0, and BSTAO=0

9.3 Ethernet specifications

9.3.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. All Ethernet signals use pad type pad_fsr. The timing specifications described i the section assume a pad slew rate setting of 11 and a load of 50 pF[2].

9.3.2 Receive and Transmit signal timing specifications

This section provides timing specs that meet the requirements for RMII interfaces for a range of transceiver devices.

Table 40. Receive signal timing for RMII interfaces

	Characteristic	RMII Mode		Unit
		Min	Max	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
E3, E7	RMII_CLK pulse width high	35%	65%	RMII_CLK period

Table continues on the next page...

2. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

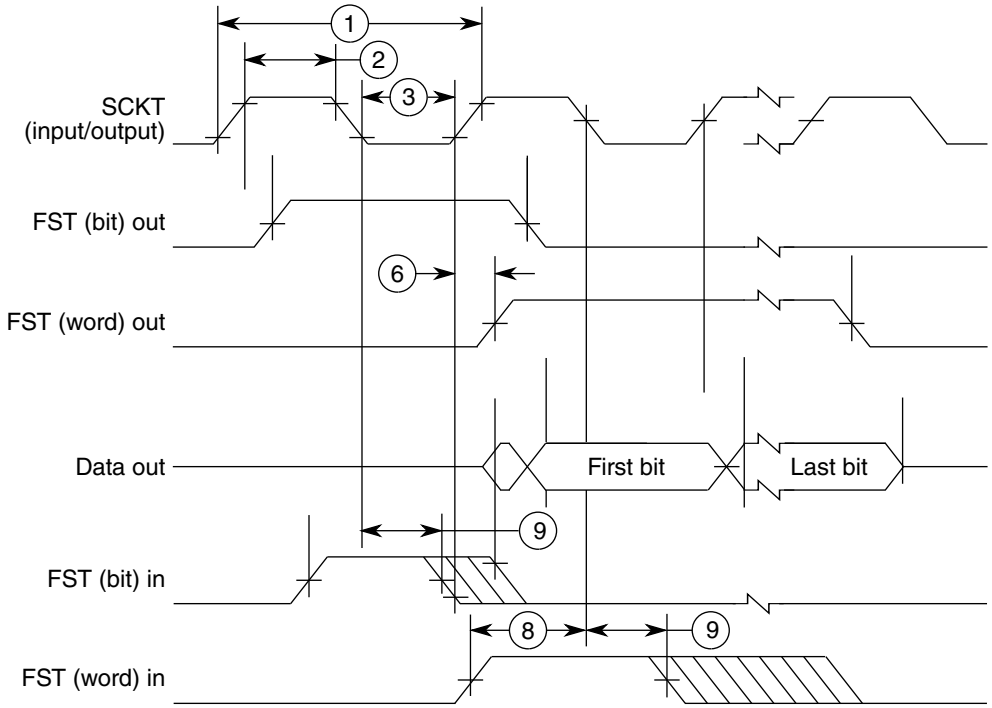


Figure 24. ESAI Transmitter Timing

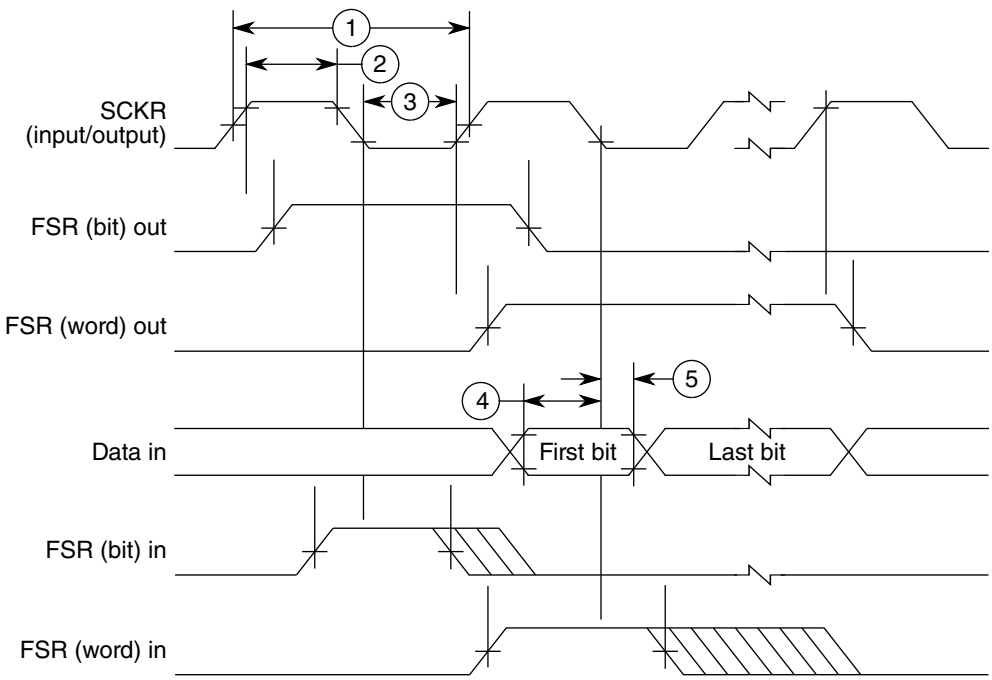


Figure 25. ESAI Receiver Timing

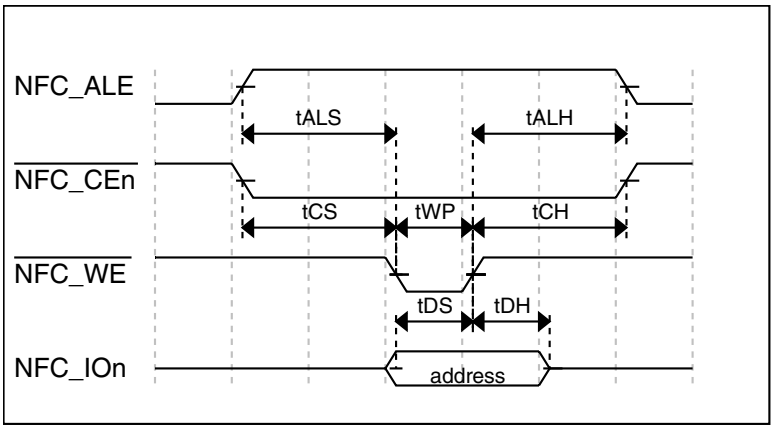


Figure 35. Address latch cycle timing

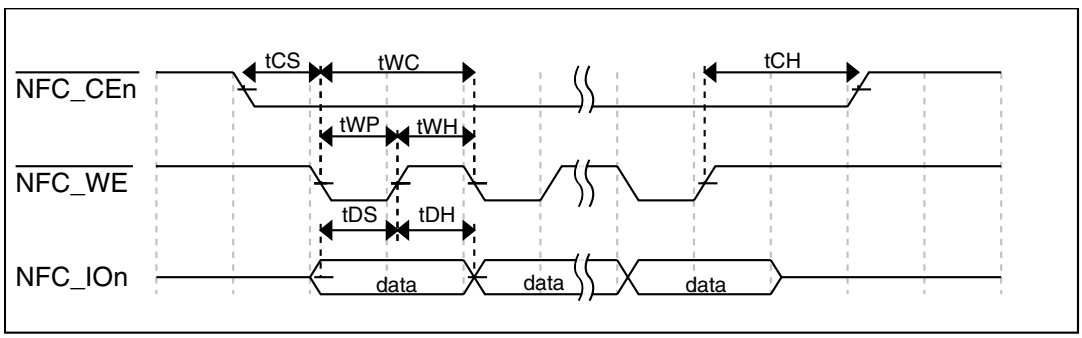


Figure 36. Write data latch cycle timing

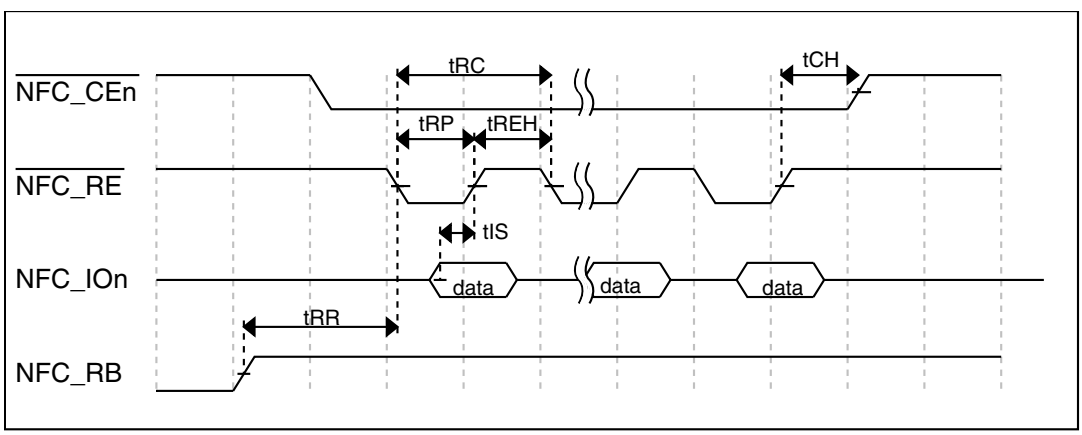


Figure 37. Read data latch cycle timing in non-fast mode

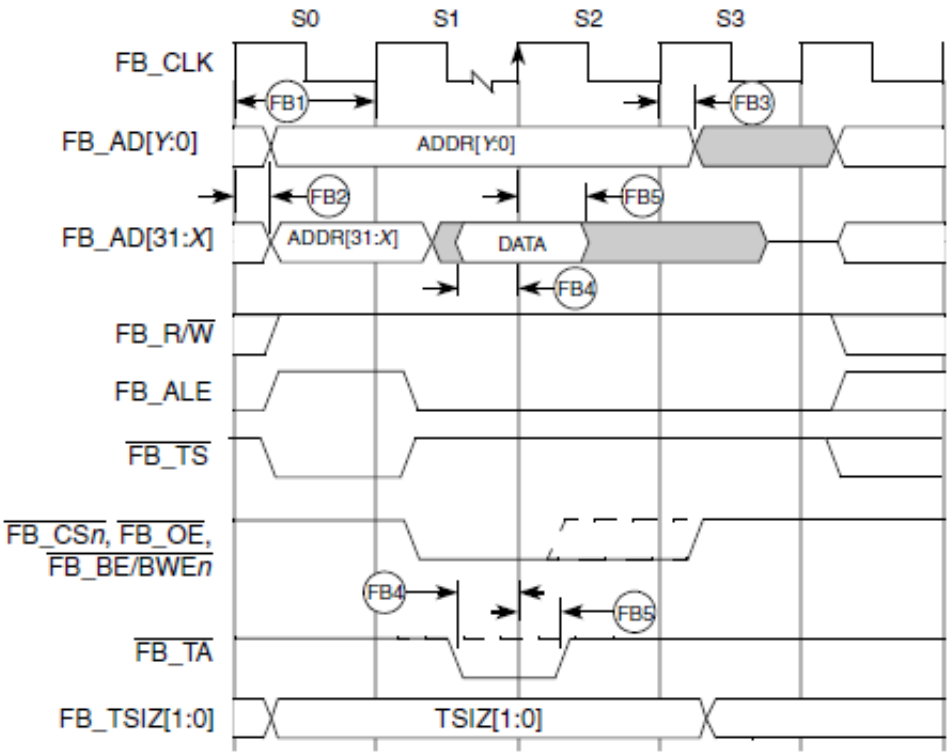


Figure 39. FlexBus read timing

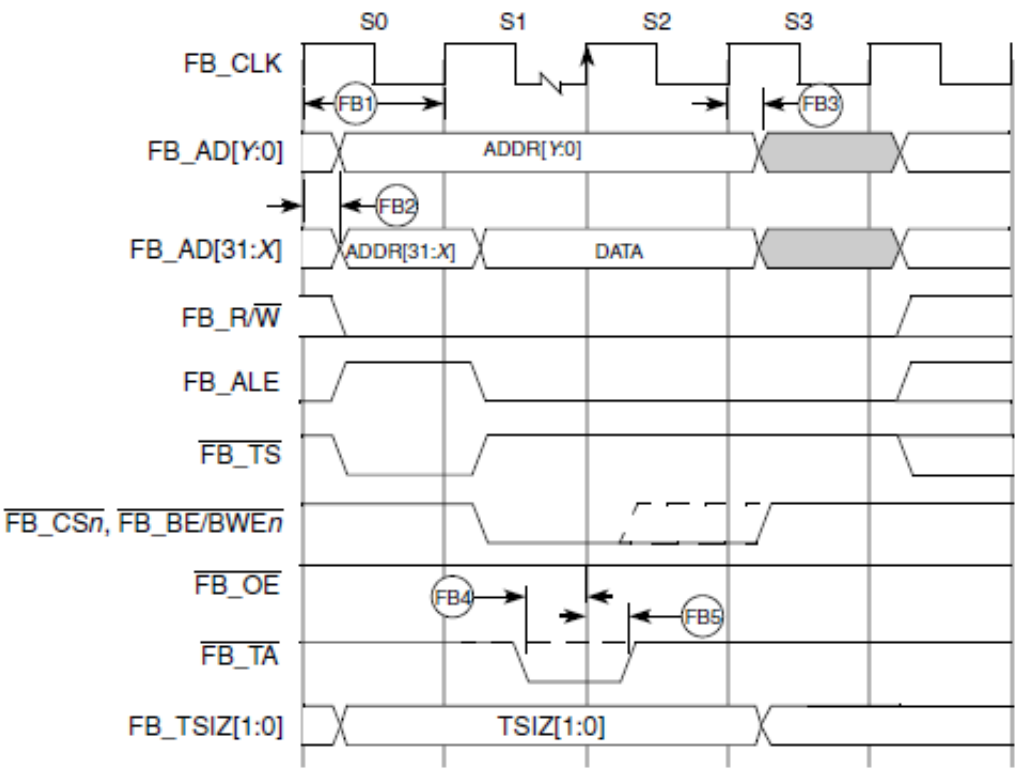


Figure 40. FlexBus write timing

NOTE

RESET pin has a external weak pull UP requirement if DDR3 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 54. DDR3 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tCK
DDR2	CK clock low-level width	tCL	0.47	0.53	tCK
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	440	-	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	315	-	ps
DDR6	Address output setup time	tIS	440	-	ps
DDR7	Address output hold time	tIH	315	-	ps

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.6.6 USB PHY specifications

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

9.7 Clocks and PLL Specifications

9.7.1 24 MHz Oscillator Specifications

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5.

Table 67. 24MHz external oscillator electrical characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
f_{osc}	Crystal oscillator range	—	—	24	—	MHz
I_{osc}	Startup current	—	—	< 5	—	mA
t_{uposc}	Oscillator startup time	—	—	< 5	—	ms

Table continues on the next page...

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C5	—	DDR_CS_b[0]			DDR_CS_b0							
D2	—	DDR_D[15]			DDR_D15							
H2	—	DDR_D[14]			DDR_D14							
C1	—	DDR_D[13]			DDR_D13							
G1	—	DDR_D[12]			DDR_D12							
E2	—	DDR_D[11]			DDR_D11							
H1	—	DDR_D[10]			DDR_D10							
D1	—	DDR_D[9]			DDR_D9							
J1	—	DDR_D[8]			DDR_D8							
G3	—	DDR_D[7]			DDR_D7							
C3	—	DDR_D[6]			DDR_D6							
J3	—	DDR_D[5]			DDR_D5							
F3	—	DDR_D[4]			DDR_D4							
G4	—	DDR_D[3]			DDR_D3							
D4	—	DDR_D[2]			DDR_D2							
H3	—	DDR_D[1]			DDR_D1							
F4	—	DDR_D[0]			DDR_D0							
G2	—	DDR_DQM[1]			DDR_DQM1							
J4	—	DDR_DQM[0]			DDR_DQM0							
E1	—	DDR_DQS[1]			DDR_DQS1							
D3	—	DDR_DQS[0]			DDR_DQS0							
F1	—	DDR_DQS_b[1]			DDR_DQS_b1							
E3	—	DDR_DQS_b[0]			DDR_DQS_b0							
A4	—	DDR_RAS_b			DDR_RAS_b							
C6	—	DDR_WE_b			DDR_WE_b							
C4	—	DDR_ODT[0]			DDR_ODT0							
B1	—	DDR_ODT[1]			DDR_ODT1							
G5	—	DDR_VREF			DDR_VREF							
A3	—	DDR_ZQ			DDR_ZQ							
D6	—	DDR_RESET			DDR_RESET							
J20	—	PTD31		PTD31	FB_AD31	NF_IO15		FTM3_CH0	SPI2_PCS1			
H20	—	PTD30		PTD30	FB_AD30	NF_IO14		FTM3_CH1	SPI2_PCS0			
H18	—	PTD29		PTD29	FB_AD29	NF_IO13		FTM3_CH2	SPI2_SIN			
H17	—	PTD28		PTD28	FB_AD28	NF_IO12	I2C2_SCL	FTM3_CH3	SPI2_SOUT			
H16	—	PTD27		PTD27	FB_AD27	NF_IO11	I2C2_SDA	FTM3_CH4	SPI2_SCK			
G16	—	PTD26		PTD26	FB_AD26	NF_IO10		FTM3_CH5	SDHC1_WP			
G18	—	PTD25		PTD25	FB_AD25	NF_IO9		FTM3_CH6				
G19	—	PTD24		PTD24	FB_AD24	NF_IO8		FTM3_CH7				

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G14	—	VSS			VSS							
J14	—	VSS			VSS							
L14	—	VSS			VSS							
N14	—	VSS			VSS							
N7	—	FA_VDD			FA_VDD							
V14	—	VBAT			VBAT							
—	FLG	VSS			VSS							

12.2 Pinout diagrams

NOTE

The 176 LQFP parts are not pin compatible between the F and R series families devices.

NOTE

If tamper detection is not required, the tamper pins must be tied to ground.

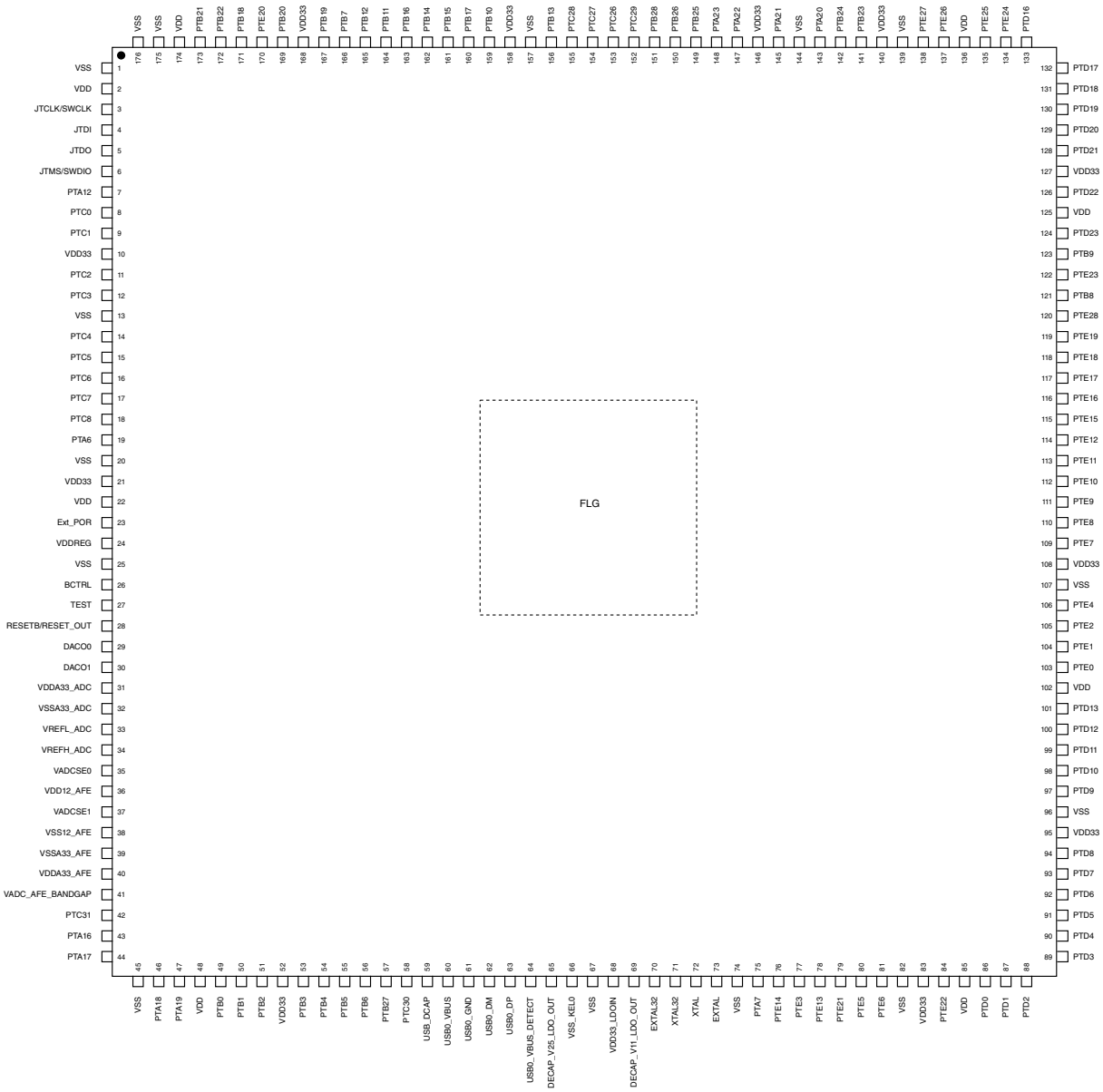


Figure 59. 176 LQFP Pinout Diagram

13 Power Supply Pins

13.1 Power Supply Pins

Table 80. Power Supply Pins

Supply Rail Name	364 MAP BGA	176 LQFP (R-series ONLY)	Comment
DECAP_V11_ LDO_OUT	V12	69	On-chip 1.1V LDO output
DECAP_V25_ LDO_OUT	T11	65	On-chip 2.5V LDO output (Intended to supply DRAM IO when required)
FA_VDD	N7	—	Factory Use Only (Connect to VDD, internally bonded in LQFP)
SDRAMC_ VDD1P5	D5, D11, E4, E7, E9, F5, H5, K5	DRAM not supported in LQFP	1.5V DDR3 DRAM Supply (1.2V for LPDDR2)
SDRAMC_ VDD2P5	E6, E10, J5	DRAM not supported in LQFP	2.5V DRAM Supply
USB_DCAP	Y10	59	On-chip 3V LDO output (Intended to be fed by external USB VBUS supply)
USB0_GND	V10	61	
USB1_GND	Y9	USB1 not supported in LQFP	
VADC_AFE_ BANDGAP	U5	41	Video ADC Bandgap Output
VBAT	V14	VBAT not supported in LQFP	On-chip SNVS regulator battery back-up supply option
VDD	G7, G9, G11, G13, H8, H10, H12, H14, J7, J13, K8, K14, L7, L13, M8, M14, N9, N11, N13, P8, P10, P12, P14	2, 22, 48, 85, 102, 125, 136, 174	1.2V Core Supply (Internally Regulated)
VDD33	C12, C15, C18, F18, K3, K17, N3, N17, T17, U16, V8, W18	10, 21, 52, 83, 95, 108, 127, 140, 146, 158, 168	3.3V IO Supply
VDDA33_ADC	V1	31	3.3V Analog To Digital convertor supply
VDD12_AFE	T5	36	1.2V Analog Front End supply for Video ADC
VDDA33_AFE	V3	40	3.3V Analog Front End supply for Video ADC
VDD33_ LDOIN	T12	68	On-chip 2.5V LDO, 1.1V LDO and SNVS regulators input supply
VDDREG	P5	24	On-chip HPREG, LPREG, WBREG and ULPREG regulators input supply
VREFH_ADC	W1	34	ATD High Voltage Reference
VREFL_ADC	U3	33	ATD Low Voltage Reference

Table continues on the next page...

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_CLK_b[0]	B2	—	SDRAMC_VDD2P5	DDR	—	DDR_CLK_b[0]	—	—
DDR_CS_b[0]	C5	—	SDRAMC_VDD2P5	DDR	—	DDR_CS_b[0]	—	—
DDR_D[0]	F4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[0]	—	—
DDR_D[1]	H3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[1]	—	—
DDR_D[2]	D4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[2]	—	—
DDR_D[3]	G4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[3]	—	—
DDR_D[4]	F3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[4]	—	—
DDR_D[5]	J3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[5]	—	—
DDR_D[6]	C3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[6]	—	—
DDR_D[7]	G3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[7]	—	—
DDR_D[8]	J1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[8]	—	—
DDR_D[9]	D1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[9]	—	—
DDR_D[10]	H1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[10]	—	—
DDR_D[11]	E2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[11]	—	—
DDR_D[12]	G1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[12]	—	—
DDR_D[13]	C1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[13]	—	—
DDR_D[14]	H2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[14]	—	—
DDR_D[15]	D2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[15]	—	—
DDR_DQM[0]	J4	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[0]	—	—
DDR_DQM[1]	G2	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[1]	—	—
DDR_DQS[0]	D3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[0]	—	—

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_DQS_b[0]	E3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS_b[0]	—	—
DDR_DQS[1]	E1	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[1]	—	—
DDR_DQS_b[1]	F1	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS_b[1]	—	—
DDR_ODT[0]	C4	—	SDRAMC_VDD2P5	DDR	—	DDR_ODT[0]	—	—
DDR_ODT[1]	B1	—	SDRAMC_VDD2P5	DDR	—	DDR_ODT[1]	—	—
DDR_RAS_b	A4	—	SDRAMC_VDD2P5	DDR	—	DDR_RAS_b	—	—
DDR_RESET	D6	—	SDRAMC_VDD2P5	DDR	—	DDR_RESET	—	—
DDR_VREF	G5	—	SDRAMC_VDD2P5	DDR	—	DDR_VREF	—	—
DDR_WE_b	C6	—	SDRAMC_VDD2P5	DDR	—	DDR_WE_b	—	—
DDR_ZQ	A3	—	SDRAMC_VDD2P5	DDR	—	DDR_ZQ	—	—
EXT_POR	T1	23	VDD33	GPIO	—	EXT_POR	—	—
EXT_TAMPER0	T14	—	VBAT	Analog	—	EXT_TAMPER0	—	—
EXT_TAMPER1	U14	—	VBAT	Analog	—	EXT_TAMPER1	—	—
EXT_TAMPER2/ EXT_WM0_TAMPER_IN	T13	—	VBAT	Analog	—	EXT_TAMPER2/ EXT_WM0_TAMPER_IN	—	—
EXT_TAMPER3/ EXT_WM0_TAMPER_OUT	U13	—	VBAT	Analog	—	EXT_TAMPER3/ EXT_WM0_TAMPER_OUT	—	—
EXT_TAMPER4/ EXT_WM1_TAMPER_IN	U12	—	VBAT	Analog	—	EXT_TAMPER4/ EXT_WM1_TAMPER_IN	—	—
EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	U10	—	VBAT	Analog	—	EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	—	—

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Removed Temperature Voltage Monitor section to security RM • Updated VideoADC Specifications table
Rev 5	April 2013	Updated pin muxing table with the following changes: • Added MII0 including M AC0.TXDATA[2], MAC0.TXDATA[3], MAC0.RXDATA[2], MAC0.RXDATA[3] , MAC0.TXERR, MAC0.TXCLK, MAC0.RXCLK, MAC0.COL, MAC0.CRS • Following signals muxed on same RMII0 Pins : MII0_MDC, MII0_MDC, MII0_RXD[1], MII0_RXD[0], MII0_RXER, MII0_TXD[1], MII0_TXD[0], MII0_TXEN • Replaced FB_ALE with FB_MUXED_ALE, FB_CS4_b with FB_MUXED_TSIZ0, FB_TSIZ1 with FB_MUXED_TSIZ1, FB_TBST_b with FB_MUXED_TBST_b, FB_BE0_b with FB_MUXED_BE0_b • Removed RCON18,19,20 • Replaced ESAI_SDO2 with ESAI_SDO2/ESAI_SDI3 Replaced ESAI_SDO3 with ESAI_SDO3/ ESAI_SDI2 Replaced ESAI_SDI0 with ESAI_SDO5/ESAI_SDI0 Replaced ESAI_SDI1 with ESAU_SDO4/ESAI_SDI1 • CKO1 additionally muxed at PAD40
Rev 5	May 2013	In the Features, minor editorial updates Added Part Number Format figure Updated the Fields table as per the device part numbers Added Part Numbers table Added External NPN Ballast section In the LVD Dig Electrical Specs, minimum value of Upper Voltage Threshold and Lower Voltage threshold In the FlexBus timing specifications table, clarified the Frequency of operation In the Power consumption, filled TBDs. Updated footnotes

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		Rewritten the EMC radiated emissions operating behaviors table In the GPIO DC Electrical characteristics table: • Vhys test condition changed • Added R_Keeper row In the DDR operating conditions, changed the Vddi Min and Max values In the Power sequencing table, rremoved some rows In the Power Supply section, removed LVDS and removed the note In the Recommended operating conditions table, updated min and max of VDD12_AFE and FA_VDD. Updated Min, Max, and Typ for VDD Added the Recommended Connections for Unused Analog Interfaces table In the 12-bit ADC Characteristics table, updated the typ and max values of TUE, DNL. INL, ZSE, FSE Added Receive and Transmit signal timing specifications for MII interfaces In the DSPI table, clarified the TBDs In PLL 4, PLL 5, PLL 6 electrical characteristics tables, added footnotes In the JTAG electrical table, clarified the TBDs In the pinouts section, added Special Signal table Added Power Supply pins section Added Functional Assignment section
Rev 6	Jan 2014	• Added QuadSPI electricals • Changed VBB references to VBAT • In the feature list, clarified that ECC supported for 8-bit mode only, not 16-bit. • Revised the part number format • Revised the field table • Added Absolute Maximum Rating table, which was madde non_cust in the previous version • In the Power Consumption Operating Behavior table, Revised min and max value of IDD_LPS3 and IDD_LPS2. Removed IDD_LPS1 row

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