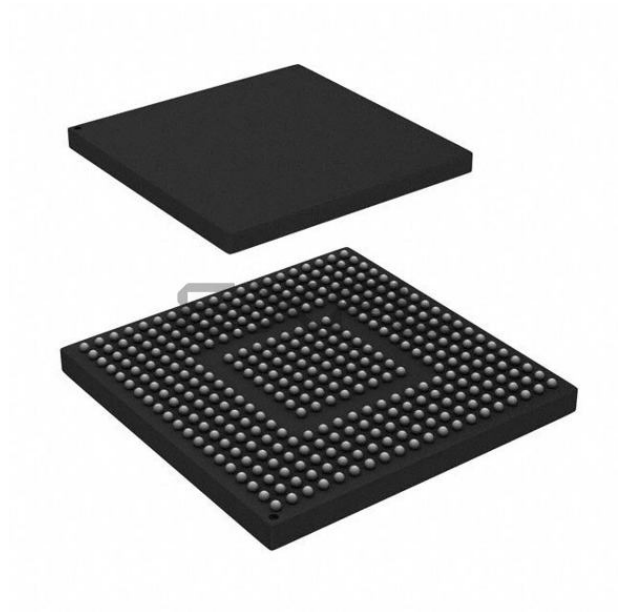

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5 + Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	400MHz, 133MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf522r2k1cmk4

- Display and Video
  - Dual Display Control Unit (DCU) with support for color TFT display up to WVGA
  - Segmented LCD (3V Glass only) configurable as 40x4, 38x8, and 36x6
  - Video Interface Unit (VIU) for camera
  - Open VG Graphics Processing Unit (GPU)
  - VideoADC
- Analog
  - Dual 12-bit SAR ADC with 1MS/s
  - Dual 12-bit DAC
- Audio
  - Four Synchronous Audio Interface (SAI)
  - Enhanced Serial Audio Interface (ESAI)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Asynchronous Sample Rate Converter (ASRC)
- Human-Machine Interface (HMI)
  - GPIO pins with interrupt support, DMA request capability, digital glitch filter.
  - Hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
- On-Chip Memory
  - 512 KB On-chip SRAM with ECC
  - 1 MB On-chip graphics SRAM (no ECC). This depends on the part selected. Alternate configuration could be 512 KB graphics and 512 KB L2 cache.
  - 96 KB Boot ROM

4 Handling ratings

4.1 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I_{LAT}	Latch-up Current at ambient temperature of 85 °C	-100	100	mA	

1. Determined according to the AEC spec AEC-Q100-002 for HBM
2. Determined according to AEC spec AEC-Q100-011

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2.1.5 External NPN Ballast

The internal main regulator requires an external NPN ballast transistor to be connected as shown in the following figure as well as an external capacitance to be connected to the device in order to provide a stable 1.2V digital supply to the device. The HPREG design allows for collector voltage lower than VDDREG value. See AN4807 at www.freescale.com .

NOTE

To not overload BCTRL output, collector voltage should appear no later than VDDREG / VDD33 (3.3V).

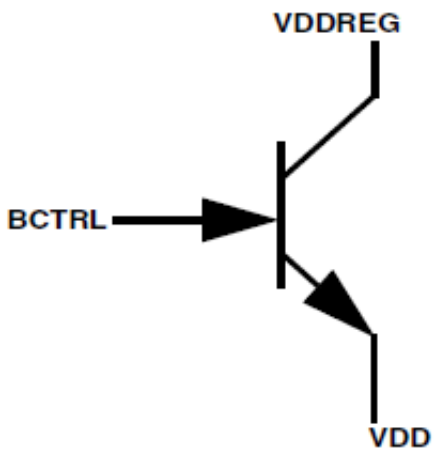

Figure 3. External NPN Ballast connections

Table 6. BCTRL OUTPUT specification

Parameter	Value	Comments
BCTRL OUTPUT specification	20mA	BCTRL driver can not drive more than 20mA current
Maximum pin voltage	VDDREG-0.5V	For Example, VDDREG =3.0V BCTRL should not exceed 2.5V.

Table 7. Assumptions For calculations

Parameter	Value
VDDREG	3.0V to 3.6V with typical value of 3.3V
Max DC Collector current	0.85A @85 °C
Emitter voltage	1.2V to 1.25V
Collector voltage	Equal to VDDREG

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV

6.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

6.2.8 Capacitance attributes

Table 18. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

7 I/O parameters

7.1 GPIO parameters

Table 19. GPIO DC operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi[1]	Core internal supply voltage		1.2		V
ovdd	I/O output supply voltage	3	3.3	3.6	V

1. This is internally controlled.

Table 20. GPIO DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voh	High-level output voltage	Ioh= -1mA	ovdd-0.15			V

Table continues on the next page...

Table 21. GPIO AC Electrical Characteristics (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Slew rate	Test conditions	Min	Max	Unit
tpr	IO Output Transition Times (PA1), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	1.70	1.81	ns
			fast		1.04	1.18	
		High 1 0 1	slow		2.30	2.44	
			fast		1.69	1.79	
		Medium 1 0 0	slow		3.07	3.31	
			fast		2.45	2.61	
		Low 0 1 1	slow		5.13	5.44	
			fast		4.79	5.18	
tpo	IO Output Propagation Delay (PA2), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	5.01	5.04	ns
			fast		3.06	3.10	
		High 1 0 1	slow		5.55	5.68	
			fast		3.52	3.55	
		Medium 1 0 0	slow		6.37	6.67	
			fast		4.04	4.11	
		Low 0 1 1	slow		7.39	7.60	
			fast		5.54	6.10	
tpv	Output Enable to Output Valid Delay, rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps, 0->1, 1->0 pad transitions	5.12	5.21	ns
			fast		3.18	3.28	
		High 1 0 1	slow		5.72	5.80	
			fast		3.67	3.71	
		Medium 1 0 0	slow		6.55	6.80	
			fast		4.06	4.09	
		Low 0 1 1	slow		7.80	8.19	
			fast		5.72	6.22	
tpi	Input Pad Propagation Delay rise/fall	without hysteresis	-	150f Cload on, input edge rate from pad =1.2ns	1.06	1.31	ns
		with hysteresis	-		1.22	1.41	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.1.1 Output Buffer Impedance measurement

Table 22. Output Buffer Average Impedance (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
Rdrv	Output driver impedance	0 0 1	116	150	220	Ohm
		0 1 0	58	75	110	
		0 1 1	39	50	73	

Table continues on the next page...

USB bus during standby. This supply can be turned-off during standby in applications that cannot tolerate the standby current and do not monitor the USB bus.

8.2 Power supply

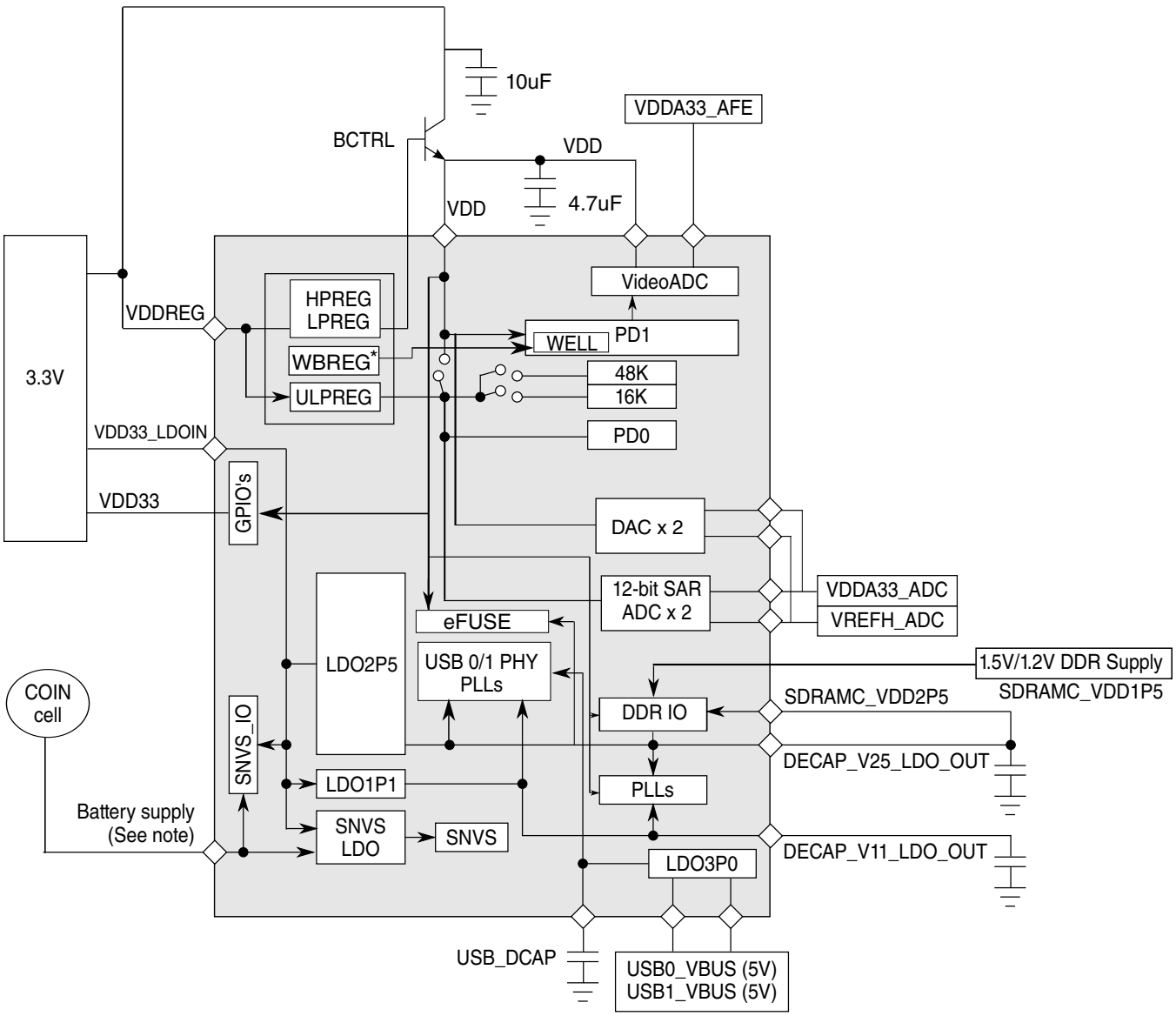

Figure 4. Power supply

NOTE

VBAT is the backup battery supply. If not required, then VBAT should be tied to VDDREG.

NOTE

WBREG is the Well Bias Regulator. Supplies PD1 WELL during well bias modes.

8.3 Absolute maximum ratings

NOTE

These are the values above which device can get damaged. Refer to the recommended operating conditions table for intended use case values

Table 29. Absolute maximum ratings

Symbol	Parameters	Min	Max	Unit
USB0_VBUS	VBUS supply for USB	-	5.25	V
USB1_VBUS	VBUS supply for USB	-	5.25	V
USB_DCAP	USB LDO 5V->3.3V Outpu	-0.3	3.6	V
VBAT	Battery supply in case of LDOIN fails	-0.3	3.6	V
VDD33_LDOIN	LDO input supply	-0.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	-0.3	1.3	V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR, EFUSE	-0.3	3.6	V
VDD33	GPIO 3.3V IO supply	-0.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	-0.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	-0.3	3.6	V
VREFH_ADC	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)	-0.3	1.3	V
FA_VDD	Test purpose only	-0.3	1.3	V
VDD	1.2V core supply	-0.3	1.3	V
SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	-0.3	1.975	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	-0.3	3.6	V

Table 30. Recommended operating conditions (continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VSSA33_AFE	Ground supply of AFE (Video ADC)			0		V
VSS12_AFE	Ground supply for AFE (Video ADC)			0		V
SDRAMC_VDD1P5	LPDDR2	External CAP 10uF	1.142	1.2	1.26	V
SDRAMC_VDD1P5	DDR3	External CAP 10uF	1.425	1.5	1.575	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	External CAP 10uF	2.25	2.5	2.75	V
-	Maximum power supply ramp rate (Slew limit for power-up)		-		0.1	V/us

1. For customer applications, this is governed by ballast output which is controlled by the device and appropriate voltage ranges are maintained.

8.5 Recommended Connections for Unused Analog Interfaces

NOTE

There are two options to handle unused power pins:

1. Connect all unused supplies to their respective voltage. To save the power, do not enable the module and/or do not enable clock gate to the module.
2. Keep all unused supplies floating.

If pin is shared by several peripheral, then all peripherals connected to multiplexer have to be powered. For example: if pin is shared by GPIO and ADC input and GPIO functionality is used, then ADC has to be powered due to internal structure of the multiplexer. Keep unused input signals grounded if power pins are powered. Keep unused input signals floating if power pins are floating. Keep unused output signals floating.

Module	Name	Recommendation if Unused
ADC	VDDA33_ADC	3.3V or float (Note: Powers both ADC and DAC)
	VREFH_ADC, VREFL_ADC	VREFH_ADC same as VDDA33_ADC VREFL_ADC ground or float
	ADC0SE8, ADC0SE9, ADC1SE8, ADC1SE9	Ground or float
CCM	LVDS0P, LVDS0N	Float
DAC	DACO0, DACO1	Float

Table continues on the next page...

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions	Symb	Min	Typ	Max	Unit	Comment
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
Total Unadjusted Error	12 bit mode	TUE	-2	-	+5	LSB	With Max Averaging
	10 bit mode		-0.5	-	+2		
	8 bit mode		-0.25	-	+1.5		
Differential Non-Linearity	12 bit mode	DNL	-	±0.6	±1.5	LSB[1]	Waiting for histogram method confirmation
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.5		
Integral Non-Linearity	12 bit mode	INL	-	±2	±4	LSB[1]	Waiting for histogram method confirmation
	10bit mode		-	±1	±2		
	8 bit mode		-	±0.5	±1		
Zero-Scale Error	12 bit mode	E_{ZS}	-	+1.0	±1.6	LSB[1]	VADIN = V_{REFL} With Max Averaging
	10bit mode		-	±0.4	±0.8		
	8 bit mode		-	±0.1	±0.4		
Full-Scale Error	12 bit mode	E_{FS}	-	±2	±3.5	LSB[1]	VADIN = V_{REFH} With Max Averaging
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.75		
Quantization Error	12 bit mode	E_Q	-	±1 to 0		LSB[1]	
	10bit mode		-	±0.5			
	8 bit mode		-	±0.5			
Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	-	Bits	Fin = 100Hz
Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	
Input Leakage Error	all modes	EIL	I_{In} x RAS			mV	I_{In} = 400 nA leakage current
Temp Sensor Slope	Across the full temperature range of the device	m	--	1.84	--	mV/°C	
Temp Sensor Voltage	25°C	V_{TEMP25}	-	696	-	mV	

1. 1 LSB = (V_{REFH} - V_{REFL})/2N

2. Intra bit skew is less than 2 ns
3. Load CL = 50 pf

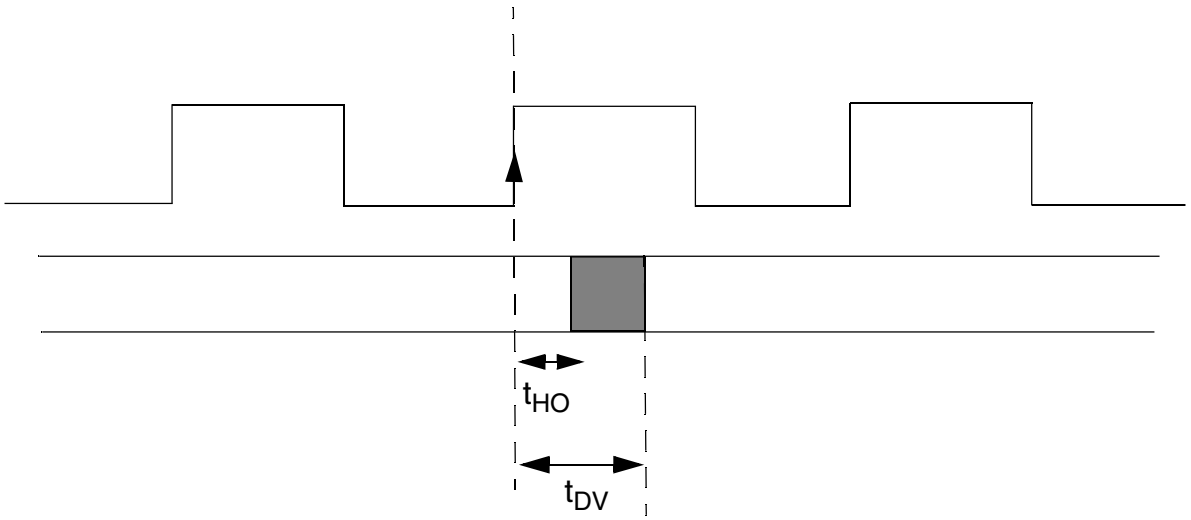

Figure 17. LCD Interface Timing Parameters—Access Level

9.2.2 Video Input Unit timing

This section provides the timing parameters of the Video Input Unit (VIU) interface.

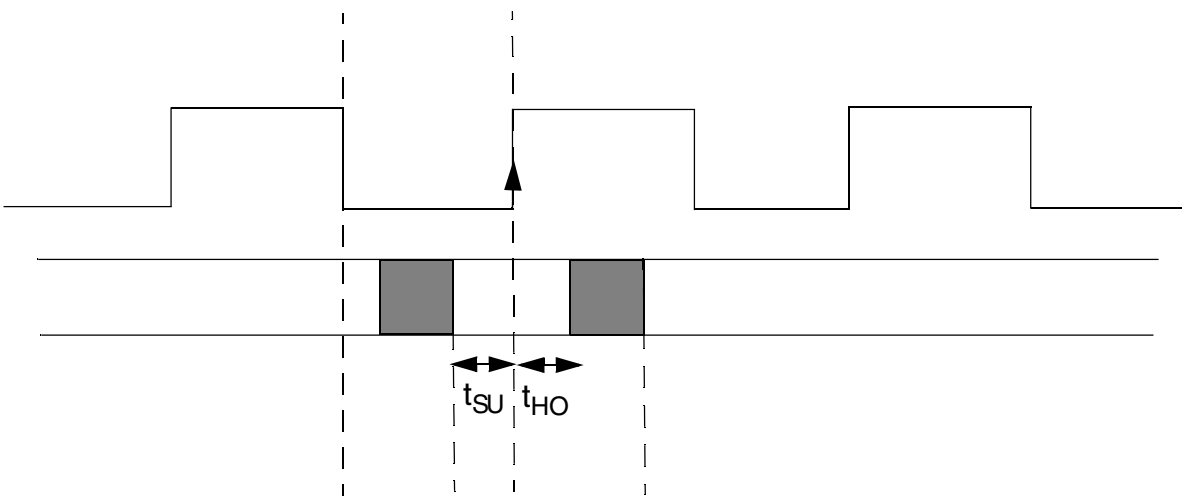

Figure 18. VIU Timing Parameters

Table 38. VIU Timing Parameters

Symbol	Characteristic	Min Value	Max Value	Unit
f_{PIX_CK}	VIU pixel clock frequency	_	64	MHz
t_{DSU}	VIU data setup time	4	_	ns
t_{DHD}	VIU data hold time	1	_	ns

Table 40. Receive signal timing for RMII interfaces (continued)

	Characteristic	RMII Mode		Unit
		Min	Max	
E4, E8	RMII_CLK pulse width low	35%	65%	RMII_CLK period
E1	RXD[1:0], CVS_DV, RXER to RMII_CLK setup	4	—	ns
E2	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
E6	RMII_CLK to TXD[1:0], TXEN valid	—	14	ns
E5	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

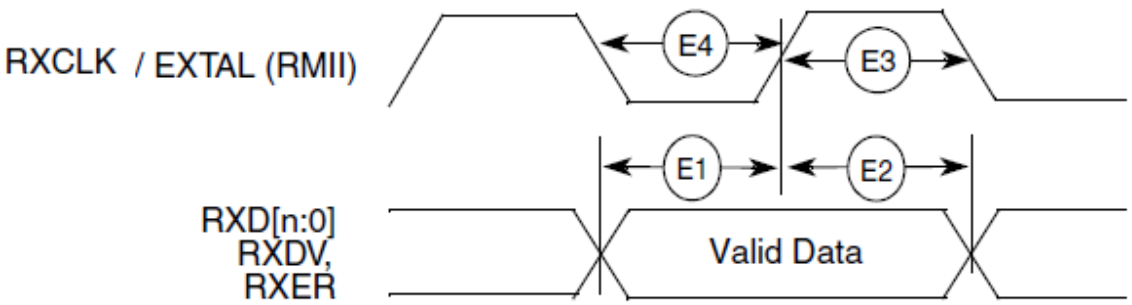

Figure 19. RMII receive signal timing diagram

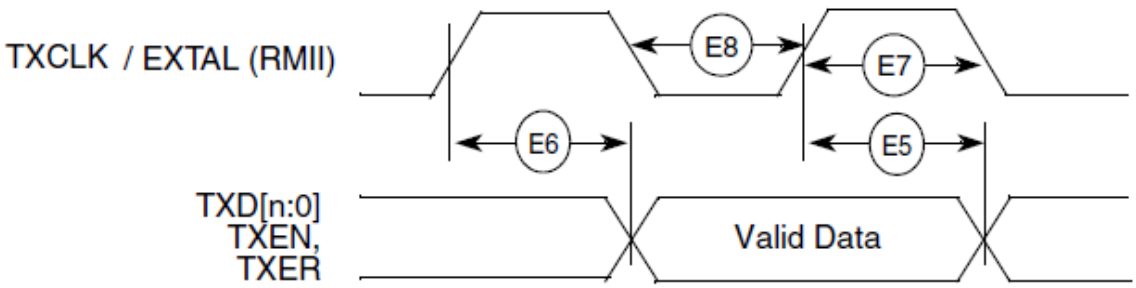

Figure 20. RMII transmit signal timing diagram

NOTE

See the most current device errata document when using the internally generated RXCLK and TXCLK clocks.

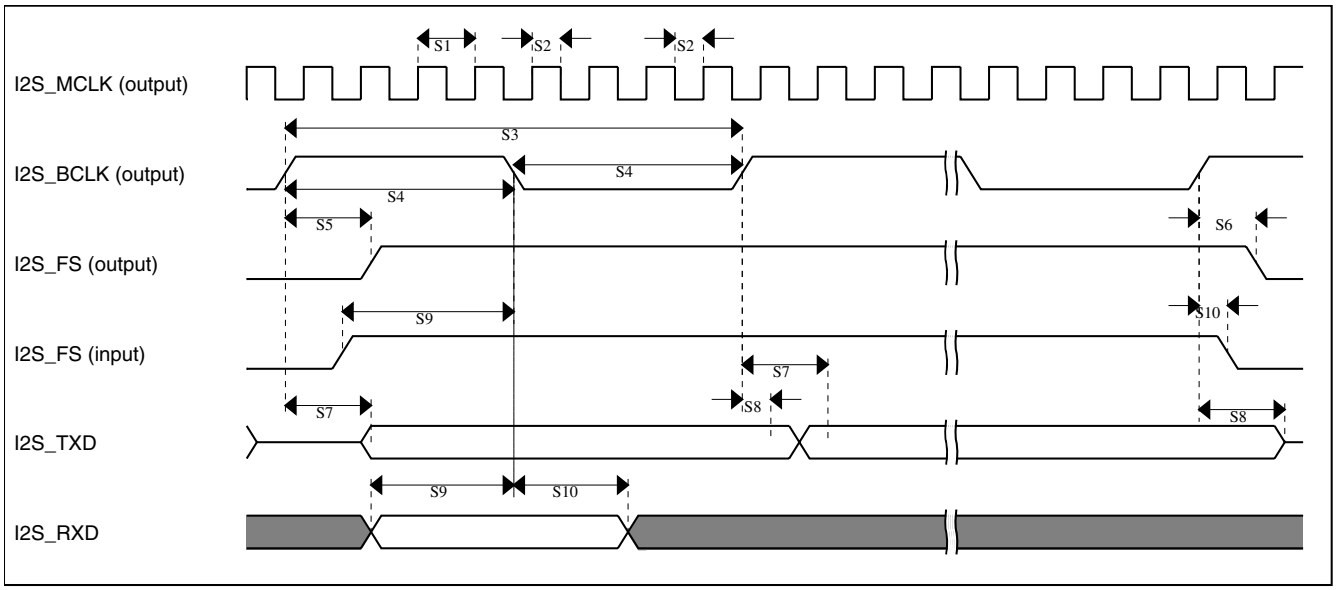

Figure 28. SAI Timing — Master Modes

Table 47. Slave Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{SYS}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FS input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

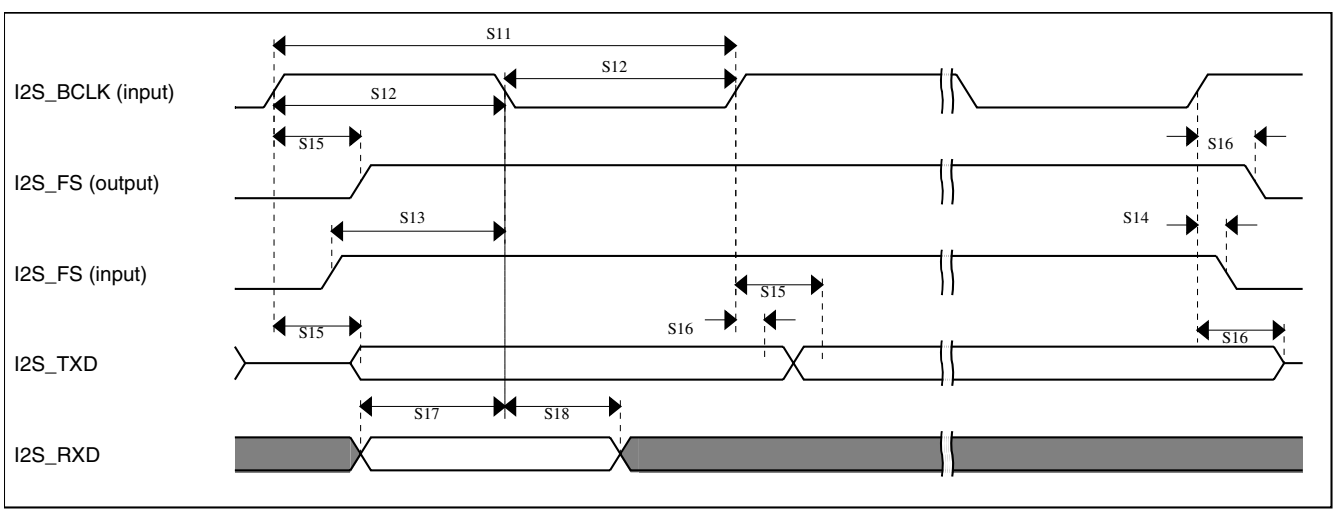

Figure 29. SAI Timing — Slave Modes

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.5 LPDDR2 Read Cycle

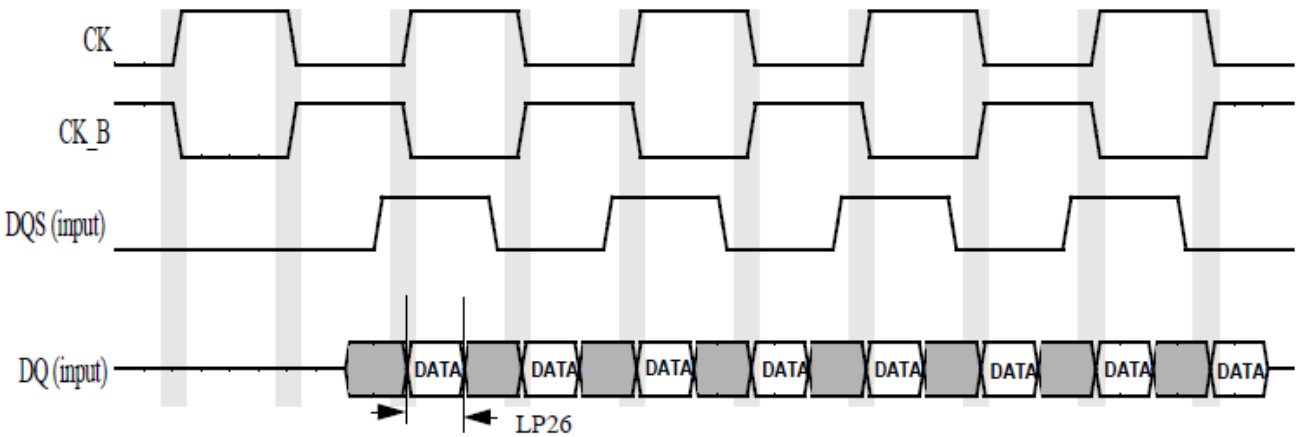

Figure 45. LPDDR2 Read cycle

Table 58. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	-	270	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

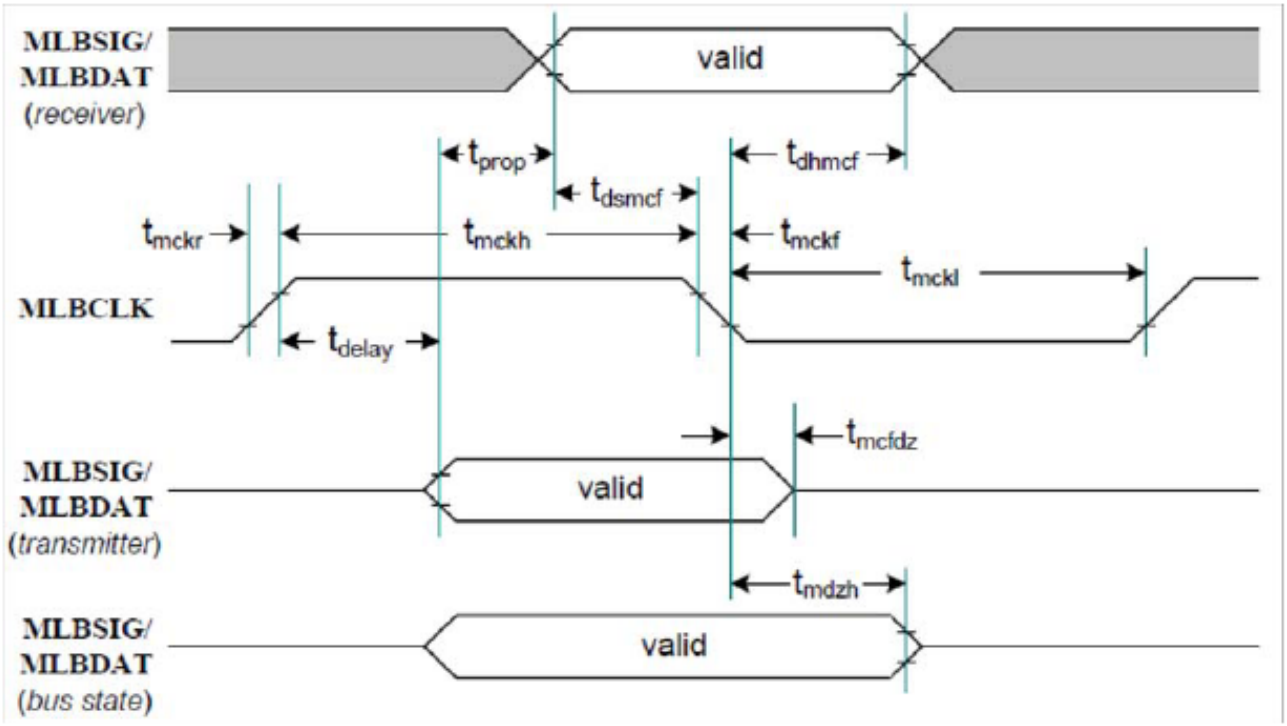

Figure 47. MediaLB 3-PinTiming

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 61. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
MLBCLK rise time	$t_{mck}r$	Refer Table 21		ns	$V_{IL\ to\ V_{IH}}$
MLBCLK fall time	$t_{mck}f$			ns	$V_{IH\ to\ V_{IL}}$
MLBCLK low time[1]	$t_{mck}l$	30, 14	—	ns	256xFs, 512xFs
MLBCLK high time	$t_{mck}h$	30, 14	—	ns	256xFs, 512xFs
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	3	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	2	—	ns	—
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	16	ns	2
Bus output hold from MLBCLK low	t_{mdzh}	2	—	ns	—

1. MLBCLK low/high time includes the pluse width variation.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G20	124	PTD23		PTD23/ MII0_ RXDATA[3]	FB_AD23	NF_IO7	FTM2CH0	ENET0_ 1588_TMR0	SDHC0_ DAT4	SCI2_TX	DCU1_R3	
F20	126	PTD22		PTD22/ MII0_ RXDATA[2]	FB_AD22	NF_IO6	FTM2CH1	ENET0_ 1588_TMR1	SDHC0_ DAT5	SCI2_RX	DCU1_R4	
F19	128	PTD21		PTD21/ MII0_CRS	FB_AD21	NF_IO5		ENET0_ 1588_TMR2	SDHC0_ DAT6	SCI2_RTS	DCU1_R5	
F17	129	PTD20		PTD20/ MII0_COL	FB_AD20	NF_IO4		ENET0_ 1588_TMR3	SDHC0_ DAT7	SCI2_CTS	DCU1_R0	
F16	130	PTD19		PTD19	FB_AD19	NF_IO3	ESAI_SCKR	I2C0_SCL	FTM2_QD_ PHA	MII0_ TXDATA[3]	DCU1_R1	
E18	131	PTD18		PTD18	FB_AD18	NF_IO2	ESAI_FSR	I2C0_SDA	FTM2_QD_ PHB	MII0_ TXDATA[2]	DCU1_G0	
E20	132	PTD17		PTD17	FB_AD17	NF_IO1	ESAI_HCKR	I2C1_SCL		MII0_TXERR	DCU1_G1	
D20	133	PTD16		PTD16	FB_AD16	NF_IO0	ESAI_HCKT	I2C1_SDA			DCU1_G2	
Y17	86	PTD0		PTD0	QSPI0_A_ SCK	SCI2_TX		FB_AD15	SPDIF_ EXTCLK			
Y18	87	PTD1		PTD1	QSPI0_A_ CS0	SCI2_RX		FB_AD14	SPDIF_IN1			
V18	88	PTD2		PTD2	QSPI0_A_ DATA3	SCI2_RTS	SPI1_PCS3	FB_AD13	SPDIF_OUT1			
Y19	89	PTD3		PTD3	QSPI0_A_ DATA2	SCI2_CTS	SPI1_PCS2	FB_AD12	SPDIF_ PLOCK			
W19	90	PTD4		PTD4	QSPI0_A_ DATA1		SPI1_PCS1	FB_AD11	SPDIF_ SRCLK			
W20	91	PTD5		PTD5	QSPI0_A_ DATA0		SPI1_PCS0	FB_AD10				
V20	92	PTD6		PTD6	QSPI0_A_ DQS		SPI1_SIN	FB_AD9				
V19	93	PTD7		PTD7	QSPI0_B_ SCK		SPI1_SOUT	FB_AD8				
U17	94	PTD8		PTD8	QSPI0_B_ CS0	FB_CLKOUT	SPI1_SCK	FB_AD7				
U18	97	PTD9		PTD9	QSPI0_B_ DATA3	SPI3_PCS1		FB_AD6		SAI1_TX_ SYNC	DCU1_B0	
U20	98	PTD10		PTD10	QSPI0_B_ DATA2	SPI3_PCS0		FB_AD5			DCU1_B1	
T20	99	PTD11		PTD11	QSPI0_B_ DATA1	SPI3_SIN		FB_AD4				
T19	100	PTD12		PTD12	QSPI0_B_ DATA0	SPI3_SOUT		FB_AD3				
T18	101	PTD13		PTD13	QSPI0_B_ DQS	SPI3_SCK		FB_AD2				
A19	141	PTB23		PTB23	SAI0_TX_ BCLK	SCI1_TX		FB_MUXED_ ALE	FB_TS_b	SCI3_RTS	DCU1_G3	

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[1]	PORT0[1]	PTA8	IOMUXC_PTA8	40048004
RGPIO[2]	PORT0[2]	PTA9	IOMUXC_PTA9	40048008
RGPIO[3]	PORT0[3]	PTA10	IOMUXC_PTA10	4004800C
RGPIO[4]	PORT0[4]	PTA11	IOMUXC_PTA11	40048010
RGPIO[5]	PORT0[5]	PTA12	IOMUXC_PTA12	40048014
RGPIO[6]	PORT0[6]	PTA16	IOMUXC_PTA16	40048018
RGPIO[7]	PORT0[7]	PTA17	IOMUXC_PTA17	4004801C
RGPIO[8]	PORT0[8]	PTA18	IOMUXC_PTA18	40048020
RGPIO[9]	PORT0[9]	PTA19	IOMUXC_PTA19	40048024
RGPIO[10]	PORT0[10]	PTA20	IOMUXC_PTA20	40048028
RGPIO[11]	PORT0[11]	PTA21	IOMUXC_PTA21	4004802C
RGPIO[12]	PORT0[12]	PTA22	IOMUXC_PTA22	40048030
RGPIO[13]	PORT0[13]	PTA23	IOMUXC_PTA23	40048034
RGPIO[14]	PORT0[14]	PTA24	IOMUXC_PTA24	40048038
RGPIO[15]	PORT0[15]	PTA25	IOMUXC_PTA25	4004803C
RGPIO[16]	PORT0[16]	PTA26	IOMUXC_PTA26	40048040
RGPIO[17]	PORT0[17]	PTA27	IOMUXC_PTA27	40048044
RGPIO[18]	PORT0[18]	PTA28	IOMUXC_PTA28	40048048
RGPIO[19]	PORT0[19]	PTA29	IOMUXC_PTA29	4004804C
RGPIO[20]	PORT0[20]	PTA30	IOMUXC_PTA30	40048050
RGPIO[21]	PORT0[21]	PTA31	IOMUXC_PTA31	40048054
RGPIO[22]	PORT0[22]	PTB0	IOMUXC_PTB0	40048058
RGPIO[23]	PORT0[23]	PTB1	IOMUXC_PTB1	4004805C
RGPIO[24]	PORT0[24]	PTB2	IOMUXC_PTB2	40048060
RGPIO[25]	PORT0[25]	PTB3	IOMUXC_PTB3	40048064
RGPIO[26]	PORT0[26]	PTB4	IOMUXC_PTB4	40048068
RGPIO[27]	PORT0[27]	PTB5	IOMUXC_PTB5	4004806C
RGPIO[28]	PORT0[28]	PTB6	IOMUXC_PTB6	40048070
RGPIO[29]	PORT0[29]	PTB7	IOMUXC_PTB7	40048074
RGPIO[30]	PORT0[30]	PTB8	IOMUXC_PTB8	40048078
RGPIO[31]	PORT0[31]	PTB9	IOMUXC_PTB9	4004807C
RGPIO[32]	PORT1[0]	PTB10	IOMUXC_PTB10	40048080
RGPIO[33]	PORT1[1]	PTB11	IOMUXC_PTB11	40048084
RGPIO[34]	PORT1[2]	PTB12	IOMUXC_PTB12	40048088
RGPIO[35]	PORT1[3]	PTB13	IOMUXC_PTB13	4004808C
RGPIO[36]	PORT1[4]	PTB14	IOMUXC_PTB14	40048090
RGPIO[37]	PORT1[5]	PTB15	IOMUXC_PTB15	40048094
RGPIO[38]	PORT1[6]	PTB16	IOMUXC_PTB16	40048098
RGPIO[39]	PORT1[7]	PTB17	IOMUXC_PTB17	4004809C

Table continues on the next page...

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[79]	PORT2[15]	PTD0	IOMUXC_PTD0	4004813C
RGPIO[80]	PORT2[16]	PTD1	IOMUXC_PTD1	40048140
RGPIO[81]	PORT2[17]	PTD2	IOMUXC_PTD2	40048144
RGPIO[82]	PORT2[18]	PTD3	IOMUXC_PTD3	40048148
RGPIO[83]	PORT2[19]	PTD4	IOMUXC_PTD4	4004814C
RGPIO[84]	PORT2[20]	PTD5	IOMUXC_PTD5	40048150
RGPIO[85]	PORT2[21]	PTD6	IOMUXC_PTD6	40048154
RGPIO[86]	PORT2[22]	PTD7	IOMUXC_PTD7	40048158
RGPIO[87]	PORT2[23]	PTD8	IOMUXC_PTD8	4004815C
RGPIO[88]	PORT2[24]	PTD9	IOMUXC_PTD9	40048160
RGPIO[89]	PORT2[25]	PTD10	IOMUXC_PTD10	40048164
RGPIO[90]	PORT2[26]	PTD11	IOMUXC_PTD11	40048168
RGPIO[91]	PORT2[27]	PTD12	IOMUXC_PTD12	4004816C
RGPIO[92]	PORT2[28]	PTD13	IOMUXC_PTD13	40048170
RGPIO[93]	PORT2[29]	PTB23	IOMUXC_PTB23	40048174
RGPIO[94]	PORT2[30]	PTB24	IOMUXC_PTB24	40048178
RGPIO[95]	PORT2[31]	PTB25	IOMUXC_PTB25	4004817C
RGPIO[96]	PORT3[0]	PTB26	IOMUXC_PTB26	40048180
RGPIO[97]	PORT3[1]	PTB27	IOMUXC_PTB27	40048184
RGPIO[98]	PORT3[2]	PTB28	IOMUXC_PTB28	40048188
RGPIO[99]	PORT3[3]	PTC26	IOMUXC_PTC26	4004818C
RGPIO[100]	PORT3[4]	PTC27	IOMUXC_PTC27	40048190
RGPIO[101]	PORT3[5]	PTC28	IOMUXC_PTC28	40048194
RGPIO[102]	PORT3[6]	PTC29	IOMUXC_PTC29	40048198
RGPIO[103]	PORT3[7]	PTC30	IOMUXC_PTC30	4004819C
RGPIO[104]	PORT3[8]	PTC31	IOMUXC_PTC31	400481A0
RGPIO[105]	PORT3[9]	PTE0	IOMUXC_PTE0	400481A4
RGPIO[106]	PORT3[10]	PTE1	IOMUXC_PTE1	400481A8
RGPIO[107]	PORT3[11]	PTE2	IOMUXC_PTE2	400481AC
RGPIO[108]	PORT3[12]	PTE3	IOMUXC_PTE3	400481B0
RGPIO[109]	PORT3[13]	PTE4	IOMUXC_PTE4	400481B4
RGPIO[110]	PORT3[14]	PTE5	IOMUXC_PTE5	400481B8
RGPIO[111]	PORT3[15]	PTE6	IOMUXC_PTE6	400481BC
RGPIO[112]	PORT3[16]	PTE7	IOMUXC_PTE7	400481C0
RGPIO[113]	PORT3[17]	PTE8	IOMUXC_PTE8	400481C4
RGPIO[114]	PORT3[18]	PTE9	IOMUXC_PTE9	400481C8
RGPIO[115]	PORT3[19]	PTE10	IOMUXC_PTE10	400481CC
RGPIO[116]	PORT3[20]	PTE11	IOMUXC_PTE11	400481D0
RGPIO[117]	PORT3[21]	PTE12	IOMUXC_PTE12	400481D4

Table continues on the next page...

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
EXTAL	Y13	73	DECAP_V11_LDO_OUT	Analog	—	EXTAL	—	—
EXTAL32	Y12	70	DECAP_V11_LDO_OUT	Analog	—	EXTAL32	—	—
JTCLK/ SWCLK	K4	3	VDD33	GPIO	ALT1	JTAG	Input	100K PU
JTDI	K2	4	VDD33	GPIO	ALT1	JTAG	Input	100K PU
JTDO	K1	5	VDD33	GPIO	ALT1	JTAG	Disabled	—
JTMS/ SWDIO	L1	6	VDD33	GPIO	ALT1	JTAG	Input	100K PU
LVDS0P	W14	—	DECAP_V25_LDO_OUT	Analog	—	LVDS0P	—	—
LVDS0N	Y14	—	DECAP_V25_LDO_OUT	Analog	—	LVDS0N	—	—
PTA6	N5	19	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA7	V15	75	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA12	L3	7	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA16	Y5	43	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA17	Y6	44	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA18	V6	46	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA19	U6	47	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA20	B18	143	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA21	D18	145	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA22	E17	147	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA23	C17	148	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA24	R16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA25	R17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA26	R19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA27	R20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA28	P20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA29	P18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA30	P17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA31	P16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB0	T6	49	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB1	T7	50	VDD33	GPIO	ALT3	RCON30	Input	Disabled
PTB2	V7	51	VDD33	GPIO	ALT3	RCON31	Input	Disabled

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		Added WBREG specifications Updated Recommended operating conditions table Updated DAC INL and DNL charts Updated Pinouts
Rev 5	April 2013	• Removed references to VF1xxR and refernces to F100 and 144 LQFP and 256 MAPBGA • Replaced references to Auto and IMM by R-series and F-series respectively • In the feature list, the ARM Core frequency changed to 500 MHz for F-series • In the feature list, changed the DRAM controller frequency • Updated Part Nummbering format • Clarified the Fields table as per Marketing • Sample numbers updated • From the VREG electrical specifications tables, deleted pre-trimming rows and comments • .In the HPREG electrical characteristics table, add footnote on maximum Output Current Capacity • In the ULPREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the WBREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the LVD electrical specifications table, added typ. values of Upper voltage threshold (value @27oC) and Lower voltage threshold (value @27oC) • In the LVD DIG electrical specifications table, removed pretrimming values and clarified other values • Updated LVD DIG electrical specifications values • Updated LDO_1P1 tables • Updated LDO_2P5 table • Updated Power consumption operating behaviors tables • Updated Absolute maximum ratings table

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• In the USB PHY Current Consumption table, removed the Normal Mode • In the Power Sequence table, revised the Power UP/ Down Order column for USB0_VBUs and USB1_VBUS • In the Recommended operating conditions table, revised the min value of VBAT. Revised the min value of VREFH_ADC Revised the min and max values of SDRAMC_VDD1P5 • In the Recommended Connections for Unused Analog Interfaces section, added the notes. Revised the Recommendation if Unused column • In the 12-bit ADC operating conditions, revised Conditions for Ground voltage. Revised min Ref High Voltage • In the 12-bit DAC operating requirements, revised the min and max value of VREFH_ADC • In the SDHC switching specifications, revised the max value of SD6 • In the 24MHz external oscillator electrical characteristics table, revised the min value of VIH and max value of VIL
Rev 7	November 2014	• Updated list of security features on page 1. • In "Part number format" figure, updated explanation for '1'. • In "Fields" table, updated definition of 'R'. • In "Part Numbers" table, added parts SVF331R3K1CKU2, SVF531R3K1CMK4, and SVF532R2K1CMK4. • In "External NPN ballast" section, updated recommendations for transistor selection. • In "DDR parameters" section, updated table footnotes regarding typical condition. • In "Power sequencing" table, added comment regarding SDRAMC_VDD1P5: "In case the Ballast transistor's collector is connected to the 1.5 V DRAM supply (instead of the 3.3 V