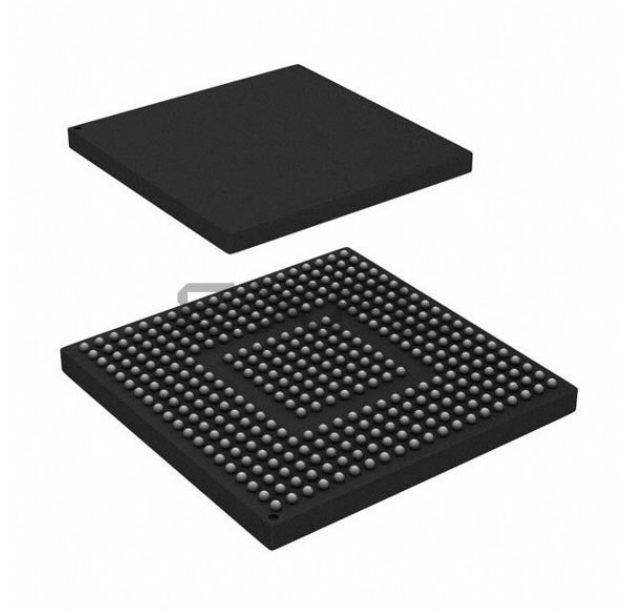

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5 + Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	400MHz, 133MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf522r2k2cmk4

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web.

1. To determine the orderable part numbers for this device, go to www.freescale.com and search the required part number. The part numbering format is described in the section that follows.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Part Number Format

The figure below represents the format of part number of this device.

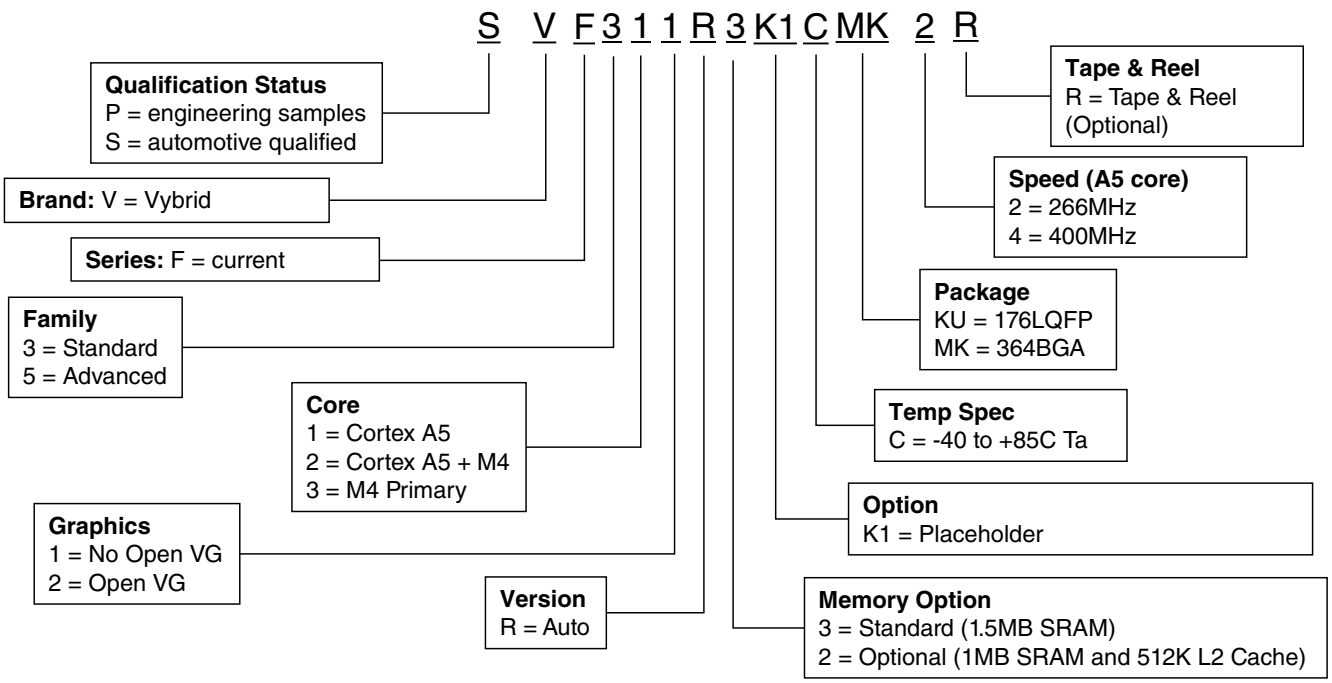


Figure 1. Part Number Format

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• P = engineering samples • S = automotive qualified
B	Brand	• V = Vybrid
S	Series	• F = current
F	Family	• 3 = Standard • 5 = Advanced
C	Core	• 1 = Cortex A5 • 2 = Cortex A5 + M4 • 3 = M4 Primary
G	Graphics	• 1 = No Open VG • 2 = OpenVG
V	Version	• R = Auto

Table continues on the next page...

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

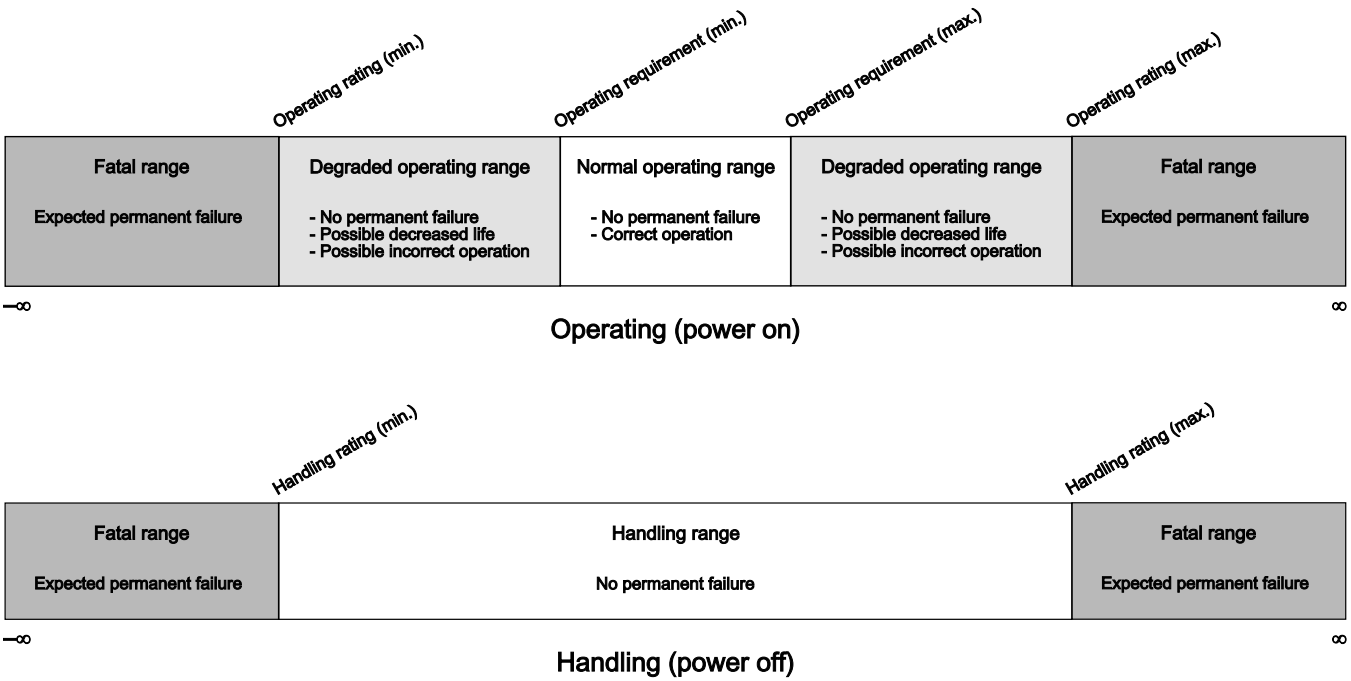
This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 3. LPREG electrical characteristics (continued)

Parameters	Min	Typ	Max	Unit	Comments
PSRR with 4.7uF output cap					
@ DC @noload			-40	dB	
@ DC @full load			-35		
Worst case @ any frequency			-12		

6.2.1.3 ULPREG electrical characteristics

Table 4. ULPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	1.88	2.3	2.86	µA	@ no load
	-	610	670	µA	@ full load
Output current capacity			20	mA	DC load current
Output voltage @ no load			1.175	V	
Output voltage @ full load	1.125			V	
PSRR with 500 pF output cap	-20			dB	Worst case at any frequency across corners
@ DC @noload			-50	dB	
@200KHz @noload			-37		
@ DC @full load			-42		
@200KHz @full load			-37		
Worst case @ any frequency @ any load			-15		

6.2.1.4 WBREG electrical characteristics

Table 5. WBREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3	3.3	3.6	V	-
Current Consumption	-	2	5	µA	@ no load
	-	2	5	µA	@ full load
Output current capacity	-	1	2	mA	DC load current
Output voltage @ no load		1.4	1.425	V	
Output voltage @ full load	1.375	1.398		V	
Output voltage programmability	1.4	1.4	1.7	V	16 steps of 25 mV each

6.2.3.3 LDO_3P0

Table 14. LDO_3P0 parameters

Specification	Min	Typ	Max	Unit	Comments
Input OTG VBUS Supply	4.4		5.25	V	
Input HOST VBUS Supply	4.4		5.25	V	
VDD3P0_OUT	2.9	3.0	3.1	V	Regulator output at default setting
I_out	-		50	mA	500 mV drop-out voltage
Regulator output programming range	2.625		3.4	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.75	2.85		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

NOTE

These values are with Anadig_REG_3P0[ENABLE_ILIMIT]= 0 and Anadig_REG_3P0[ENABLE_LINREG]= 1. It is required to set these values before using USB.

6.2.4 Power consumption operating behaviors

Table 15. Power consumption operating behaviors

Symbol	Description	Typ.[1]	Max.[2]	Unit	Notes
I_{DD_RUN}	Run mode current — All functionalities of the chip available	400	850	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.3 V ± 10%	80	500	mA	3
I_{DD_LPRUN}	Low-power run mode current at 3.3 V ± 10%, 24MHz operation, PLL Bypass.	13	325	mA	4
I_{DD_ULPRUN}	Ultra-low-power run mode current at 3.3 V ± 10%	12	395	mA	5
I_{DD_STOP}	Stop mode current at 3.3 V ± 10%	7	300	mA	6
I_{DD_LPS3}	Low-power stop3 mode current at 3.3 V ± 10%	300	1300	uA	7
I_{DD_LPS2}	Low-power stop 2 mode current at 3.3 V ± 10%	50	875	uA	8
I_{DD_VBAT}	Battery backup mode	5	45	uA	9

1. The Typ numbers represent the average value taken from a matrix lot of parts across normal process variation at ambient temperature.

8.4 Recommended operating conditions

Table 30. Recommended operating conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
USB0_VBUS	VBUS supply for USB w.r.t USB0_GND		4.4	5	5.25	V
USB1_VBUS	VBUS supply for USB w.r.t USB1_GND		4.4	5	5.25	V
USB_DCAP	USB LDO 5V->3 V Output	External DCAP (10uF termination for USBREG)		3		V
VBAT	Battery supply in case of LDOIN fails	External CAP 0.1uF	2.4	3.3	3.6	V
VDD33_LDOIN	LDO input supply		3	3.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	Recommended External DCAP: 1uF(Min) 10uF (Max)		1.1		V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR pre-driver, EFUSE	Recommended External DCAP: 1uF(Min) 10uF (Max)		2.5		V
VDD33	GPIO 3.3V IO supply	External CAP (10uF)	3	3.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	External CAP (10uF)	3	3.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	External CAP (10uF)	3	3.3	3.6	V
VREFH_ADC	High reference voltage for ADC and DAC	Relation with VDDDA33_ADC (1uF)	2.5	3.3	VDDA33_ADC	V
VREFL_ADC	Low reference voltage for ADC and DAC	External CAP (10uF)		0		V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	External CAP 10uF	3	3.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)		1.16	1.23	1.26	V
FA_VDD	For testing purpose only should be shorted to VDD on board.		1.16	1.23	1.26	V
VDD[1]	1.2V core supply	4.7uF with a low ESR value (100 milliohms)	1.16	1.23	1.26	V
USB0_GND	Ground supply for USB			0		V
USB1_GND	Ground supply for USB			0		V
VSS_KEL0	USB LDO ground output			0		V
VSS	VSS ground			0		V
VSSA33_ADC	Ground supply for ADC, DAC and IO segment			0		V

Table continues on the next page...

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions	Symb	Min	Typ	Max	Unit	Comment
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
Total Unadjusted Error	12 bit mode	TUE	-2	-	+5	LSB	With Max Averaging
	10 bit mode		-0.5	-	+2		
	8 bit mode		-0.25	-	+1.5		
Differential Non-Linearity	12 bit mode	DNL	-	±0.6	±1.5	LSB[1]	Waiting for histogram method confirmation
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.5		
Integral Non-Linearity	12 bit mode	INL	-	±2	±4	LSB[1]	Waiting for histogram method confirmation
	10bit mode		-	±1	±2		
	8 bit mode		-	±0.5	±1		
Zero-Scale Error	12 bit mode	E_{ZS}	-	+1.0	±1.6	LSB[1]	VADIN = V_{REFL} With Max Averaging
	10bit mode		-	±0.4	±0.8		
	8 bit mode		-	±0.1	±0.4		
Full-Scale Error	12 bit mode	E_{FS}	-	±2	±3.5	LSB[1]	VADIN = V_{REFH} With Max Averaging
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.75		
Quantization Error	12 bit mode	E_Q	-	±1 to 0		LSB[1]	
	10bit mode		-	±0.5			
	8 bit mode		-	±0.5			
Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	-	Bits	Fin = 100Hz
Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	
Input Leakage Error	all modes	EIL	I_{In} x RAS			mV	I_{In} = 400 nA leakage current
Temp Sensor Slope	Across the full temperature range of the device	m	--	1.84	--	mV/°C	
Temp Sensor Voltage	25°C	V_{TEMP25}	-	696	-	mV	

1. 1 LSB = (V_{REFH} - V_{REFL})/2N

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

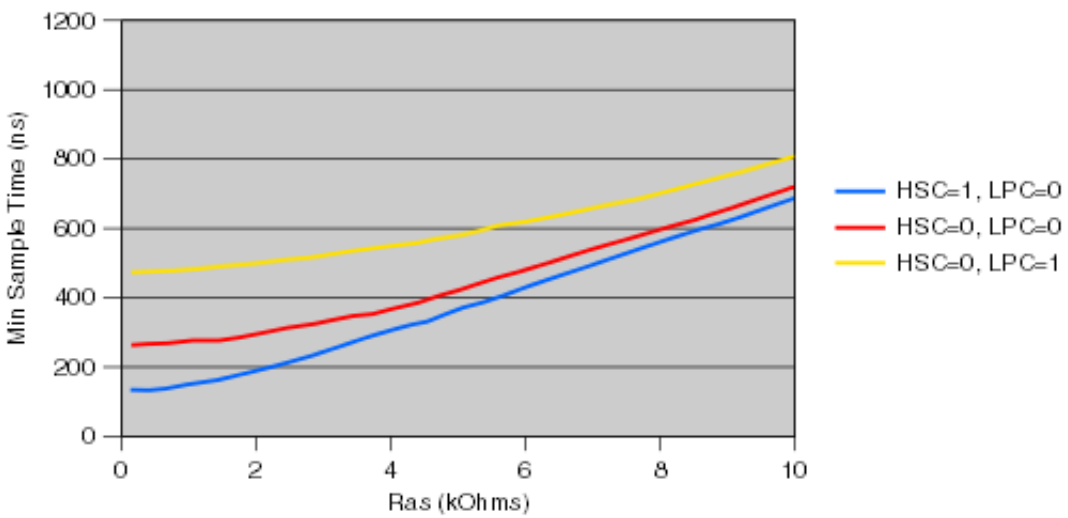


Figure 6. Minimum Sample Time Vs Ras (Cas = 2pF)

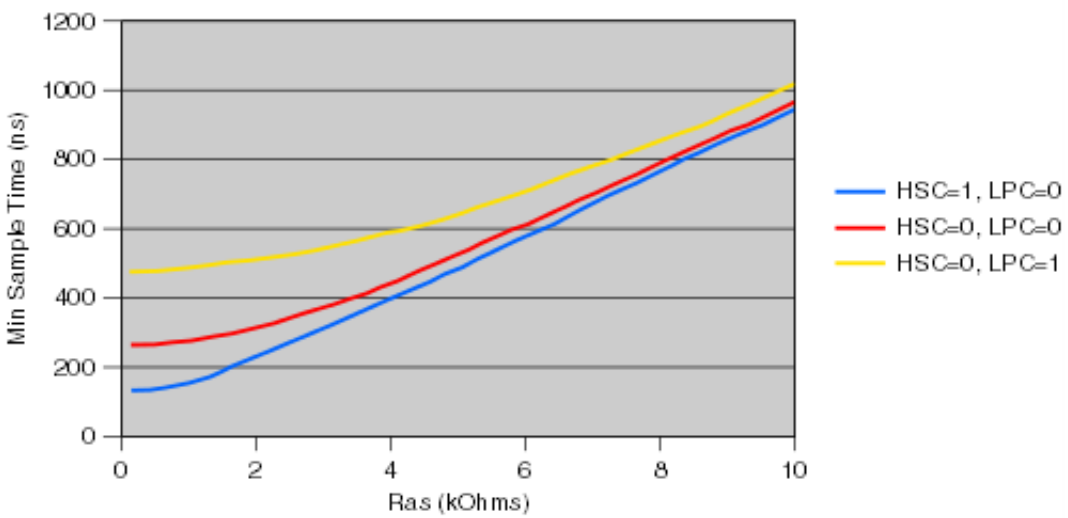


Figure 7. Minimum Sample Time Vs Ras (Cas = 5pF)

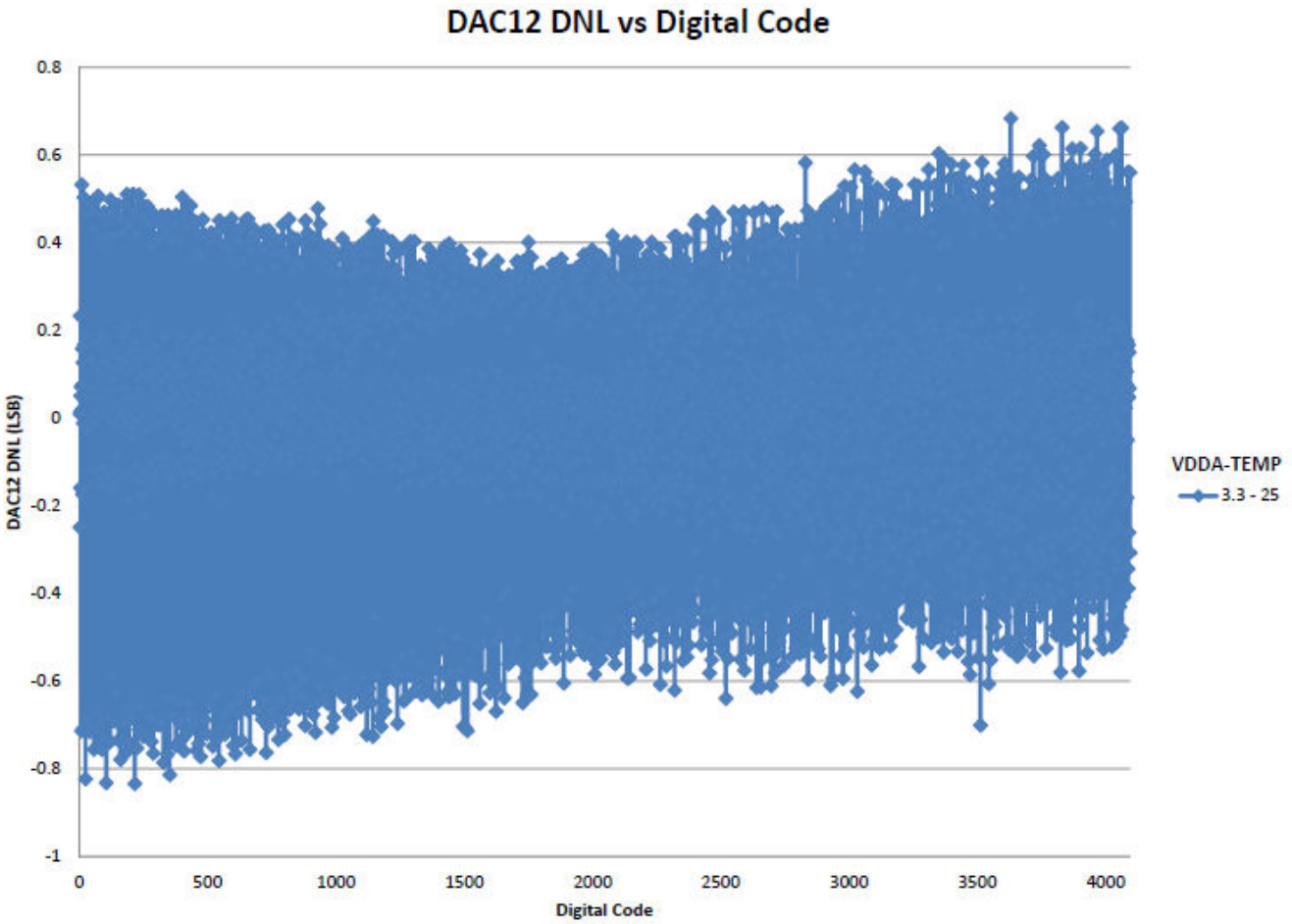


Figure 10. DNL error vs. digital code

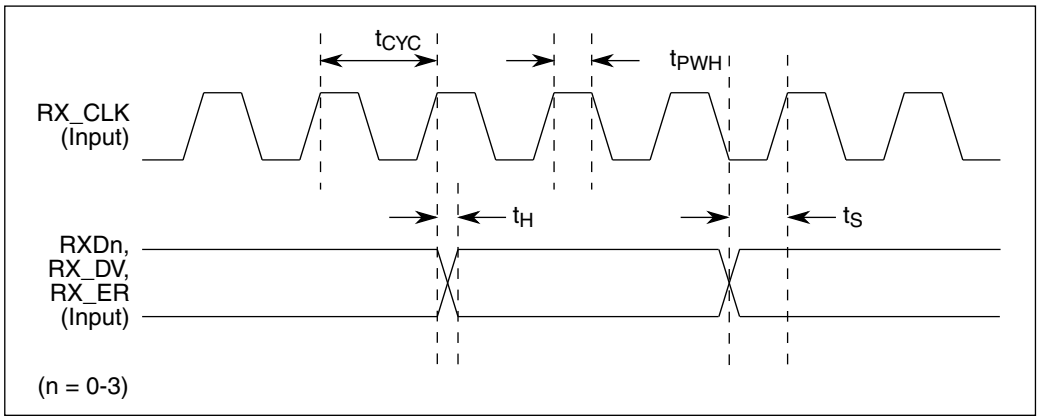


Figure 21. MII receive signal timing diagram

Table 41. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_S	5			ns
Input setup time after RX_CLK	t_H	5			ns

9.3.3 Receive and Transmit signal timing specifications for MII interfaces

This section provides timing specs that meet the requirements for MII interfaces for a range of transceiver devices.

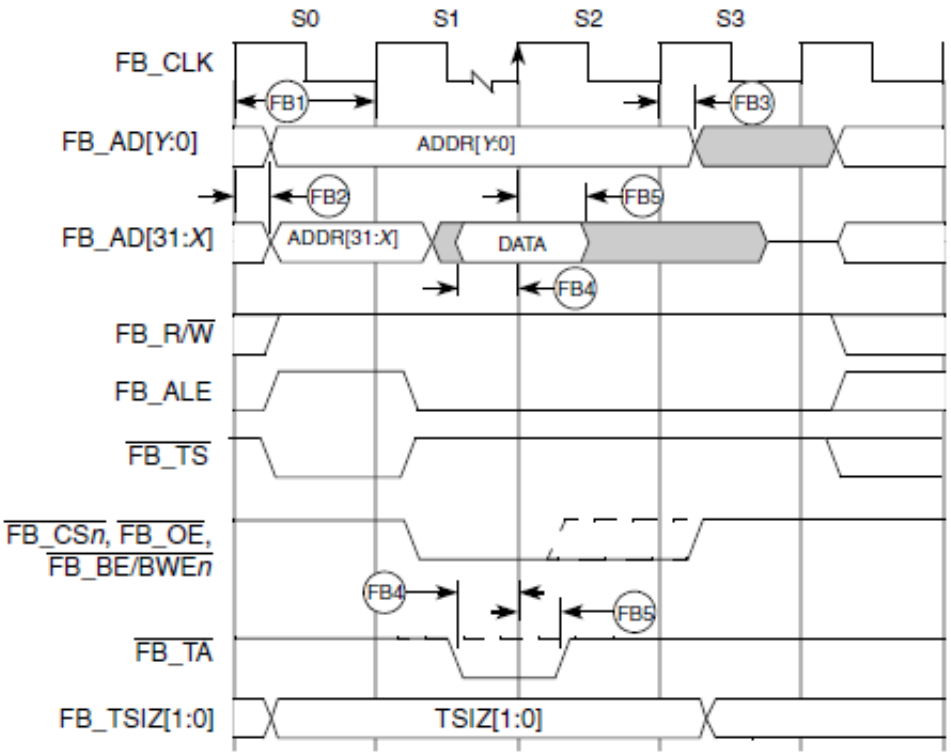


Figure 39. FlexBus read timing

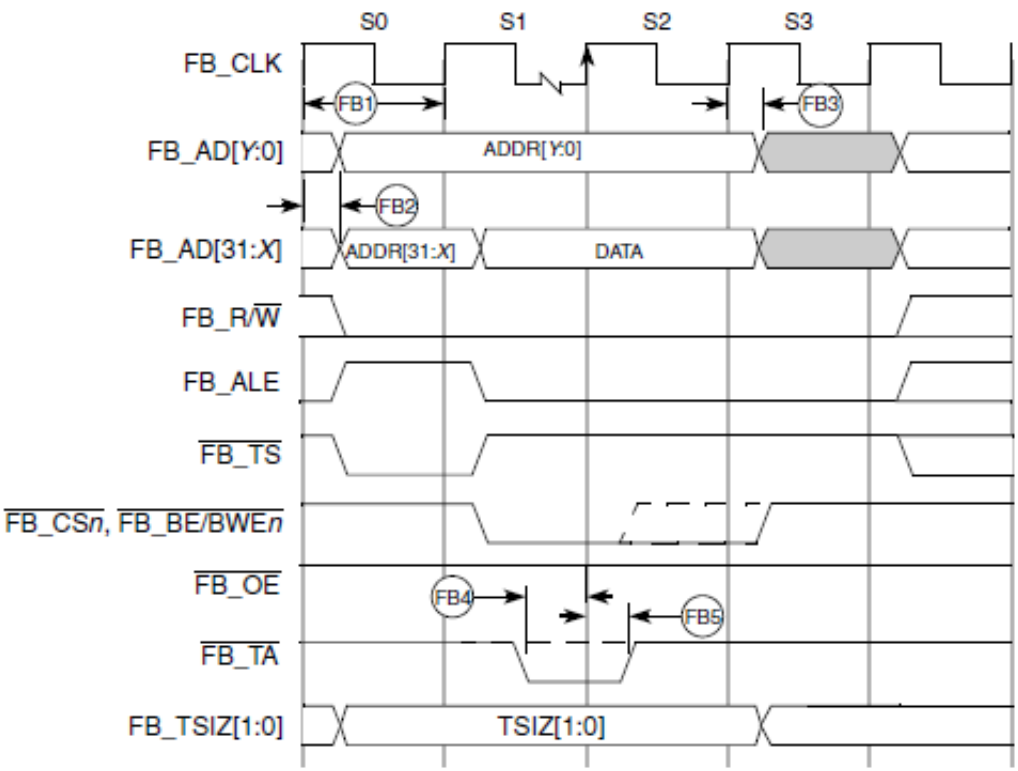


Figure 40. FlexBus write timing

9.5.4.3 DDR3 Write cycle

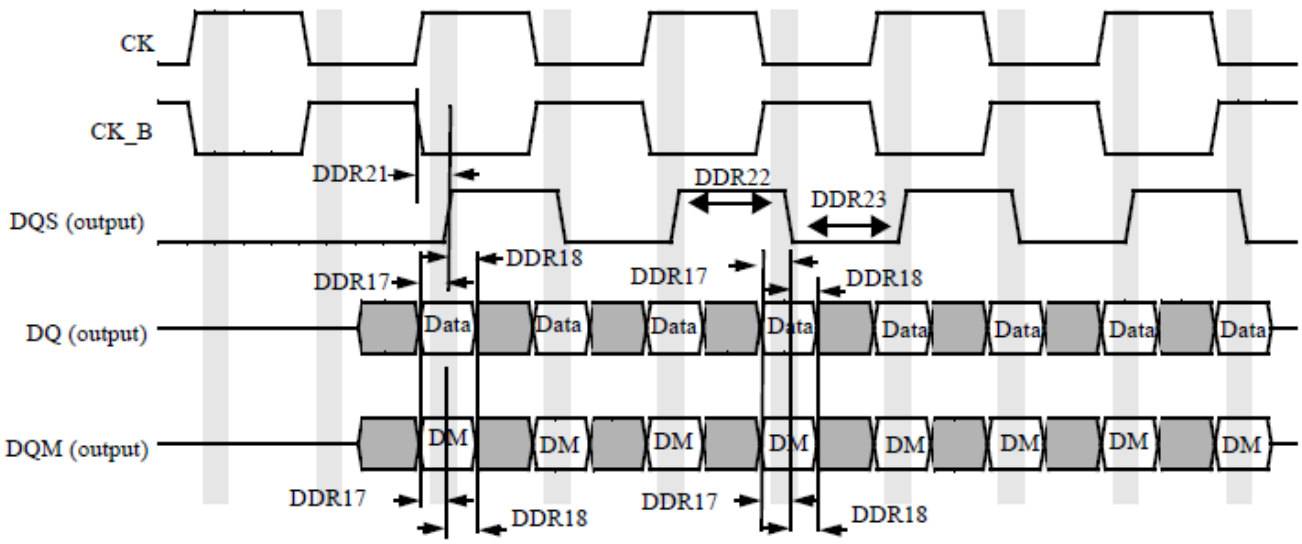


Figure 43. DDR3 Write cycle

Table 56. DDR3 Write cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	240	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	215	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR22	DQS low level width	tDQSL	0.45	0.55	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.6 Communication interfaces

9.6.1 MediaLB (MLB) DC Characteristics

The section lists the MediaLB 3-pin interface electrical characteristics.

Table 60. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = –6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	$_{IL}$	0 < Vin < VDD	—	±10	µA

1. Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

9.6.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module.

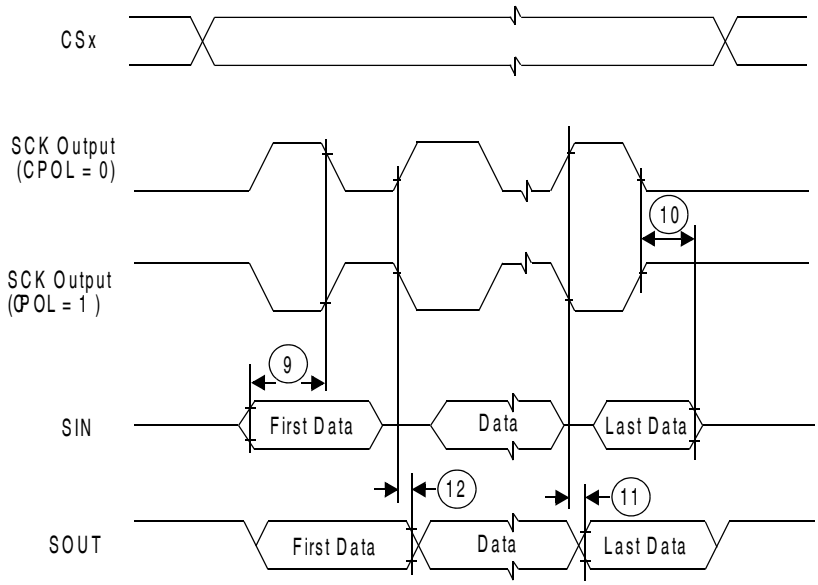


Figure 49. DSPI classic SPI timing master, CPHA=1

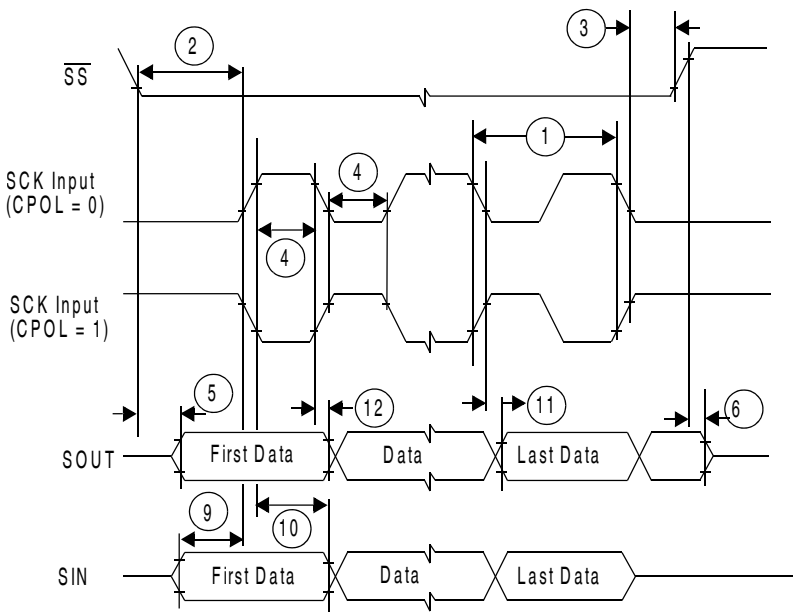


Figure 50. DSPI classic SPI timing slave, CPHA=0

Table 67. 24MHz external oscillator electrical characteristics (continued)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{IN}	Input Capacitance	EXTAL and XTAL pins	—	9	—	pF
VIH	XTAL pin input high voltage	—	0.8 x Vdd[1]	—	Vdd +0.3	V
VIL	XTAL pin input low voltage	—	Vss -0.3	—	0.2 x Vdd	V

1. V_{DD} =1.1 V ± 10%, TA = -40 to +85 °C, unless otherwise specified.

9.7.2 32 KHz Oscillator Specifications

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery or VDDIO such as the oscillator consumes power from VDDIO when that supply is available and transitions to the back up battery when VDDIO is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to the 128kHz internal RC clock divided by 4.

The OSC32k runs from vdd_rtc supply, generated inside OSC32k itself from VDDIO/ VBAT. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDIO range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell.

For example:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

Table 68. OSC32K Main Characteristics

	Notes	Min	Typ	Max
F_{OSC}	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.		32.768 KHz	
Current consumption	The 4 µA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 µA when ring oscillator is inactive, 20 µA when the ring		4 µA	

Table continues on the next page...

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_SYNC	I2C2_SDA	DCU1_DE/DCU1_TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_VBUS_EN			SDHC1_CLK	DCU1_TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_VBUS_OC			SDHC1_CMD	DCU1_TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_BCLK			SDHC1_DAT0	DCU1_TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_BCLK			SDHC1_DAT1	DCU1_TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_DATA	ENET1_1588_TMR0	SCI4_TX	SDHC1_DAT2	DCU1_TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_DATA	ENET1_1588_TMR1	SCI4_RX	SDHC1_DAT3	DCU1_TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_SYNC	ENET1_1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_SYNC	ENET1_1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_BCLK	VIU_DATA18	QSPI1_A_CS0	
T7	50	PTB1	RCON30	PTB1	FTM0_CH1	ADC0_SE3	RCON30	LCD35	SAI2_RX_DATA	VIU_DATA19	QSPI1_A_DATA3	
V7	51	PTB2	RCON31	PTB2	FTM0_CH2	ADC1_SE2	RCON31	LCD36	SAI2_RX_SYNC	VIU_DATA20	QSPI1_A_DATA2	
W7	53	PTB3		PTB3	FTM0_CH3	ADC1_SE3	EXTRIG	LCD37		VIU_DATA21	QSPI1_A_DATA1	
Y7	54	PTB4		PTB4	FTM0_CH4	SCI1_TX	ADC0_SE4	LCD38	VIU_FID	VIU_DATA22	QSPI1_A_DATA0	
Y8	55	PTB5		PTB5	FTM0_CH5	SCI1_RX	ADC1_SE4	LCD39	VIU_DE	VIU_DATA23	QSPI1_A_DQS	
W8	56	PTB6		PTB6	FTM0_CH6	SCI1_RTS	QSPI0_A_CS1	LCD40	FB_CLKOUT	VIU_HSYNC	SCI2_TX	
D13	166	PTB7		PTB7	FTM0_CH7	SCI1_CTS	QSPI0_B_CS1	LCD41		VIU_VSYNC	SCI2_RX	
J16	121	PTB8		PTB8	FTM1CH0		FTM1_QD_PHA		VIU_DE		DCU1_R6	
J19	123	PTB9		PTB9	FTM1CH1		FTM1_QD_PHB				DCU1_R7	
B15	159	PTB10		PTB10	SCI0_TX			DCU0_TCON4	VIU_DE	CKO1	ENET_TS_CLKIN	
D14	164	PTB11		PTB11	SCI0_RX			DCU0_TCON5	SNVS_ALARM_OUT_B	CKO2	ENET0_1588_TMR0	
E13	165	PTB12	NMI	PTB12	SCI0_RTS		SPI0_PCS5	DCU0_TCON6	FB_AD1	NMI	ENET0_1588_TMR1	
D15	156	PTB13		PTB13	SCI0_CTS		SPI0_PCS4	DCU0_TCON7	FB_AD0	TRACECTL		

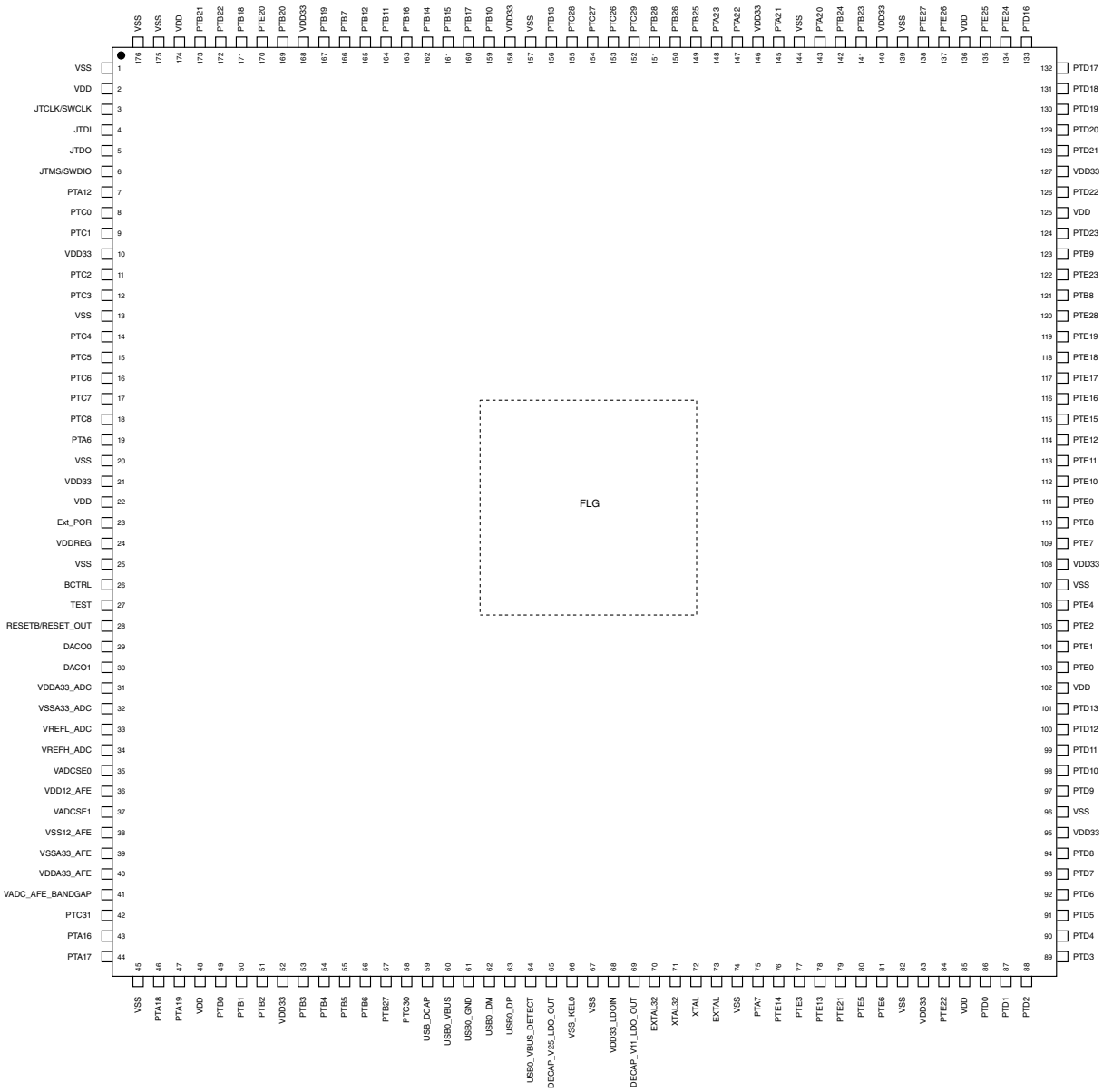
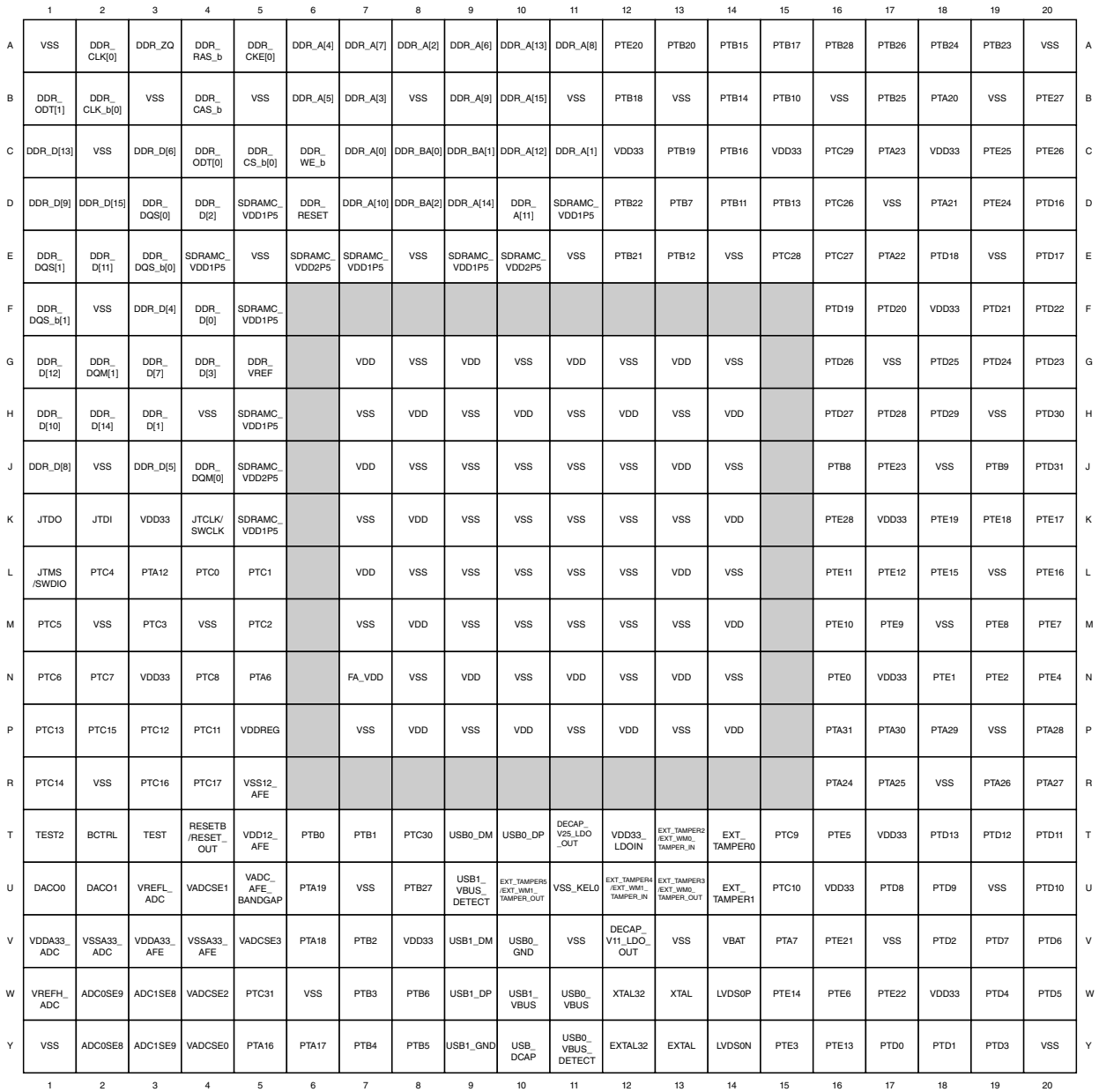


Figure 59. 176 LQFP Pinout Diagram



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	DDR_ CLK[0]	DDR_ZQ	DDR_ RAS_b	DDR_ CKE[0]	DDR_A[4]	DDR_A[7]	DDR_A[2]	DDR_A[6]	DDR_A[13]	DDR_A[8]	PTE20	PTB20	PTB15	PTB17	PTB28	PTB26	PTB24	PTB23	VSS	A
B	DDR_ ODT[1]	DDR_ CLK_b[0]	VSS	DDR_ CAS_b	VSS	DDR_A[5]	DDR_A[3]	VSS	DDR_A[9]	DDR_A[15]	VSS	PTB18	VSS	PTB14	PTB10	VSS	PTB25	PTA20	VSS	PTE27	B
C	DDR_D[13]	VSS	DDR_D[6]	DDR_ ODT[0]	DDR_ CS_b[0]	DDR_ WE_b	DDR_A[0]	DDR_BA[0]	DDR_BA[1]	DDR_A[12]	DDR_A[1]	VDD33	PTB19	PTB16	VDD33	PTC29	PTA23	VDD33	PTE25	PTE26	C
D	DDR_D[9]	DDR_D[15]	DDR_ DQS[0]	DDR_ D[2]	SDRAMC_ VDD1P5	DDR_ RESET	DDR_A[10]	DDR_BA[2]	DDR_A[14]	DDR_ A[11]	SDRAMC_ VDD1P5	PTB22	PTB7	PTB11	PTB13	PTC26	VSS	PTA21	PTE24	PTD16	D
E	DDR_ DQS[1]	DDR_ D[11]	DDR_ DQS_b[0]	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD2P5	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD1P5	SDRAMC_ VDD2P5	VSS	PTB21	PTB12	VSS	PTC28	PTC27	PTA22	PTD18	VSS	PTD17	E
F	DDR_ DQS_b[1]	VSS	DDR_D[4]	DDR_ D[0]	SDRAMC_ VDD1P5											PTD19	PTD20	VDD33	PTD21	PTD22	F
G	DDR_ D[12]	DDR_ DQM[1]	DDR_ D[7]	DDR_ D[3]	DDR_ VREF		VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTD26	VSS	PTD25	PTD24	PTD23	G
H	DDR_ D[10]	DDR_ D[14]	DDR_ D[1]	VSS	SDRAMC_ VDD1P5		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTD27	PTD28	PTD29	VSS	PTD30	H
J	DDR_D[8]	VSS	DDR_D[5]	DDR_ DQM[0]	SDRAMC_ VDD2P5		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTB8	PTE23	VSS	PTB9	PTD31	J
K	JTDO	JTDI	VDD33	JTCLK/ SWCLK	SDRAMC_ VDD1P5		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE28	VDD33	PTE19	PTE18	PTE17	K
L	JTMS /SWDIO	PTC4	PTA12	PTC0	PTC1		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTE11	PTE12	PTE15	VSS	PTE16	L
M	PTC5	VSS	PTC3	VSS	PTC2		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE10	PTE9	VSS	PTE8	PTE7	M
N	PTC6	PTC7	VDD33	PTC8	PTA6		FA_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTE0	VDD33	PTE1	PTE2	PTE4	N
P	PTC13	PTC15	PTC12	PTC11	VDDREG		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTA31	PTA30	PTA29	VSS	PTA28	P
R	PTC14	VSS	PTC16	PTC17	VSS12_ AFE											PTA24	PTA25	VSS	PTA26	PTA27	R
T	TEST2	BCTRL	TEST	RESETB /RESET_ OUT	VDD12_ AFE	PTB0	PTB1	PTC30	USB0_DM	USB0_DP	DECAP_ V25_LDO _OUT	VDD33_ LDOIN	EXT_TAMPER2 /EXT_WM0_ TAMPER_IN	EXT_ TAMPER0	PTC9	PTE5	VDD33	PTD13	PTD12	PTD11	T
U	DACO0	DACO1	VREFL_ ADC	VADCSE1	VADC_ AFE_ BANDGAP	PTA19	VSS	PTB27	USB1_ VBUS_ DETECT	EXT_TAMPER5 /EXT_WM1_ TAMPER_OUT	VSS_KEL0	EXT_TAMPER4 /EXT_WM1_ TAMPER_IN	EXT_TAMPER3 /EXT_WM0_ TAMPER_OUT	EXT_ TAMPER1	PTC10	VDD33	PTD8	PTD9	VSS	PTD10	U
V	VDDA33_ ADC	VSSA33_ ADC	VDDA33_ AFE	VSSA33_ AFE	VADCSE3	PTA18	PTB2	VDD33	USB1_DM	USB0_ GND	VSS	DECAP_ V11_LDO_ OUT	VSS	VBAT	PTA7	PTE21	VSS	PTD2	PTD7	PTD6	V
W	VREFH_ ADC	ADC0SE9	ADC1SE8	VADCSE2	PTC31	VSS	PTB3	PTB6	USB1_DP	USB1_ VBUS	USB0_ VBUS	XTAL32	XTAL	LVDS0P	PTE14	PTE6	PTE22	VDD33	PTD4	PTD5	W
Y	VSS	ADC0SE8	ADC1SE9	VADCSE0	PTA16	PTA17	PTB4	PTB5	USB1_GND	USB_ DCAP	USB0_ VBUS_ DETECT	EXTAL32	EXTAL	LVDS0N	PTE3	PTE13	PTD0	PTD1	PTD3	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 60. 364-pin BGA package ballmap

12.2.1 GPIO Mapping

Table 78. RGPIO versus Pins

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[0]	PORT0[0]	PTA6	IOMUXC_PTA6	40048000

Table continues on the next page...

15 Revision History

The following table provides a revision history for this document.

Table 82. Revision History

Rev. No.	Date	Substantial Changes
Rev1	12/2011	Initial release
Rev2	02/2012	Updated feature list Updated VREG electrical specifications Updated LDO_1P1, LDO2P5 tables Updated DDR IO parameters Added DDR memory controller parameters Updated Power sequencing table Added Power supply diagram Updated Recommended operating conditions Replaced DryIce Tamper Electrical Specifications with Voltage and temperature monitor electrical specifications Updated VideoADC electricals. Updated VideoADC supply scheme diagram. Added VideoADC supply_decoupling diagram Added QuadSPI DDR mode electrical specifications Updated Fast internal RC oscillator table Updated Slow internal RC oscillator table Updated Pinouts section
Rev3	04/2012	Updated device name throughout the document Minor editorial updates in the feature list Updated VREG electrical specifications Updated LDO electrical specifications Updated Power consumption operating behaviors table Added USB PHY Current Consumption table Updated GPIO parameters Updated DDR parameters

Table continues on the next page...