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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz, 133MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	DDR3, LPDDR2
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf532r2k2cmk4

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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web.

1. To determine the orderable part numbers for this device, go to www.freescale.com and search the required part number. The part numbering format is described in the section that follows.

2 Part identification

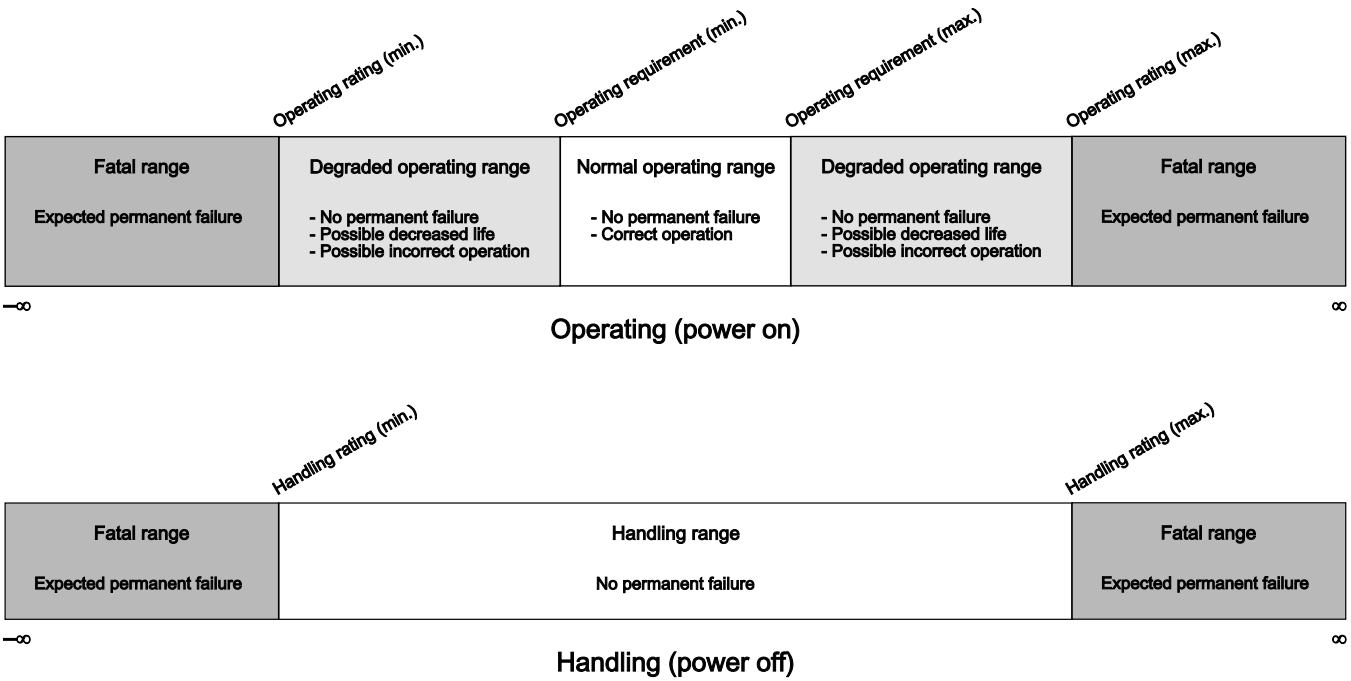
2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Part Number Format

The figure below represents the format of part number of this device.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

4 Handling ratings

4.1 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I_{LAT}	Latch-up Current at ambient temperature of 85 °C	-100	100	mA	

1. Determined according to the AEC spec AEC-Q100-002 for HBM
2. Determined according to AEC spec AEC-Q100-011

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

Table 28. Power sequencing (continued)

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VDD33_LDOIN	VDD33	LDO input supply (LDO1P1, LDO2P5, LDO1P1_RTC)	1	VDD33_LDOIN,VDDREG and VDD33 should come from a common supply source (represented as 3.3V SMPS in the Figure 4)
VDDREG	VDD33	Device PMU regulator and External ballast supply	1	
VDD33	VDD33	GPIO 3.3V IO supply, LCD Supply	1	
SDRAMC_VDD1P5	SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	NA	In case the Ballast transistor's collector is connected to the 1.5V DRAM supply (instead of the 3.3V supply), turn this 1.5V supply on before turning on the 3.3V.
VDDA33_ADC	VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	1	
VREFH_ADC	VREFH_ADC	High Reference of ADC, DAC	1	
VDDA33_AFE	VDDA33_AFE	3.3V supply of AFE (Video ADC)	1	
VDD12_AFE	VDD	1.2V supply for AFE (Video ADC)	2	
FA_VDD	VDD	Shorted with VDD at Board Level in 364BGA (Test pin only)	NA	
VDD	VDD	1.2V core supply from External ballast	2	
USB0_VBUS	USB_VBUS	VBUS supply for USB	NA	
USB1_VBUS	USB_VBUS	VBUS supply for USB	NA	

NOTE

NA stands for no sequencing needs, for example, the supply can come in any order.

NOTE

All supplies grouped together e.g. 1,2, others. These have no power sequencing restriction in between them.

NOTE

If none of the SDRAMC pins are connected on the board, the SDRAMC supply could be left floating.

NOTE

At power up, 1.2V supply will follow 3.3V supply. At power down, it should be checked that 1.2V falls before 3.3V.

NOTE

The standby current on USBx_VBUS is 300 - 500 uA. This is well below the 2.5 mA limit set by the USB 2.0 specification. This supply will be ON for applications that need to monitor the

USB bus during standby. This supply can be turned-off during standby in applications that cannot tolerate the standby current and do not monitor the USB bus.

8.2 Power supply

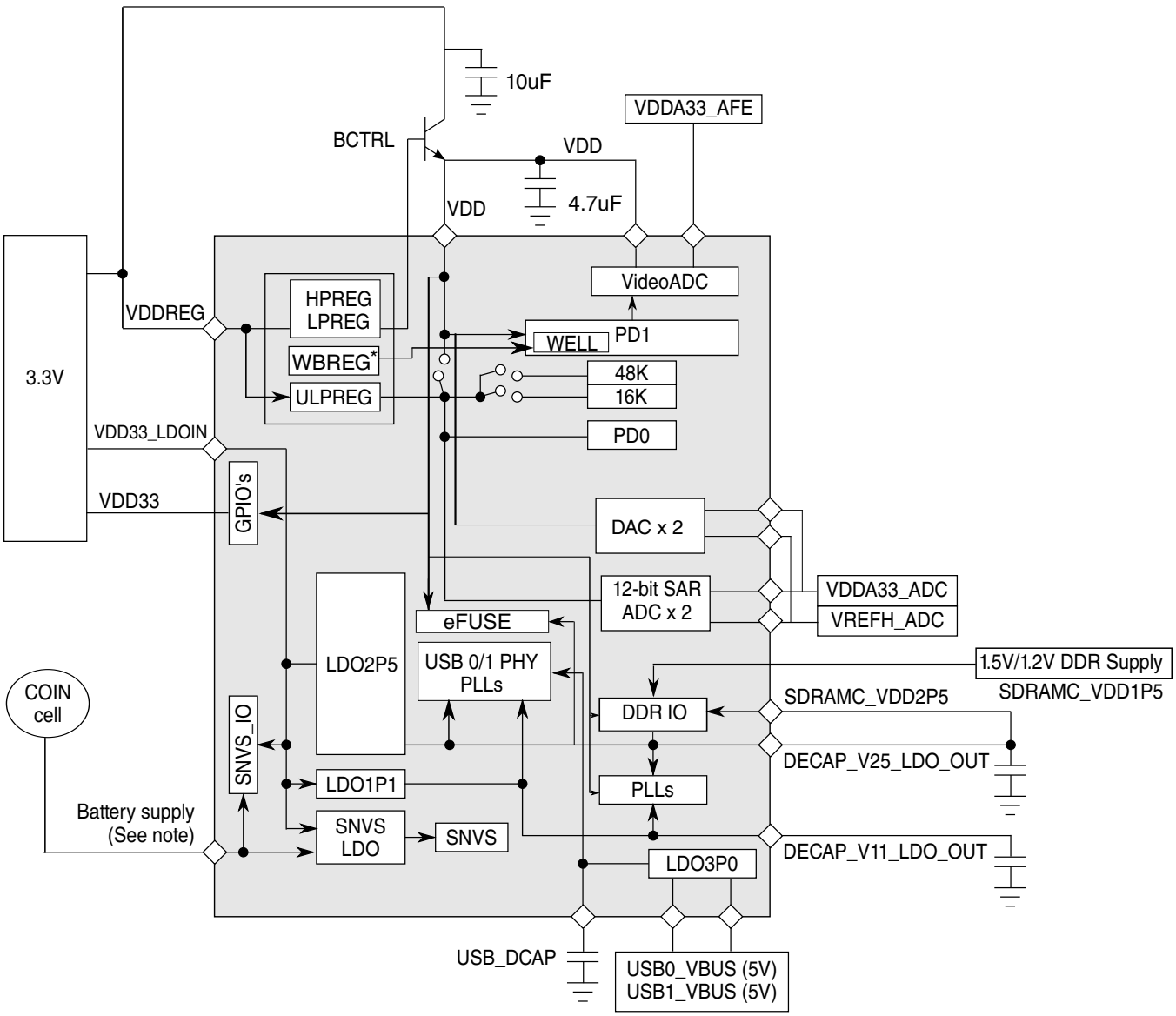


Figure 4. Power supply

NOTE

VBAT is the backup battery supply. If not required, then VBAT should be tied to VDDREG.

9.4.2 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal. Table and Figure below show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 45. SPDIF Timing Parameters

Characteristic	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply			0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling			• 1.5 • 24.2 • 31.3	ns
SPDIFOUT1 output (Load = 30pf) - Skew			1.5	ns
• Transition rising • Transition falling		Refer Table 21		
Modulating Rx clock (SRCK) period	srckp	40		ns
SRCK high period	srckph	16		ns
SRCK low period	srckpl	16		ns
Modulating Tx clock (STCLK) period	stclkp	40		ns
STCLK high period	stclkph	16		ns
STCLK low period	stclkpl	16		ns

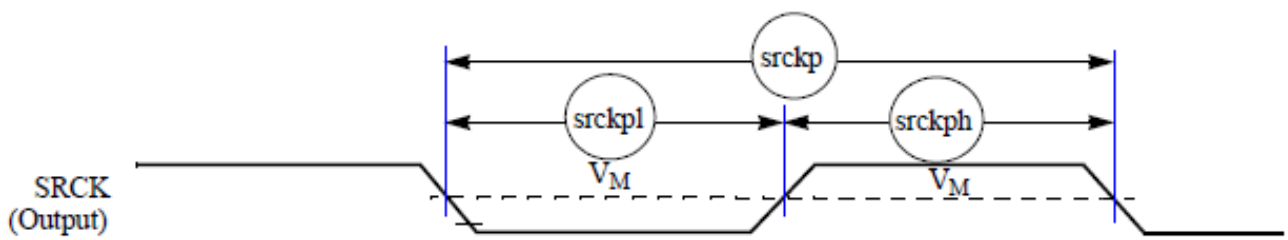


Figure 26. SRCK Timing Diagram

9.5 Memory interfaces

9.5.1 QuadSPI timing

- All data is based on a negative edge data launch from the device and a negative edge data capture, as shown in the timing diagrams in this section. This corresponds to the N/1 sample point as shown in the reference manual QSPI section "Internal Sampling of Serial Flash Input Data."
- Measurements are with a load of 35 pF on output pins. I/P Slew : 1ns
- Timings assume a setting of 0x0000_000x for QSPI_SMPR register (see the reference manual for details).

SDR mode

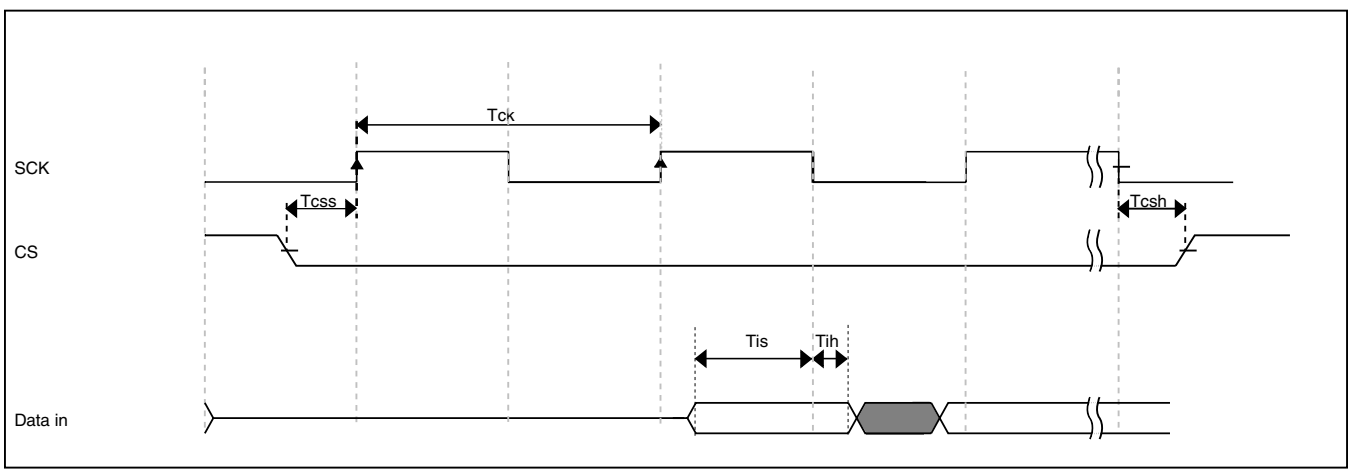


Figure 30. QuadSPI Input/Read timing (SDR mode)

Table 48. QuadSPI Input/Read timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4.5	—	ns
T_{ih}	Hold time requirement for incoming data	0	—	ns

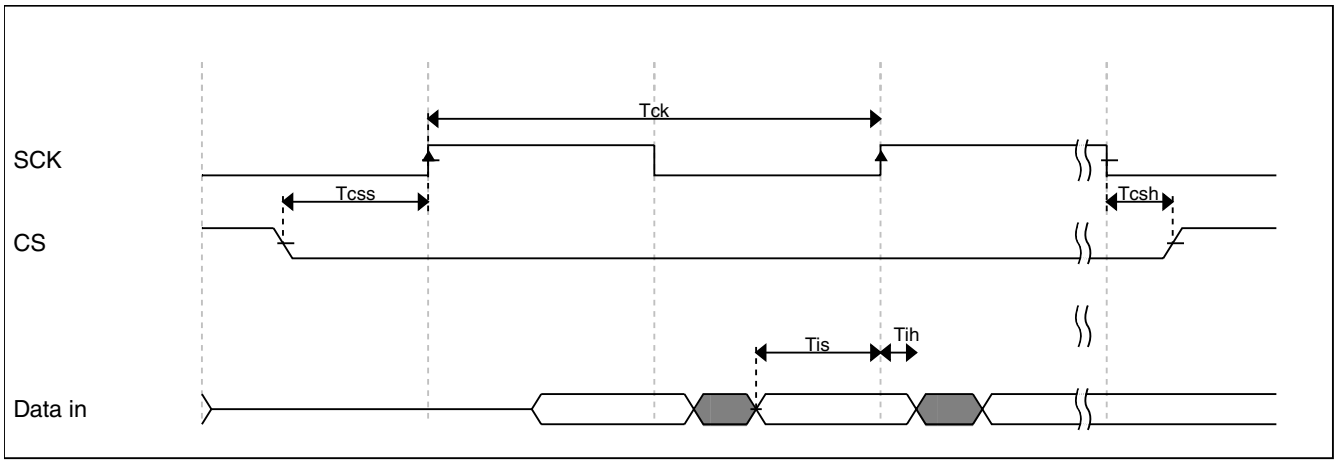


Figure 32. QuadSPI Input/Read timing (DDR mode)

NOTE

- The numbers are for a setting of 0x1 in regiater QuadSPI_SMPR[DDRSMP]
- Read frequency calculations should be: SCK/2 > (flash access time) + Setup (Tis) - (QuadSPI_SMPR[DDRSMP])x SCK/4
- Frequency calculator guideline (Max read frequency): SCK/2 > (Flash access time)max + (Tis)max - (QuadSPI_SMPR[DDRSMP]) xSCK/4
- Hold timing: flash_access (min) + flash_data_valid (min) > SCK/2 + HOLD(Tih) + (QuadSPI_SMPR[DDRSMP])SCK/4
- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.

Table 50. QuadSPI Input/Read timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	6.4	—	ns
T_{ih}	Hold time requirement for incoming data	-3.0	—	ns

NOTE

Table 63. DSPI timing (continued)

No.	Symbol	Characteristic	Condition	Min	Max	Unit
			Slave	4	—	
10	t_{HI}	Data Hold Time for Inputs	Master	0	—	ns
			Slave	2	—	
11	t_{DV}	Data Valid (after SCK edge) for Outputs	Master	—	5	ns
			Slave	—	10	
12	t_{HO}	Data Hold Time for Outputs	Master	0	—	ns
			Slave	0	—	

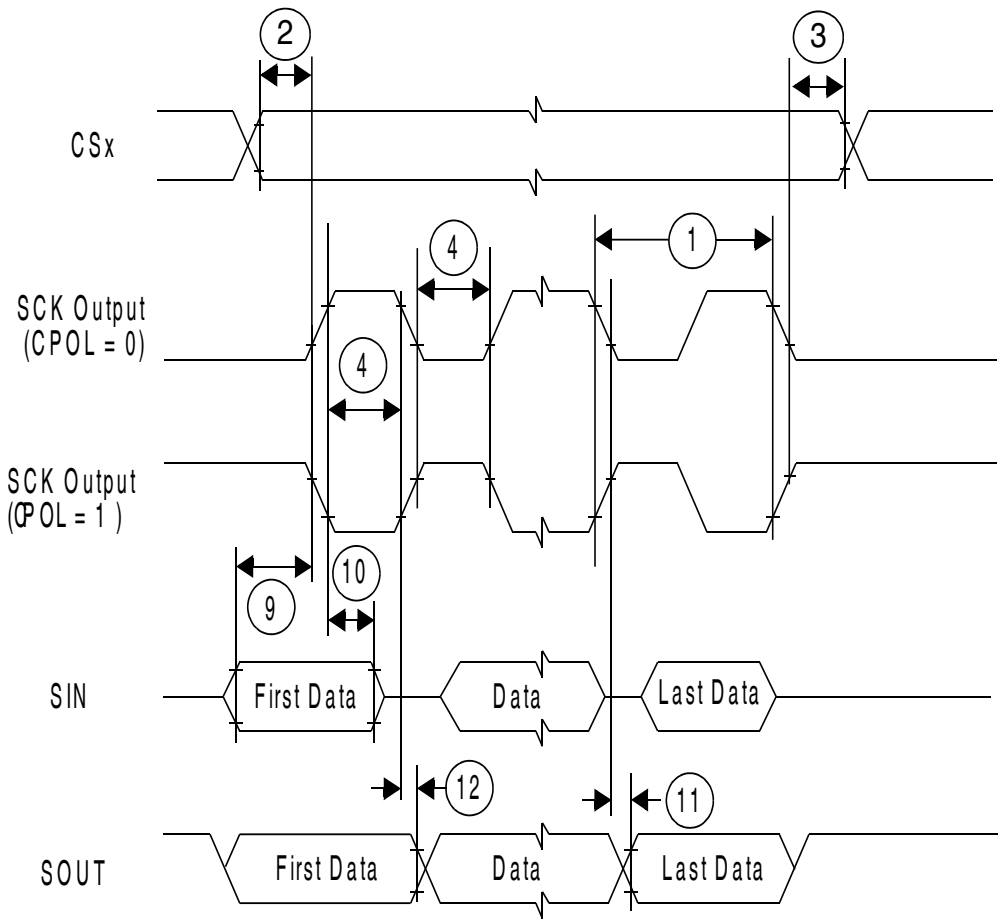


Figure 48. DSPI classic SPI timing master, CPHA=0

9.6.6 USB PHY specifications

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

9.7 Clocks and PLL Specifications

9.7.1 24 MHz Oscillator Specifications

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5.

Table 67. 24MHz external oscillator electrical characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
f_{osc}	Crystal oscillator range	—	—	24	—	MHz
I_{osc}	Startup current	—	—	< 5	—	mA
t_{uposc}	Oscillator startup time	—	—	< 5	—	ms

Table continues on the next page...

Table 67. 24MHz external oscillator electrical characteristics (continued)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{IN}	Input Capacitance	EXTAL and XTAL pins	—	9	—	pF
VIH	XTAL pin input high voltage	—	0.8 x Vdd[1]	—	Vdd +0.3	V
VIL	XTAL pin input low voltage	—	Vss -0.3	—	0.2 x Vdd	V

1. V_{DD} =1.1 V ± 10%, TA = -40 to +85 °C, unless otherwise specified.

9.7.2 32 KHz Oscillator Specifications

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery or VDDIO such as the oscillator consumes power from VDDIO when that supply is available and transitions to the back up battery when VDDIO is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to the 128kHz internal RC clock divided by 4.

The OSC32k runs from vdd_rtc supply, generated inside OSC32k itself from VDDIO/ VBAT. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDIO range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell.

For example:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

Table 68. OSC32K Main Characteristics

	Notes	Min	Typ	Max
F_{OSC}	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.		32.768 KHz	
Current consumption	The 4 µA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 µA when ring oscillator is inactive, 20 µA when the ring		4 µA	

Table continues on the next page...

Table 68. OSC32K Main Characteristics (continued)

	Notes	Min	Typ	Max
	oscillator is running. Another 1.5 µA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 µA on vdd_rtc when the ring oscillator is not running.			
Bias resistor	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.		14 MΩ	
Crystal Properties				
Cload	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal		12.5 pF	
ESR	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.		50 kΩ	

9.7.3 Fast internal RC oscillator (24 MHz) electrical characteristics

This section describes a fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 69. Fast internal oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCM}	RC oscillator high frequency	T_A= 25 °C, trimmed	—	24	—	MHz
I_{RCMRUN}	RC oscillator high frequency current in running mode	T_A= 25 °C, trimmed	—	55		µA
I_{RCMPWD}	RC oscillator high frequency current in power down mode	T_A= 25 °C		100		nA
RCMTRIM	RC oscillator precision after trimming of f_{RC}	T_A= 25 °C	-1	—	+1	%
RCMVAR	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration		-5		+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.8.2 Debug trace timing specifications

Table 77. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	50		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	Refer Table 21		ns
T_f	Clock and data fall time Refer			ns
tDV	Data output valid	3	—	ns
tHO	Data output hold	1	—	ns

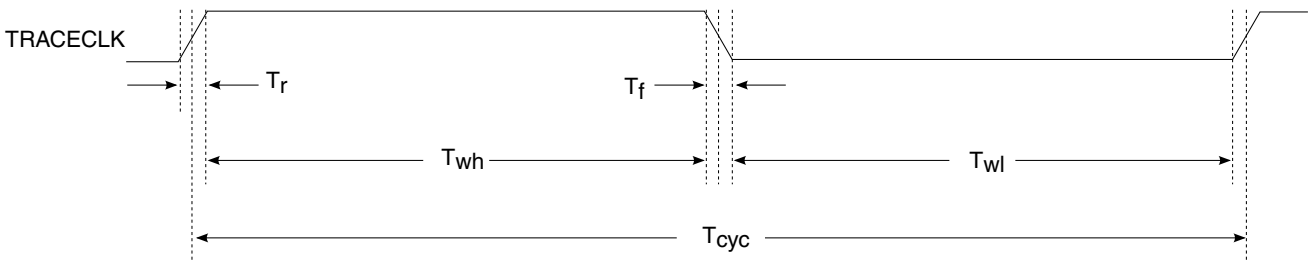


Figure 57. TRACE_CLKOUT specifications

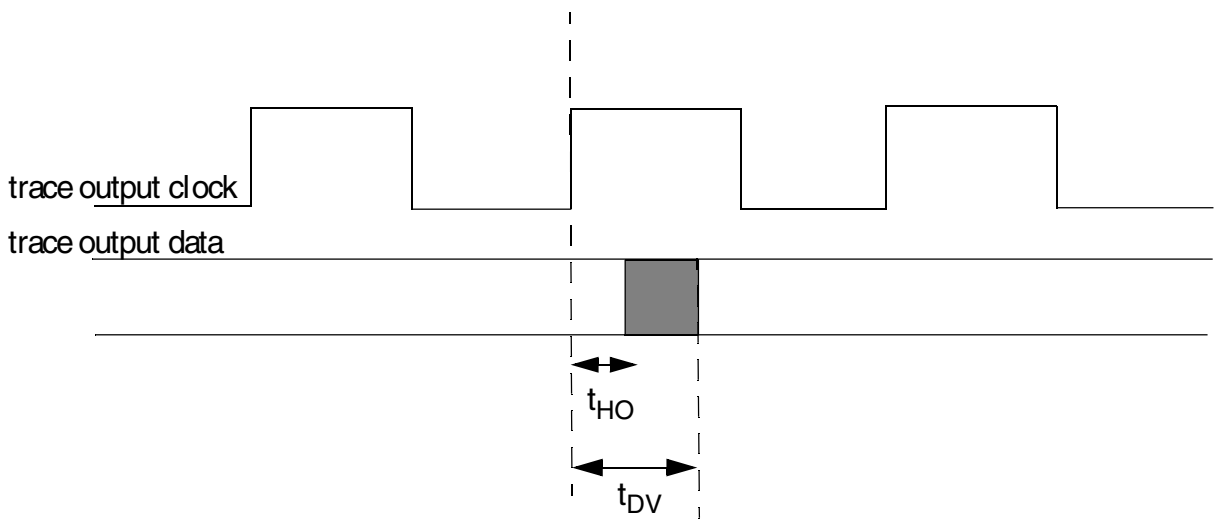


Figure 58. Trace data specifications

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_SYNC	I2C2_SDA	DCU1_DE/DCU1_TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_VBUS_EN			SDHC1_CLK	DCU1_TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_VBUS_OC			SDHC1_CMD	DCU1_TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_BCLK			SDHC1_DAT0	DCU1_TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_BCLK			SDHC1_DAT1	DCU1_TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_DATA	ENET1_1588_TMR0	SCI4_TX	SDHC1_DAT2	DCU1_TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_DATA	ENET1_1588_TMR1	SCI4_RX	SDHC1_DAT3	DCU1_TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_SYNC	ENET1_1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_SYNC	ENET1_1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_BCLK	VIU_DATA18	QSPI1_A_CS0	
T7	50	PTB1	RCON30	PTB1	FTM0_CH1	ADC0_SE3	RCON30	LCD35	SAI2_RX_DATA	VIU_DATA19	QSPI1_A_DATA3	
V7	51	PTB2	RCON31	PTB2	FTM0_CH2	ADC1_SE2	RCON31	LCD36	SAI2_RX_SYNC	VIU_DATA20	QSPI1_A_DATA2	
W7	53	PTB3		PTB3	FTM0_CH3	ADC1_SE3	EXTRIG	LCD37		VIU_DATA21	QSPI1_A_DATA1	
Y7	54	PTB4		PTB4	FTM0_CH4	SCI1_TX	ADC0_SE4	LCD38	VIU_FID	VIU_DATA22	QSPI1_A_DATA0	
Y8	55	PTB5		PTB5	FTM0_CH5	SCI1_RX	ADC1_SE4	LCD39	VIU_DE	VIU_DATA23	QSPI1_A_DQS	
W8	56	PTB6		PTB6	FTM0_CH6	SCI1_RTS	QSPI0_A_CS1	LCD40	FB_CLKOUT	VIU_HSYNC	SCI2_TX	
D13	166	PTB7		PTB7	FTM0_CH7	SCI1_CTS	QSPI0_B_CS1	LCD41		VIU_VSYNC	SCI2_RX	
J16	121	PTB8		PTB8	FTM1CH0		FTM1_QD_PHA		VIU_DE		DCU1_R6	
J19	123	PTB9		PTB9	FTM1CH1		FTM1_QD_PHB				DCU1_R7	
B15	159	PTB10		PTB10	SCI0_TX			DCU0_TCON4	VIU_DE	CKO1	ENET_TS_CLKIN	
D14	164	PTB11		PTB11	SCI0_RX			DCU0_TCON5	SNVS_ALARM_OUT_B	CKO2	ENET0_1588_TMR0	
E13	165	PTB12	NMI	PTB12	SCI0_RTS		SPI0_PCS5	DCU0_TCON6	FB_AD1	NMI	ENET0_1588_TMR1	
D15	156	PTB13		PTB13	SCI0_CTS		SPI0_PCS4	DCU0_TCON7	FB_AD0	TRACECTL		

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G20	124	PTD23		PTD23/ MII0_ RXDATA[3]	FB_AD23	NF_IO7	FTM2CH0	ENET0_ 1588_TMR0	SDHC0_ DAT4	SCI2_TX	DCU1_R3	
F20	126	PTD22		PTD22/ MII0_ RXDATA[2]	FB_AD22	NF_IO6	FTM2CH1	ENET0_ 1588_TMR1	SDHC0_ DAT5	SCI2_RX	DCU1_R4	
F19	128	PTD21		PTD21/ MII0_CRS	FB_AD21	NF_IO5		ENET0_ 1588_TMR2	SDHC0_ DAT6	SCI2_RTS	DCU1_R5	
F17	129	PTD20		PTD20/ MII0_COL	FB_AD20	NF_IO4		ENET0_ 1588_TMR3	SDHC0_ DAT7	SCI2_CTS	DCU1_R0	
F16	130	PTD19		PTD19	FB_AD19	NF_IO3	ESAI_SCKR	I2C0_SCL	FTM2_QD_ PHA	MII0_ TXDATA[3]	DCU1_R1	
E18	131	PTD18		PTD18	FB_AD18	NF_IO2	ESAI_FSR	I2C0_SDA	FTM2_QD_ PHB	MII0_ TXDATA[2]	DCU1_G0	
E20	132	PTD17		PTD17	FB_AD17	NF_IO1	ESAI_HCKR	I2C1_SCL		MII0_TXERR	DCU1_G1	
D20	133	PTD16		PTD16	FB_AD16	NF_IO0	ESAI_HCKT	I2C1_SDA			DCU1_G2	
Y17	86	PTD0		PTD0	QSPI0_A_ SCK	SCI2_TX		FB_AD15	SPDIF_ EXTCLK			
Y18	87	PTD1		PTD1	QSPI0_A_ CS0	SCI2_RX		FB_AD14	SPDIF_IN1			
V18	88	PTD2		PTD2	QSPI0_A_ DATA3	SCI2_RTS	SPI1_PCS3	FB_AD13	SPDIF_OUT1			
Y19	89	PTD3		PTD3	QSPI0_A_ DATA2	SCI2_CTS	SPI1_PCS2	FB_AD12	SPDIF_ PLOCK			
W19	90	PTD4		PTD4	QSPI0_A_ DATA1		SPI1_PCS1	FB_AD11	SPDIF_ SRCLK			
W20	91	PTD5		PTD5	QSPI0_A_ DATA0		SPI1_PCS0	FB_AD10				
V20	92	PTD6		PTD6	QSPI0_A_ DQS		SPI1_SIN	FB_AD9				
V19	93	PTD7		PTD7	QSPI0_B_ SCK		SPI1_SOUT	FB_AD8				
U17	94	PTD8		PTD8	QSPI0_B_ CS0	FB_CLKOUT	SPI1_SCK	FB_AD7				
U18	97	PTD9		PTD9	QSPI0_B_ DATA3	SPI3_PCS1		FB_AD6		SAI1_TX_ SYNC	DCU1_B0	
U20	98	PTD10		PTD10	QSPI0_B_ DATA2	SPI3_PCS0		FB_AD5			DCU1_B1	
T20	99	PTD11		PTD11	QSPI0_B_ DATA1	SPI3_SIN		FB_AD4				
T19	100	PTD12		PTD12	QSPI0_B_ DATA0	SPI3_SOUT		FB_AD3				
T18	101	PTD13		PTD13	QSPI0_B_ DQS	SPI3_SCK		FB_AD2				
A19	141	PTB23		PTB23	SAI0_TX_ BCLK	SCI1_TX		FB_MUXED_ ALE	FB_TS_b	SCI3_RTS	DCU1_G3	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
W15	76	PTE14		PTE14	DCU0_G1			LCD14				
L18	115	PTE15	RCON6	PTE15	DCU0_G2		RCON6	LCD15				
L20	116	PTE16	RCON7	PTE16	DCU0_G3		RCON7	LCD16				
K20	117	PTE17	RCON8	PTE17	DCU0_G4		RCON8	LCD17				
K19	118	PTE18	RCON9	PTE18	DCU0_G5		RCON9	LCD18				
K18	119	PTE19	RCON10	PTE19	DCU0_G6		RCON10	LCD19	I2C0_SCL			
A12	170	PTE20	RCON11	PTE20	DCU0_G7		RCON11	LCD20	I2C0_SDA		EWM_in	
V16	79	PTE21		PTE21	DCU0_B0			LCD21				
W17	84	PTE22		PTE22	DCU0_B1			LCD22				
J17	122	PTE23	RCON12	PTE23	DCU0_B2		RCON12	LCD23				
D19	134	PTE24	RCON13	PTE24	DCU0_B3		RCON13	LCD24				
C19	135	PTE25	RCON14	PTE25	DCU0_B4		RCON14	LCD25				
C20	137	PTE26	RCON15	PTE26	DCU0_B5		RCON15	LCD26				
B20	138	PTE27	RCON16	PTE27	DCU0_B6		RCON16	LCD27	I2C1_SCL			
K16	120	PTE28	RCON17	PTE28	DCU0_B7		RCON17	LCD28	I2C1_SDA		EWM_out	
V15	75	PTA7		PTA7	VIU_PIX_CLK							
T14	—	EXT_TAMPER0			EXT_TAMPER0							
U14	—	EXT_TAMPER1			EXT_TAMPER1							
T13	—	EXT_TAMPER2/EXT_WM0_TAMPER_IN			EXT_TAMPER2/EXT_WM0_TAMPER_IN							
U13	—	EXT_TAMPER3/EXT_WM0_TAMPER_OUT			EXT_TAMPER3/EXT_WM0_TAMPER_OUT							
U12	—	EXT_TAMPER4/EXT_WM1_TAMPER_IN			EXT_TAMPER4/EXT_WM1_TAMPER_IN							
U10	—	EXT_TAMPER5/EXT_WM1_TAMPER_OUT			EXT_TAMPER5/EXT_WM1_TAMPER_OUT							
G7	2	VDD			VDD							
J7	22	VDD			VDD							
L7	48	VDD			VDD							
H8	—	VDD			VDD							
K8	85	VDD			VDD							
M8	102	VDD			VDD							

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[1]	PORT0[1]	PTA8	IOMUXC_PTA8	40048004
RGPIO[2]	PORT0[2]	PTA9	IOMUXC_PTA9	40048008
RGPIO[3]	PORT0[3]	PTA10	IOMUXC_PTA10	4004800C
RGPIO[4]	PORT0[4]	PTA11	IOMUXC_PTA11	40048010
RGPIO[5]	PORT0[5]	PTA12	IOMUXC_PTA12	40048014
RGPIO[6]	PORT0[6]	PTA16	IOMUXC_PTA16	40048018
RGPIO[7]	PORT0[7]	PTA17	IOMUXC_PTA17	4004801C
RGPIO[8]	PORT0[8]	PTA18	IOMUXC_PTA18	40048020
RGPIO[9]	PORT0[9]	PTA19	IOMUXC_PTA19	40048024
RGPIO[10]	PORT0[10]	PTA20	IOMUXC_PTA20	40048028
RGPIO[11]	PORT0[11]	PTA21	IOMUXC_PTA21	4004802C
RGPIO[12]	PORT0[12]	PTA22	IOMUXC_PTA22	40048030
RGPIO[13]	PORT0[13]	PTA23	IOMUXC_PTA23	40048034
RGPIO[14]	PORT0[14]	PTA24	IOMUXC_PTA24	40048038
RGPIO[15]	PORT0[15]	PTA25	IOMUXC_PTA25	4004803C
RGPIO[16]	PORT0[16]	PTA26	IOMUXC_PTA26	40048040
RGPIO[17]	PORT0[17]	PTA27	IOMUXC_PTA27	40048044
RGPIO[18]	PORT0[18]	PTA28	IOMUXC_PTA28	40048048
RGPIO[19]	PORT0[19]	PTA29	IOMUXC_PTA29	4004804C
RGPIO[20]	PORT0[20]	PTA30	IOMUXC_PTA30	40048050
RGPIO[21]	PORT0[21]	PTA31	IOMUXC_PTA31	40048054
RGPIO[22]	PORT0[22]	PTB0	IOMUXC_PTB0	40048058
RGPIO[23]	PORT0[23]	PTB1	IOMUXC_PTB1	4004805C
RGPIO[24]	PORT0[24]	PTB2	IOMUXC_PTB2	40048060
RGPIO[25]	PORT0[25]	PTB3	IOMUXC_PTB3	40048064
RGPIO[26]	PORT0[26]	PTB4	IOMUXC_PTB4	40048068
RGPIO[27]	PORT0[27]	PTB5	IOMUXC_PTB5	4004806C
RGPIO[28]	PORT0[28]	PTB6	IOMUXC_PTB6	40048070
RGPIO[29]	PORT0[29]	PTB7	IOMUXC_PTB7	40048074
RGPIO[30]	PORT0[30]	PTB8	IOMUXC_PTB8	40048078
RGPIO[31]	PORT0[31]	PTB9	IOMUXC_PTB9	4004807C
RGPIO[32]	PORT1[0]	PTB10	IOMUXC_PTB10	40048080
RGPIO[33]	PORT1[1]	PTB11	IOMUXC_PTB11	40048084
RGPIO[34]	PORT1[2]	PTB12	IOMUXC_PTB12	40048088
RGPIO[35]	PORT1[3]	PTB13	IOMUXC_PTB13	4004808C
RGPIO[36]	PORT1[4]	PTB14	IOMUXC_PTB14	40048090
RGPIO[37]	PORT1[5]	PTB15	IOMUXC_PTB15	40048094
RGPIO[38]	PORT1[6]	PTB16	IOMUXC_PTB16	40048098
RGPIO[39]	PORT1[7]	PTB17	IOMUXC_PTB17	4004809C

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Table 79. Special Signal Considerations (continued)

Special Signal	Comments
JTCLK, JTDI, JTDO, JTMS	For JTAG the use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is matched. For example, do not use an external pull down on an input that has on-chip pull-up. JTDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTDO is detrimental and should be avoided.
LVDS0N, LVDS0P	Not recommended for application use, intended for clock observation purposes during debug only.
RESETB/RESET_OUT	Active low input used to generate a system wide reset (except the SRTC). A glitch filter is include to help prevent unexpected resets, a minimum pulse width of 125 nsecs is required to guarantee a reset is detected.
XTAL, EXTAL	A 24.0 MHz fundamental mode crystal should be connected between XTAL and EXTAL. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTAL must be directly driven by the external oscillator and EXTAL floated. The XTAL signal level must swing from ~0.8 x DECAP_V11_ LDO_OUT to ~0.2 V.
XTAL32, EXTAL32	If the user wishes to configure XTAL32 and EXTAL32 as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between XTAL32 and EXTAL32. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTAL32 and EXTAL32 to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTAL32 and EXTAL32 should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTAL32 the EXTAL32 pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed DECAP_V11_ LDO_OUT level and the frequency should be <100 kHz under typical conditions. In the case where the SIRC is used, it is recommended to connect XTAL32 to ground and leave EXTAL32 floating.

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTB3	W7	53	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB4	Y7	54	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB5	Y8	55	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB6	W8	56	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB7	D13	166	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB8	J16	121	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB9	J19	123	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB10	B15	159	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB11	D14	164	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB12	E13	165	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB13	D15	156	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB14	B14	162	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB15	A14	161	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB16	C14	163	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB17	A15	160	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB18	B12	171	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB19	C13	167	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB20	A13	169	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB21	E12	173	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB22	D12	172	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB23	A19	141	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB24	A18	142	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB25	B17	149	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB26	A17	150	VDD33	GPIO	ALT3	RCON21	Input	Disabled
PTB27	U8	57	VDD33	GPIO	ALT3	RCON22	Input	Disabled
PTB28	A16	151	VDD33	GPIO	ALT3	RCON23	Input	Disabled
PTC0	L4	8	VDD33	GPIO	ALT7	RCON18	Input	Disabled
PTC1	L5	9	VDD33	GPIO	ALT7	RCON19	Input	Disabled
PTC2	M5	11	VDD33	GPIO	ALT7	RCON20	Input	Disabled
PTC3	M3	12	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC4	L2	14	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC5	M1	15	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC6	N1	16	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC7	N2	17	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC8	N4	18	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC9	T15	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC10	U15	—	VDD33	GPIO	ALT0	GPIO	Disabled	

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